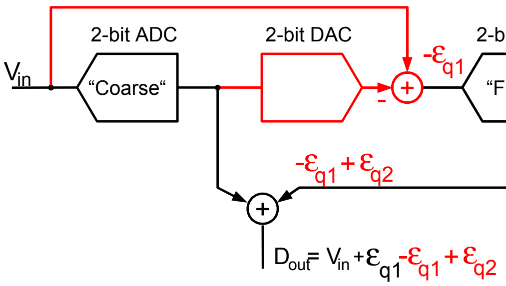
EE247
Lecture 22

ADC Converters

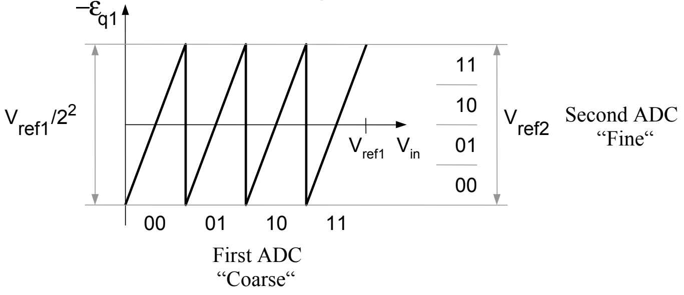
- Techniques to reduce flash ADC complexity (continued)
  - Multi-Step ADCs
    - Two-Step flash
    - Pipelined ADCs
      - Effect of sub-ADC, sub-DAC, gain stage non-idealities on overall ADC performance
        - Error correction by adding redundancy
        - Digital calibration

Two Stage Example



- Use DAC to compute missing voltage
- Add quantized representation of missing voltage
- Why does this help? How about ε_{q2} ?

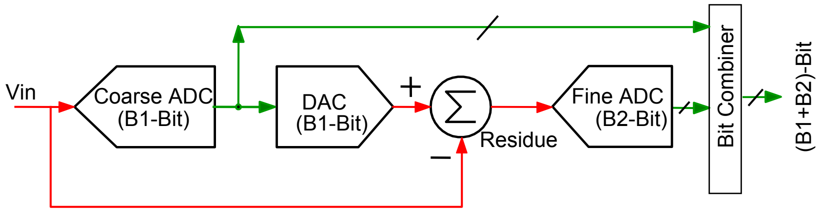
Two Stage Example



- Fine ADC is re-used 2^2 times
- Fine ADC's full scale range needs to span only 1 LSB of coarse quantizer

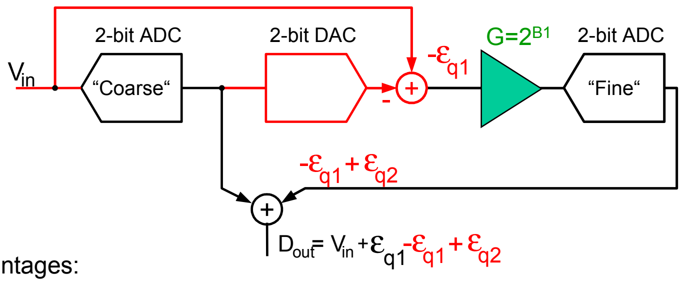
$$\varepsilon_{q2} = \frac{V_{ref2}}{2^2} = \frac{V_{ref1}}{2^2 \cdot 2^2}$$

Residue or Multi-Step Type ADC Issues



- Operation:
  - Coarse ADC determines MSBs
  - DAC converts the coarse ADC output to analog- Residue is found by subtracting (V_{in}-V_{DAC})
  - Fine ADC converts the residue and determines the LSBs
  - Bits are combined in digital domain
- Issue:
  1. Fine ADC has to have precision in the order of overall ADC 1/2LSB
  2. Speed penalty →Need at least 1 clock cycle per extra series stage to resolve one sample

Solution to Issue (1)
Reducing Precision Required for Fine ADC



Advantages:

- Accuracy needed for fine ADC relaxed by introducing inter-stage gain
  - Example: By adding gain of x($G=2^{B1}=4$) prior to fine ADC in (2+2)bit case, precision required for fine ADC is reduced from 4 to 2-bit only!
- Full-scale input same for both → coarse and fine ADC can be identical stages
- Same reference voltage used for all stage w/o need for scaling down of Vref

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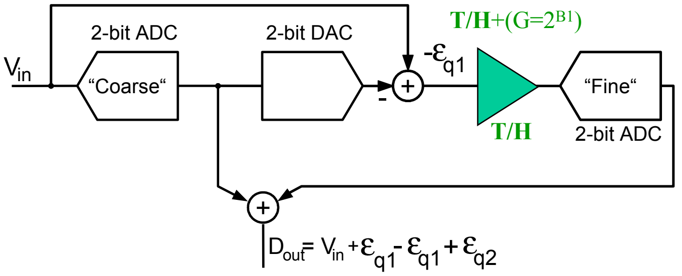
Solution to Issue (2)
Increasing ADC Throughput

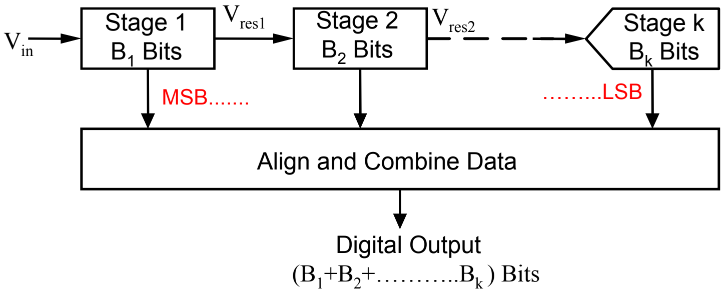


- Conversion time significantly decreased by employing T/H between stages
  - All stages busy at all times → operation concurrent
  - During one clock cycle coarse & fine ADCs operate concurrently:
    - First stage samples/converts/generates residue of input signal sample # *n*
    - While 2nd stage samples/converts residue associated with sample # *n-1*

Pipelined A/D Converters

- Ideal operation
- Errors and correction
  - Redundancy
  - Digital calibration
- Implementation
  - Practical circuits
  - Stage scaling

Pipeline ADC Block Diagram



V_{in}

Stage 1 B_1 Bits

V_{res1}

Stage 2 B_2 Bits

V_{res2}

Stage k B_k Bits

MSB.......

………..LSB

Align and Combine Data

Digital Output

$(B_1+B_2+\ldots\ldots\ldots B_k)$ Bits

- Idea: Cascade several low resolution stages to obtain high overall resolution (e.g. 10bit ADC can be built with series of 10 ADCs each 1-bit only!)
- Each stage performs coarse A/D conversion and computes its quantization error, or "residue“
- All stages operate concurrently

Pipeline ADC
Characteristics

- Number of components (stages) grows linearly with resolution
- Pipelining
  - Trading latency for resolution
  - Latency may be an issue in e.g. control systems
  - Throughput limited by speed of one stage → Fast
- Versatile: 8...16bits, 1...200MS/s
- One important feature of pipeline ADC: many analog circuit non-idealities can be corrected digitally

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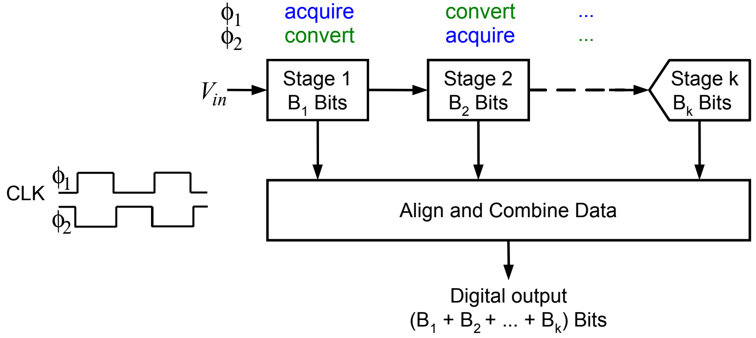
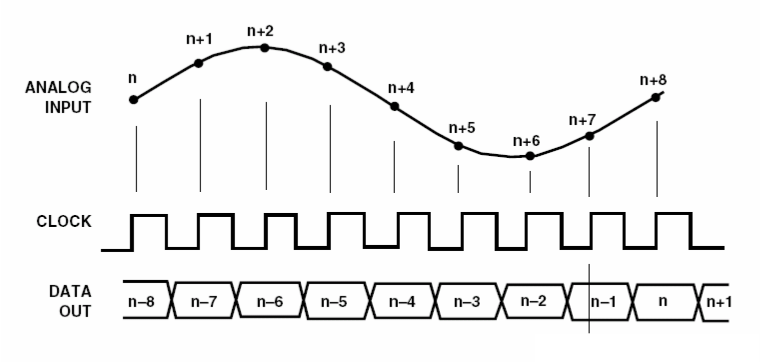
Pipeline ADC
Concurrent Stage Operation



- Stages operate on the input signal like a shift register
- New output data *every* clock cycle, but each stage introduces at least ½ clock cycle latency

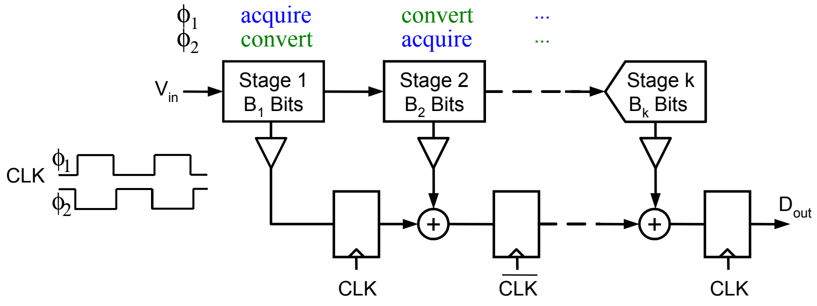
Pipeline ADC
Latency



Note: One conversion per clock cycle & 8 clock cycle latency

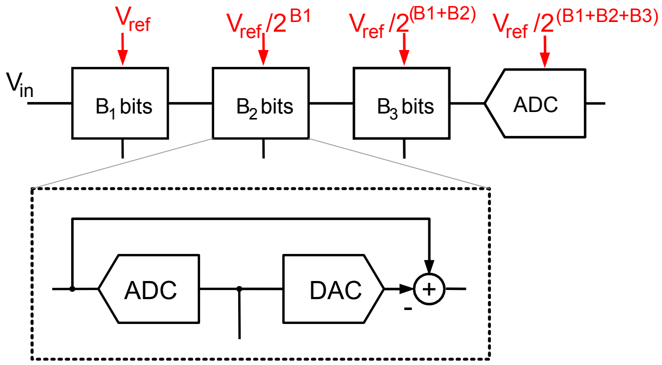
[Analog Devices, AD 9226 Data Sheet]

Pipeline ADC
Digital Data Alignment



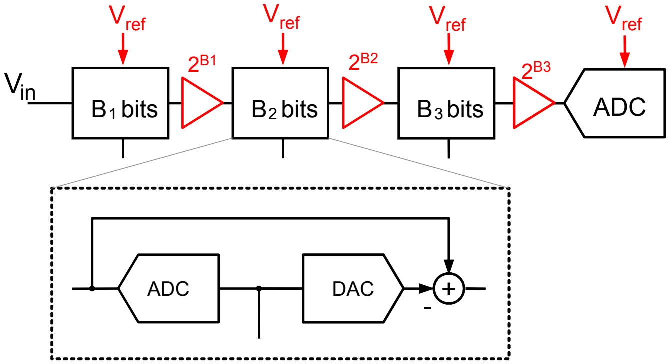
- Digital shift register aligns sub-conversion results in time

Cascading More Stages



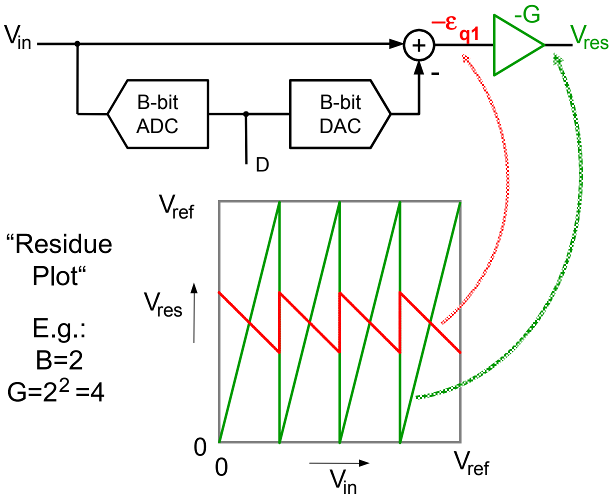
- LSB of last stage becomes very small
- Impractical to generate several V_{ref}
- All stages need to have full precision

Pipeline ADC
Inter-Stage Gain Elements



- Practical pipelines by adding inter-stage gain → use single V_{ref}
- Precision requirements decrease down the pipe
  - Advantageous for noise, matching (later), power dissipation

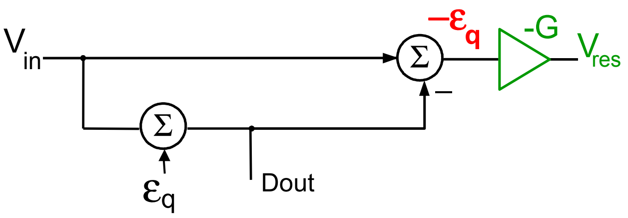
Complete Pipeline Stage



"Residue Plot"

E.g.:
B=2
$G=2^2=4$

Pipeline ADC Single Stage Model

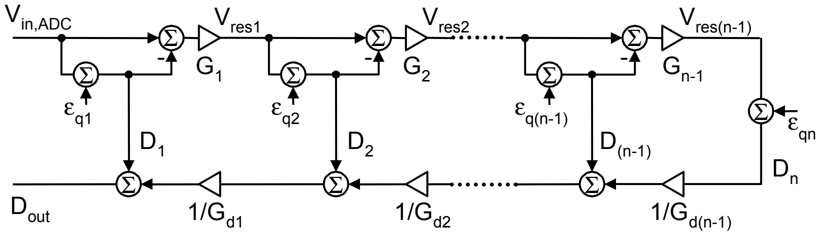


$$V_{res} = G \times \varepsilon_q$$

Pipeline ADC Errors

- Non-idealities associated with sub-ADCs, sub-DACs and gain stages → error in overall pipeline ADC performance
- Need to find means to tolerate/correct errors
- Important sources of error
  - Sub-ADC errors- comparator offset
  - Gain stage offset
  - Gain stage gain error
  - Sub-DAC error

Pipeline ADC Multi-Stage Model



$$D_{out} = V_{in,ADC} + \varepsilon_{q1}\left(1-\frac{G_1}{G_{d1}}\right) + \frac{\varepsilon_{q2}}{G_{d1}}\left(1-\frac{G_2}{G_{d2}}\right) + \dots + \frac{\varepsilon_{q(n-1)}}{\prod_{j=1}^{n-2} G_{dj}}\left(1-\frac{G_{(n-1)}}{G_{d(n-1)}}\right) + \frac{\varepsilon_{qn}}{\prod_{j=1}^{n-1} G_{dj}}$$

Pipeline ADC Model

- If the "Analog" and "Digital" gain/loss is precisely matched:

$$D_{out} = V_{in,ADC} + \frac{\varepsilon_{qn}}{\prod_{j=1}^{n-1} G_j}$$

$$D.R. = 20\log\frac{rms\ FS\ Signal}{rms\ Quant.\ Noise} = 20\log\frac{\frac{V_{ref}}{2\sqrt{2}}}{\frac{V_{ref}}{\sqrt{12}\times 2^{B_n}\prod_{j=1}^{n-1} G_j}} = 20\log\left(\sqrt{\frac{3}{2}}\times 2^{B_n}\times\prod_{j=1}^{n-1} G_j\right)$$

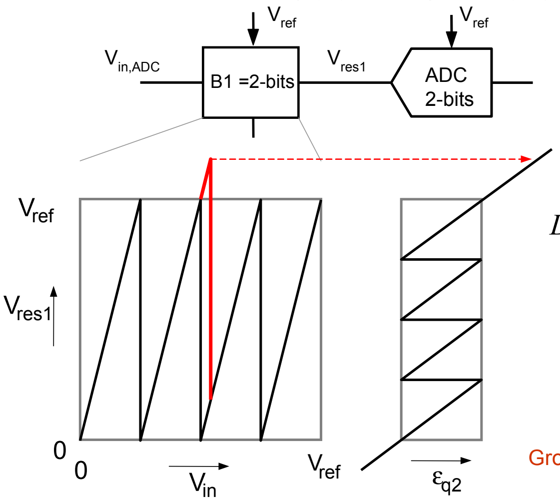
$$B_{ADC} \approx \log_2\left(2^{B_n}\times\prod_{j=1}^{n-1} G_j\right)$$

$$B_{ADC} \approx B_n + \log_2\prod_{j=1}^{n-1} G_j = B_n + \sum_{j=1}^{n-1}\log_2 G_j$$

Pipeline ADC Observations

- The aggregate **ADC resolution is independent of sub-ADC resolution!**
- *Effective* stage resolution $B_j = \log_2(G_j)$
- **Overall conversion error does not (directly) depend on sub-ADC errors!**
- Only error term in D_{out} contains quantization error associated with the last stage
- So why do we care about sub-ADC errors?
  - ➢ Go back to two stage example

Pipeline ADC
Sub-ADC Errors

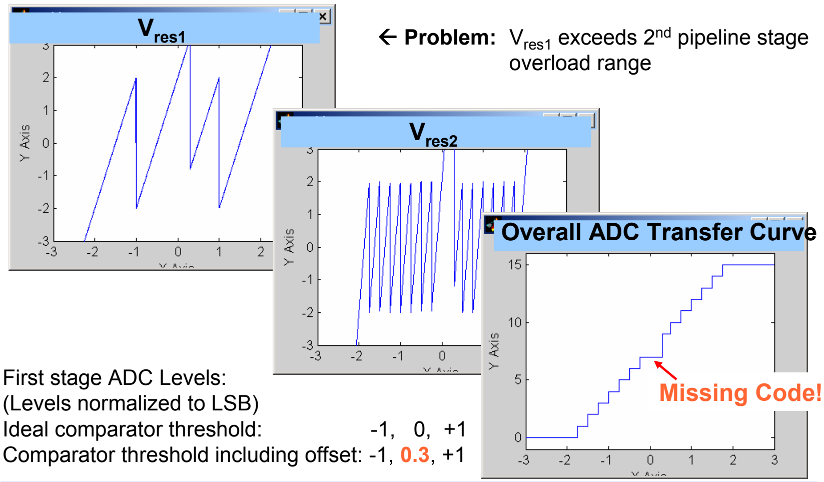


$$D_{out} = V_{in,ADC} + \frac{\varepsilon_{qn}}{\prod_{j=1}^{n-1} G_j}$$

$$D_{out} = V_{in,ADC} + \boxed{\frac{\varepsilon_{q2}}{G_1}}$$

Grows outside ½ LSB bounds

Pipeline ADC
1st-Stage Comparator Offset


V_{res1}

V_{res2}

Overall ADC Transfer Curve

Missing Code!

← **Problem:** V_{res1} exceeds 2nd pipeline stage overload range

First stage ADC Levels:
(Levels normalized to LSB)
Ideal comparator threshold: -1, 0, +1
Comparator threshold including offset: -1, 0.3, +1

Pipeline ADC
Three Ways to Deal with Errors

- All involve "sub-ADC redundancy"
- Redundancy in stage that produces errors
  - Choose gain for residue to be processed by the 2nd stage < 2^{B1}
  - Higher resolution sub-ADC & sub-DAC
- Redundancy in succeeding stage(s)

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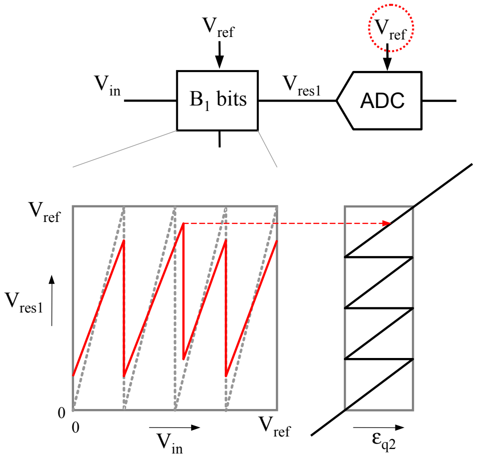
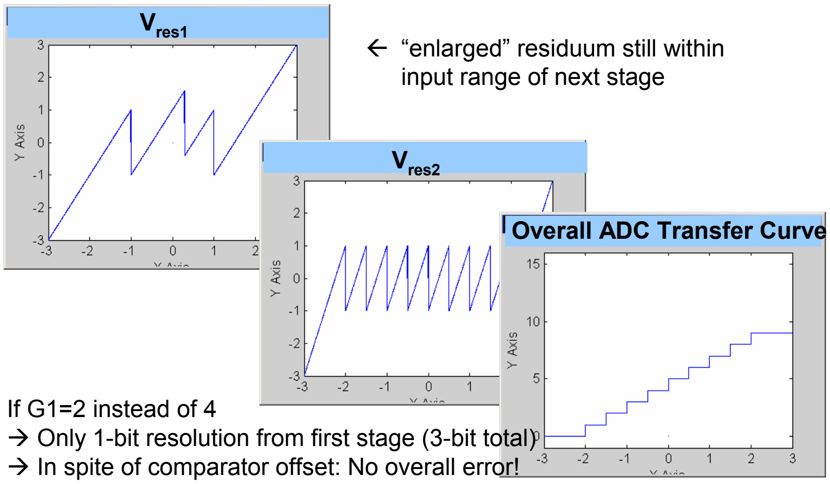
(1) Inter-Stage Gain Following 1st Stage <2^{B1}



- Choose G_1 less than 2^{B1}
- Effective stage resolution could become non-integer $B_{1eff}=\log_2 G_1$
- E.g. if $G_1=3.8$ → $B_{1eff}=1.8$bit

-Ref: A. Karanicolas et. al., JSSC 12/1993

Correction Through Redundancy



← “enlarged” residuum still within input range of next stage

If G1=2 instead of 4
→ Only 1-bit resolution from first stage (3-bit total)
→ In spite of comparator offset: No overall error!

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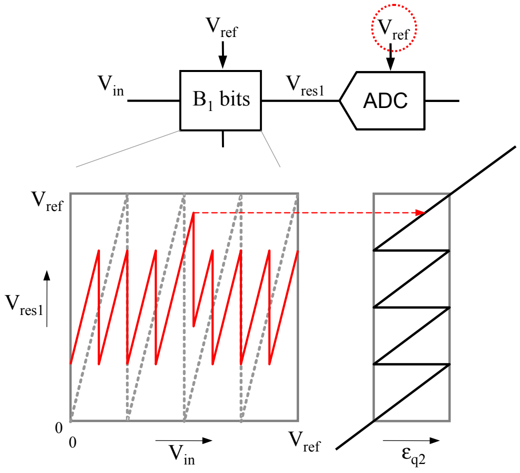
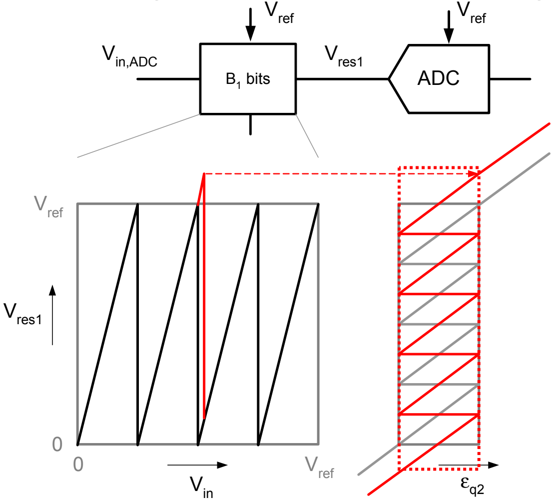
(2) Higher Resolution Sub-ADC



- Keep G1 precise power of two (e.g. G_1=4)
- Add extra decision levels in sub-ADC (e.g. add 1 extra bit to 1st stage)
- E.g. $B_1 = B_{1eff} + 1$

-Ref: Singer et. al., VSLI 1996

(3) Over-Range Accommodation Through Increase in Following Stage Resolution

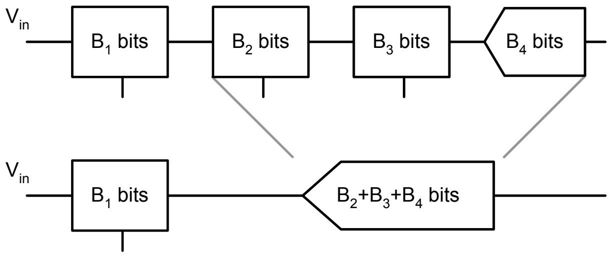


- No redundancy in stage with errors
- Add extra decision levels in succeeding stage

❖ Ref: Opris et. al., JSSC 12/1998

Redundancy

- The preceding analysis applies to any stage in an n-stage pipeline
- Can always perceive a multi-stage pipelined ADC as a single stage + backend ADC



Redundancy

- In literature, sub-ADC redundancy schemes are often called "digital correction" – a misnomer!
- No error correction takes place
- We can ***tolerate*** sub-ADC errors as long as:
  - –The residues stay "within the box", or
  - –Another stage downstream "returns the residue to “within the box" before it reaches last quantizer
- Let's calculate tolerable errors for popular "1.5 bits/stage" topology

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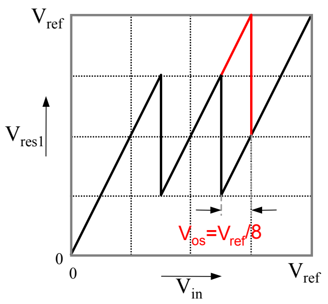
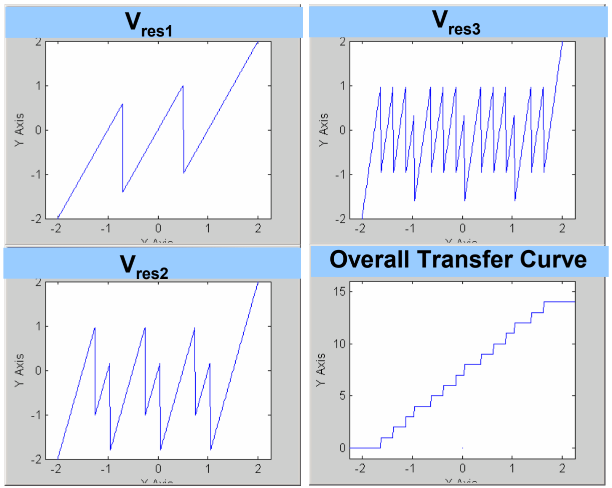
1.5 Bits/Stage Example



- Comparators placed strategically to minimize overhead
- G=2
- $B_{eff}=\log_2 G=\log_2 2=1$
- $B=\log_2(2+1)=1.589...$
- 0.5bit→ redundancy

❖ Ref: Lewis et. al., JSSC 3/1992

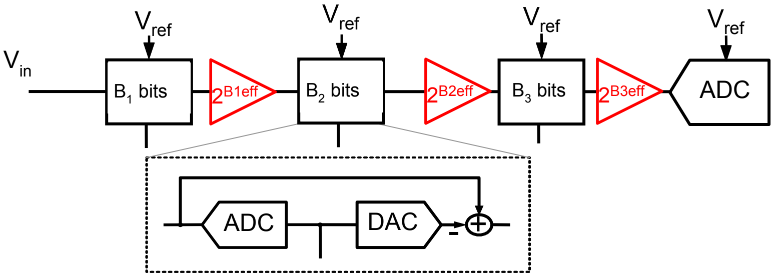
3-Stage 1.5-bit-per-Stage Pipelined ADC



- All three stages → Comparator with offset
- Overall transfer curve
  - ❑ No missing codes
  - ❑ Some DNL error

Ref: S. Lewis et al, “A 10-b 20-MS/s Analog-to-Digital Converter,” J. Solid-State Circ., pp. 351-8, March 1992

Summary So Far
Pipelined A/D Converters

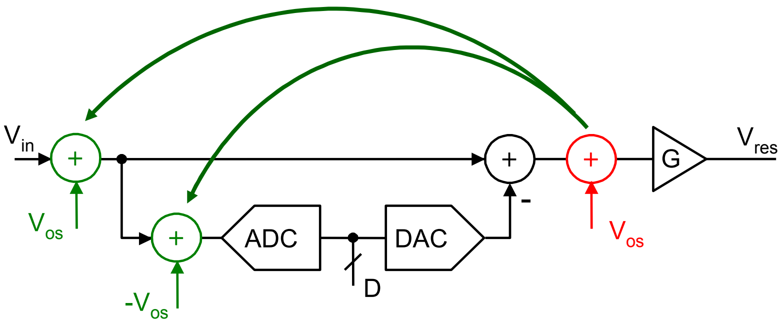


- Cascade of low resolution stages
  - Stages operate concurrently- trades latency for resolution
  - Throughput limited by speed of one stage → Fast
- Errors and correction
  - Built-in redundancy compensate for sub-ADC inaccuracies (interstage gain: $G=2^{B_{neff}}$, $B_{neff} < B_n$)

Pipeline ADC Errors

- Non-idealities associated with sub-ADCs, sub-DACs and gain stages → error in overall pipeline ADC performance
- Need to find means to tolerate/correct errors
- Important sources of error
  - Sub-ADC errors- comparator offset
  - ➡ Gain stage offset
  - Gain stage error
  - Sub-DAC error

Inter-Stage Amplifier Offset

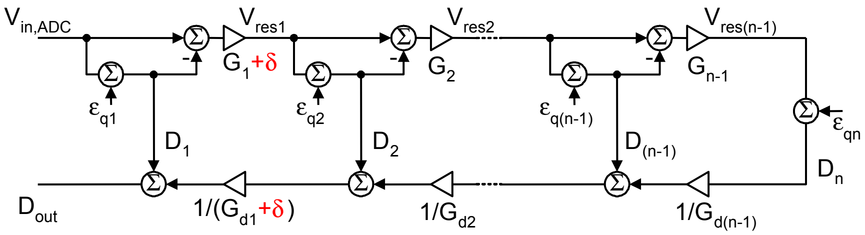


- Input referred converter offset – usually no problem
- Equivalent sub-ADC offset - accommodated through adequate redundancy

Pipeline ADC Errors

- Non-idealities associated with sub-ADCs, sub-DACs and gain stages → error in overall pipeline ADC performance
- Need to find means to tolerate/correct errors
- Important sources of error
  - Sub-ADC errors- comparator offset
  - Gain stage offset
  - ⇨ Gain stage gain error
  - Sub-DAC error

Gain Stage Gain Error

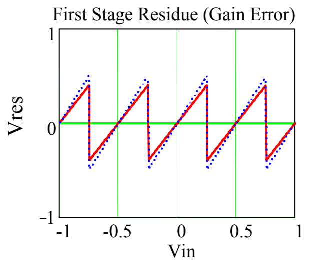


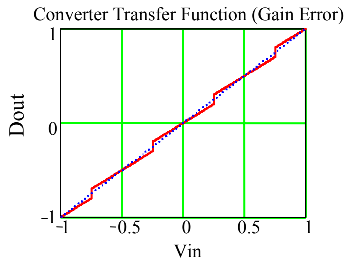
$$D_{out} = V_{in,ADC} + \varepsilon_{q1}\left(1-\frac{G_1+\delta}{G_{d1}+\delta}\right)$$

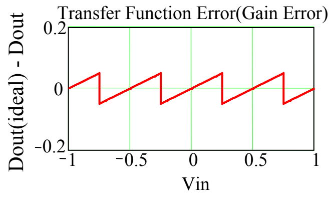
$$+\frac{\varepsilon_{q2}}{G_{d1}}\left(1-\frac{G_2}{G_{d2}}\right)+\ldots+\frac{\varepsilon_{q(n-1)}}{\prod_{j=1}^{n-2} G_{dj}}\left(1-\frac{G_{(n-1)}}{G_{d(n-1)}}\right)+\frac{\varepsilon_{qn}}{\prod_{j=1}^{n-1} G_{dj}}$$

→ Small amount of gain error can be tolerated

Interstage Gain Error



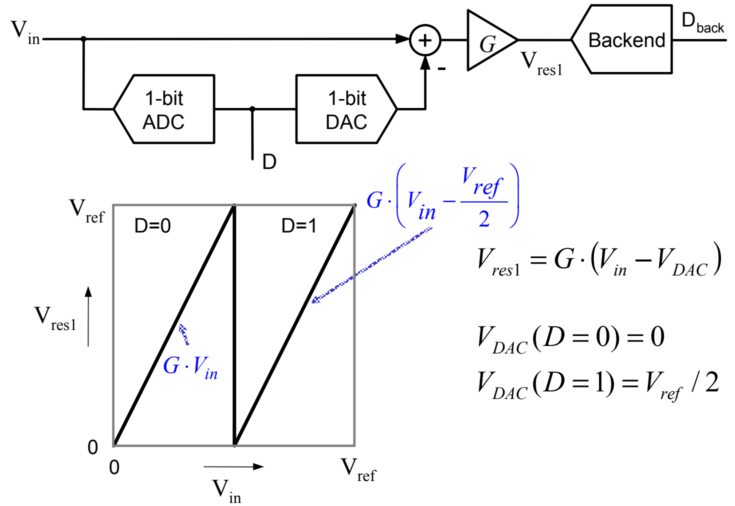




Gain Stage Gain Inaccuracy

- Gain error can be compensated in digital domain – "Digital Calibration"
- Problem: Need to measure/calibrate digital correction coefficient
- Example: Calibrate 1-bit first stage
- Objective: Measure G in digital domain

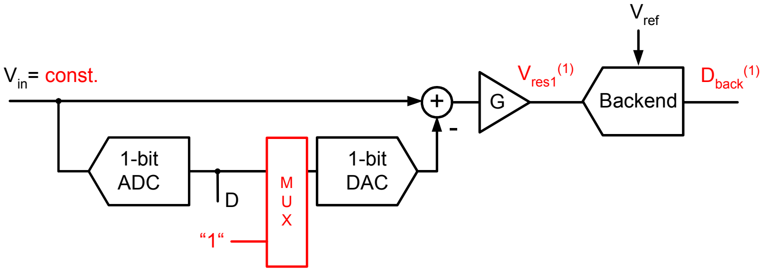
ADC Model



$$V_{res1}=G\cdot\left(V_{in}-V_{DAC}\right)$$

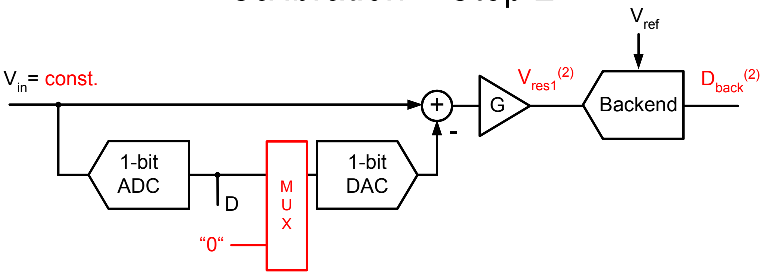
$$V_{DAC}(D=0)=0$$
$$V_{DAC}(D=1)=V_{ref}/2$$

Gain Stage Inacurracy Calibration – Step 1



$$V_{res1}^{(1)}=G\cdot\left(V_{in}-V_{ref}/2\right)$$
$$D_{back}^{(1)}=G\cdot\frac{\left(V_{in}-V_{ref}/2\right)}{V_{ref}}\rightarrow store$$

Gain Stage Inacurracy Calibration – Step 2



$$V_{res1}^{(2)} = G \cdot (V_{in} - 0)$$

$$D_{back}^{(2)} = G \cdot \frac{(V_{in} - 0)}{V_{ref}} \rightarrow store$$

Gain Stage Inacurracy Calibration – Evaluate

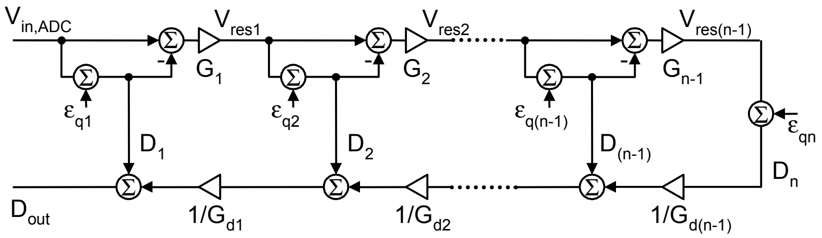
$$D_{back}^{(1)} = G \cdot \frac{(V_{in} - V_{ref}/2)}{V_{ref}}$$

$$-D_{back}^{(2)} = G \cdot \frac{(V_{in} - 0)}{V_{ref}}$$

$$D_{back}^{(1)} - D_{back}^{(2)} = \frac{1}{2} \cdot G$$

- To minimize the effect of backend ADC noise → perform measurement several times and take the average

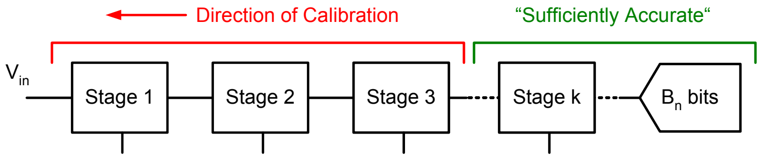
Accuracy Bootstrapping



$$D_{out} = V_{in,ADC} + \varepsilon_{q1}\left(1-\frac{G_1}{G_{d1}}\right) + \frac{\varepsilon_{q2}}{G_{d1}}\left(1-\frac{G_2}{G_{d2}}\right) + \ldots + \frac{\varepsilon_{q(n-1)}}{\prod_{j=1}^{n-2} G_{dj}}\left(1-\frac{G_{(n-1)}}{G_{d(n-1)}}\right) + \frac{\varepsilon_{qn}}{\prod_{j=1}^{n-1} G_{dj}}$$

- Highest sensitivity to gain errors in front-end stages

"Accuracy Bootstrapping"



Ref:

A. N. Karanicolas et al. "A 15-b 1-Msample/s digitally self-calibrated pipeline ADC," *IEEE J. Of Solid-State Circuits*, pp. 1207-15, Dec. 1993

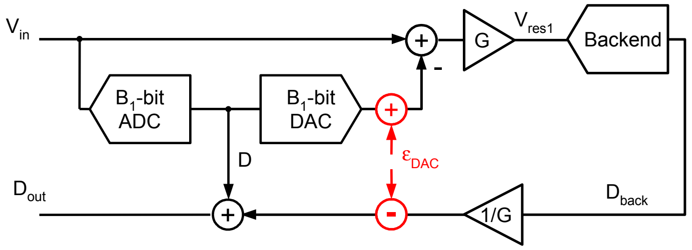
E. G. Soenen et al., "An architecture and an algorithm for fully digital correction of monolithic pipelined ADCs," TCAS II, pp. 143-153, March 1995

L. Singer et al., "A 12 b 65 MSample/s CMOS ADC with 82 dB SFDR at 120 MHz," *ISSCC 2000, Digest of Tech. Papers.*, pp. 38-9 (calibration in opposite direction!)

Pipeline ADC Errors

- Non-idealities associated with sub-ADCs, sub-DACs and gain stages → error in overall pipeline ADC performance
- Need to find means to tolerate/correct errors
- Important sources of error
  - Sub-ADC errors- comparator offset
  - Gain stage offset
  - Gain stage error
  - ➡ Sub-DAC error

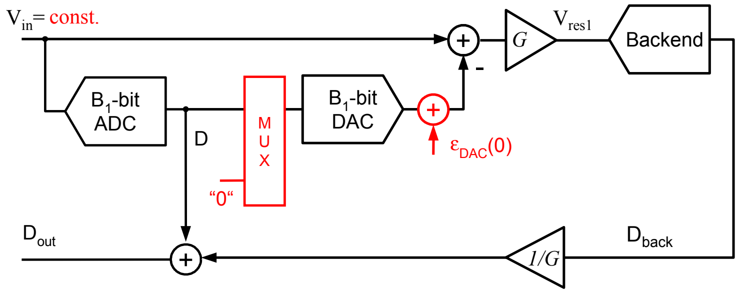
DAC Errors



- Can be corrected digitally as well
- Same calibration concept as gain errors

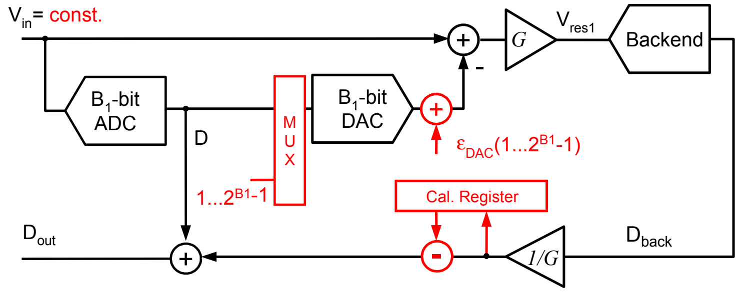
  → Vary DAC codes & measure errors via backend ADC

DAC Calibration – Step 1



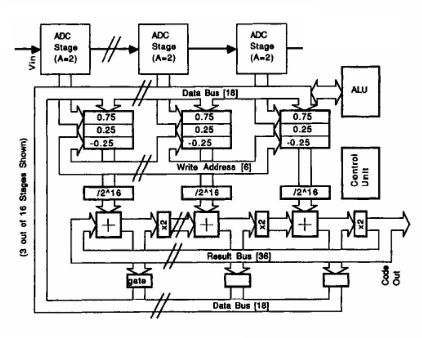
- $\varepsilon_{DAC}(0)$ equivalent to amp. offset → ignore

DAC Calibration – Step 2…2^{B1}



- Stepping through DAC codes $1 \ldots 2^{(B1-1)}$ yields all incremental correction values
- Measurements repeated and averages to account for variance associated with noise

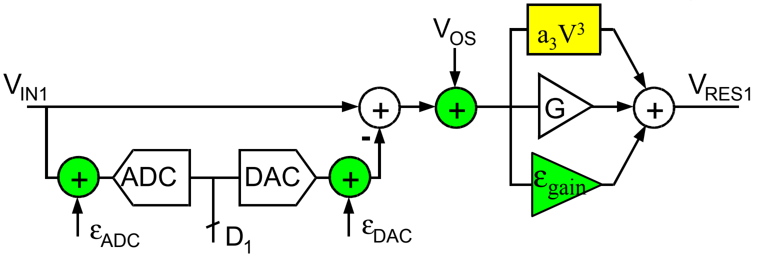
Pipeline ADC
Example: Calibration Hardware



- Above block diagram may seem extensive however, in current fine-line CMOS technologies digital portion of a pipeline ADCs consume insignificant power and area compared to the analog sections

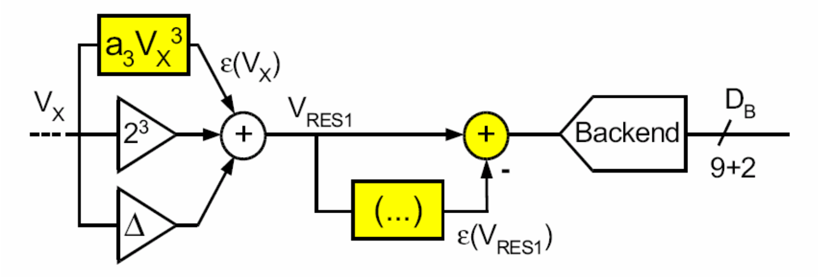
Ref: E. G. Soenen et al., "An architecture and an algorithm for fully digital correction of monolithic pipelined ADCs," TCAS II, pp. 143-153, March 1995

Pipelined ADC
Error Correction/Calibration Summary



Error	Correction/Calibration
ε_{ADC}, V_{os}	Redundancy either same stage or next stage
ε_{gain}	Digital adjustment
ε_{DAC}	Either sufficient component matching or digital calibration
Inter-stage amplifier non-linearity	?

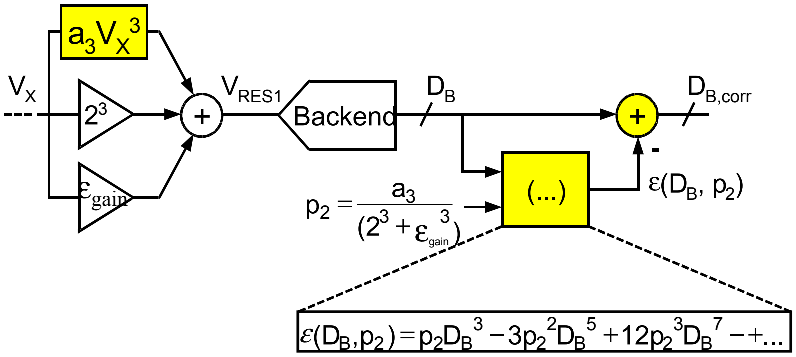
Inter-stage Gain Nonlinearity



- Invert gain stage non-linear polynomial
- Express error as function of V_{RES1}
- Push error into digital domain through backend

Ref: B. Murmann and B. E. Boser, "A 12-b, 75MS/s Pipelined ADC using Open-Loop Residue Amplification," *ISSCC Dig. Techn. Papers*, pp. 328-329, 2003

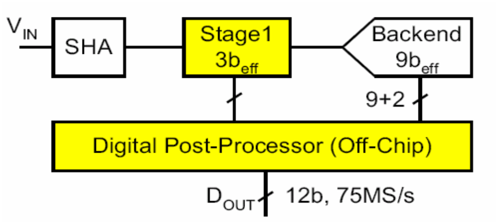
Inter-stage Gain Nonlinearity



- Pre-computed table look-up
- p_2 continuously estimated & updated (account for temp. & other variations)

Ref: B. Murmann and B. E. Boser, "A 12-b, 75MS/s Pipelined ADC using Open-Loop Residue Amplification," *ISSCC Dig. Techn. Papers*, pp. 328-329, 2003

Inter-stage Gain Nonlinearity Compensation Proof of Concept Evaluation Prototype

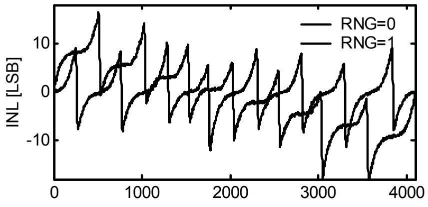


- Re-used 14-bit ADC in 0.35μm from Analog Devices [Kelly, ISSCC 2001]
- Modified only 1st stage with 3-b_{eff} → open-loop amplifier built with simple diff-pair + resistive load instead of the conventional feedback around high-gain amp
- Conventional 9-b_{eff} backend, 2-bit redundancy in 1st stage
- Real-time post-processor off-chip (FPGA)

Ref: B. Murmann and B. E. Boser, "A 12-b, 75MS/s Pipelined ADC using Open-Loop Residue Amplification," *ISSCC Dig. Techn. Papers*, pp. 328-329, 2003

Measurement Results 12-bit ADC w Extra 2-bits for Calibration

(a) without calibration



(b) with calibration