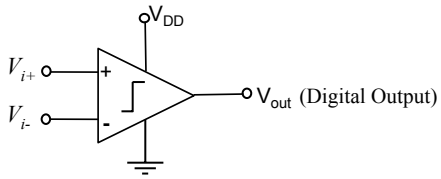
EE247
Lecture 20

ADC Converters

Comparator design

- Single-stage open-loop amplifier
- Cascade of open-loop amplifiers
- Problem associated with DC offset
  - Cascaded output series cancellation
  - Input series cancellation
  - Offset cancellation through additional input pair plus offset storage capacitors
- Latched comparators
- Comparator examples

Voltage Comparators



Play an important role in majority of ADCs

Function: Compare the instantaneous value of two analog signals & generate a digital output voltage based on the sign of the difference:

$$\text{If } V_{i+} - V_{i-} > 0 \rightarrow V_{out} = \text{“1”}$$
$$\text{If } V_{i+} - V_{i-} < 0 \rightarrow V_{out} = \text{“0”}$$

Voltage Comparator Architectures

Comparator architectures:

- High gain amplifier with differential analog input & single-ended large swing output
  - Output swing has to be compatible with driving digital logic circuits
  - Open-loop amplification→ no frequency compensation required
  - Precise gain not required
- Latched comparators; in response to a strobe (clock edge), input stage disabled & digital output stored in a latch till next strobe
  - Two options for implementation :
    - Latch-only comparator
    - Low-gain preamplifier + high-sensitivity latch
- Sampled-data comparators
  - T/H input
  - Offset cancellation

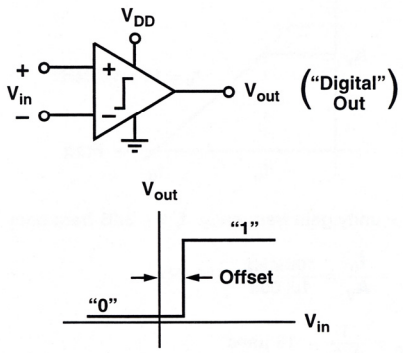
Comparator Built with High-Gain Amplifier

Amplify V_{in}(min) to V_{DD}
→ V_{in}(min) determined by ADC resolution

Example: 12-bit ADC with:
- V_{FS}= 1.5V→ 1LSB=0.36mV
- V_{DD}=1.8V

→ For 1.8V output & 0.5LSB precision:

$$A_v^{Min} = \frac{1.8V}{0.18mV} \approx 10{,}000$$



Comparators
1-Single-Stage Amplification

- Amplifier maximum Gain-Bandwidth product (f_u) for a given technology, typically a function of maximum device f_t

$f_u = unity\text{-}gain\ frequency,\ f_o = -3dB\ frequency \qquad f_o = \frac{f_u}{A_V}$

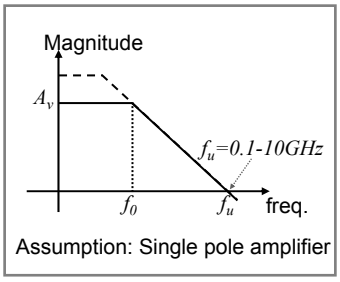
$Example: f_u = 10GHz \quad \& \quad A_V = 10{,}000$

$$f_o = \frac{10GHz}{10{,}000} \approx 1MHz$$

$$\tau_{settling} = \frac{1}{2\pi f_o} = 0.16\mu sec$$

$Allow\ a\ few\ \tau\ for\ output\ to\ settle$

$$f_{Clock}^{Max.} \rightarrow \frac{1}{5\tau_{settling}} \approx 1.26MHz$$

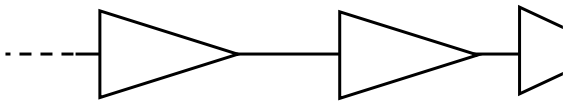


Assumption: Single pole amplifier

Too slow for majority of applications!

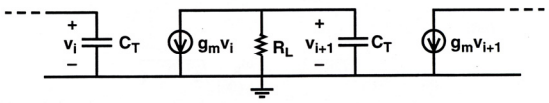
→ Try cascade of lower gain stages to broaden frequency of operation

Comparators
2- Cascade of Open Loop Amplifiers



The stages identical → small-signal model for the cascades:

One stage:



$|A_V(0)| = g_m R_L$

ω_o = – 3dB frequency = $\frac{1}{R_L C_T}$

ω_u = – unity gain frequency = G×BW = $\frac{g_m}{C_T}$

$\therefore \omega_o = \frac{\omega_u}{|A_V(0)|}$

Open Loop Cascade of Amplifiers

For an N-stage cascade:

$$A_T(j\omega) = [A_V(j\omega)]^N = \frac{[A_V(0)]^N}{\left(1+j\frac{\omega}{\omega_0}\right)^N}$$

Define

$\omega_{oN} \equiv$ **–3dB frequency of the N-stage cascade**

Then

$$|A_T(j\omega_{oN})| = \frac{|A_V(0)|^N}{\sqrt{2}}$$

and

$$\omega_{oN} = \omega_o\sqrt{2^{1/N}-1} = \frac{\omega_u}{|A_V(0)|}\sqrt{2^{1/N}-1}$$

$\therefore$ **For a specified $|A_T(0)|$**

$$|A_V(0)| = |A_T(0)|^{1/N}$$

$$\Rightarrow \omega_{oN} = \frac{\omega_u}{|A_T(0)|^{1/N}}\sqrt{2^{1/N}-1}$$

Thus,

$$\frac{\omega_{oN}}{\omega_{o1}} = \left[\frac{\omega_u}{|A_T(0)|^{1/N}}\sqrt{2^{1/N}-1}\right] \Big/ \left[\frac{\omega_u}{|A_T(0)|}\right]$$

$$= |A_T(0)|^{\left(\frac{N-1}{N}\right)}\sqrt{2^{1/N}-1}$$

Example: N=4, A_T=10000→ $\omega_{oN}=430\omega_{o1}$

Open Loop Cascade of Amplifiers

For $|A_T(DC)|$=10,000

N	ω_{oN}/ω_{o1}	$\|A_V(0)\|$
1	1	10,000
2	64	100
3	236	21.5
4	435	10
5	611	6.3
10	1067	2.5
20	1185	1.6

Example:

$N=3,\ f_u=10GHz\ \&\ |A_T(0)|=10000$

$$f_{oN} = \frac{10GHz}{(10{,}000)^{1/3}}\sqrt{2^{1/3-1}} \approx 237MHz$$

$$\tau_{settling} = \frac{1}{2\pi f_o} = 0.7nsec$$

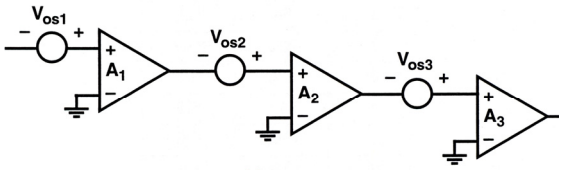
Allow a few τ for output to settle

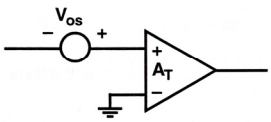
$$f_{Clock}^{Max} \rightarrow \frac{1}{5\tau_{settling}} \approx 290MHz$$

f_{max} improved from *1.26MHz to 290MHz* → *X236*

Open Loop Cascade of Amplifiers Offset Voltage

- **From offset point of view: high gain/stage is preferred**
- **Choice of # of stage**
  →bandwidth vs offset tradeoff



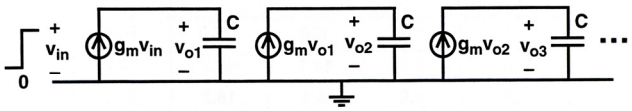


$$A_T = A_1 \cdot A_2 \cdot A_3$$

Input-referred offset $\rightarrow V_{os} = V_{os1} + \frac{V_{os2}}{A_1} + \frac{V_{os3}}{A_1 \cdot A_2}$

Open Loop Cascade of Amplifiers Step Response

- **Assuming linear behavior (not slew limited)**



$$v_{o1} = \frac{1}{C}\int_0^t g_m v_{in} dt = \frac{g_m}{C} v_{in} t$$

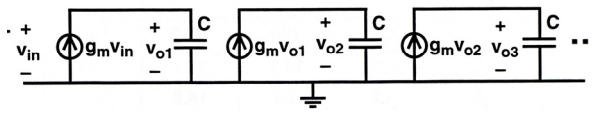
$$v_{o2} = \frac{1}{C}\int_0^t g_m v_{o1} dt = \frac{g_m}{C}\int_0^t \frac{g_m}{C} v_{in} t\, dt = \frac{1}{2}\left(\frac{g_m}{C}\right)^2 v_{in} t^2$$

$$v_{o3} = \frac{1}{C}\int_0^t g_m v_{o2} dt = \frac{g_m}{C}\int_0^t \left[\frac{1}{2}\left(\frac{g_m}{C}\right)^2 v_{in} t^2\right] dt$$

$$= \frac{1}{3}\left(\frac{1}{2}\right)\left(\frac{g_m}{C}\right)^3 v_{in} t^3$$

Open Loop Cascade of Amplifiers Step Response

•**Assuming linear behavior**



N Stages

$$v_{oN} = \left(\frac{g_m}{C}\right)^N \left(\frac{t^N}{N!}\right) v_{in}$$

For the output to reach a specified v_{out} (i.e., $v_{oN} = v_{out}$) the delay is

$$\tau_D = \left(\frac{C}{g_m}\right)\left[(N!)\left(\frac{v_{out}}{v_{in}}\right)\right]^{1/N}$$

Open Loop Cascade of Amplifiers Delay/(C/g_m)

$$\tau_D = \left(\frac{C}{g_m}\right)\left[(N!)\left(\frac{V_{out}}{V_{in}}\right)\right]^{1/N}$$

- **Minimum total delay broad function of N**
- **Relationship between # of stages resulting in minimize delay (N_{op}) and gain (V_{out}/V_{in}) approximately:**

$$N_{opt} \approx 1 + \log_2 A_T \quad for\ A < 1000$$

$$N_{opt} \approx 1.2 \ln A_T \quad for\ A \geq 1000$$

Delay/(C/g_m)

N \ v_{out}/v_{in}	10	100	1000	10K
1	10	100	1000	10K
2	4.5	14.1	44.7	141
3	3.9	8.4	18.2	39.1
4	3.9	7.0	12.4	22.1
5	4.1	6.5	10.4	16.4
6	4.4	6.4	9.5	13.9
7	4.7	6.5	9.1	12.6
8	5.0	6.7	8.9	11.9
9	5.4	6.9	8.9	11.5
10	5.7	7.2	9.0	11.4
11	6.1	7.5	9.2	11.3
12	6.4	7.8	9.4	11.4
20	9.3	10.5	11.7	13.2

Ref: J.T. Wu, et al., "A 100-MHz pipelined CMOS comparator " *IEEE Journal of Solid-State Circuits,* vol. 23, pp. 1379 - 1385, December 1988.

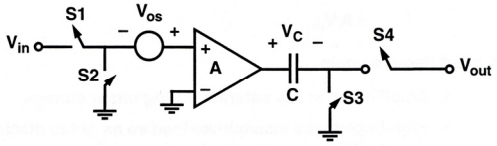
Offset Cancellation

- **In sampled-data cascade of amplifiers Vos can be cancelled**
  → Store on ac-coupling caps in series with amp stages
- **Offset associated with a specific amp can be cancelled by storing it in series with either the input or the output of that stage**
- **Offset can be cancelled by adding a pair of auxiliary inputs to the amplifier and storing the offset on capacitors connected to the aux. inputs during offset cancellation phase**

Ref: J.T. Wu, et al., "A 100-MHz pipelined CMOS comparator " *IEEE Journal of Solid-State Circuits,* vol. 23, pp. 1379 - 1385, December 1988.

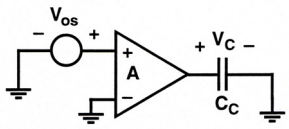
Offset Cancellation
Output Series Cancellation

- **Amp modeled as ideal + V_{os} (input referred)**



1- Store offset:

- **S1, S4→ open**
- **S2, S3→ closed**
  → V_C=AxV_{OS}



$V_C = A \cdot V_{os}$

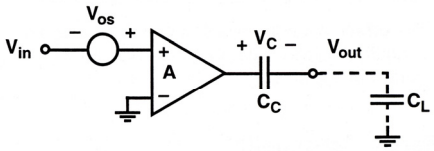
Ref: J.T. Wu, et al., "A 100-MHz pipelined CMOS comparator " *IEEE Journal of Solid-State Circuits,* vol. 23, pp. 1379 - 1385, December 1988.

Offset Cancellation
Output Series Cancellation

2- Amplify:

- **S2, S3→ open**
- **S1, S4→ closed**

  →V_C=AxV_{OS}

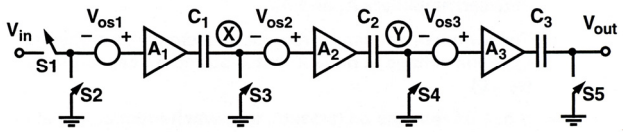


Circuit requirements:

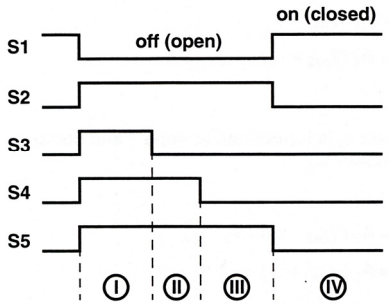
- **Amp not saturate during offset storage**
- **High-impedance (C) load → C_c not discharged**
- **C_c >> C_L to avoid attenuation**
- **C_c >> C_{switch} avoid excessive offset due to charge injection**

$$V_{out} = A\cdot(V_{in} + V_{os}) - V_C$$
$$= A\cdot(V_{in} + V_{os}) - A\cdot V_{os}$$
$$= A\cdot V_{in}$$

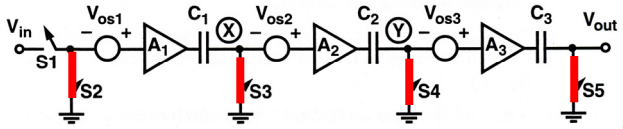
Offset Cancellation
Cascaded Output Series Cancellation



Note: Offset storage capacitors in series with the amplifier outputs



Offset Cancellation
Cascaded Output Series Cancellation

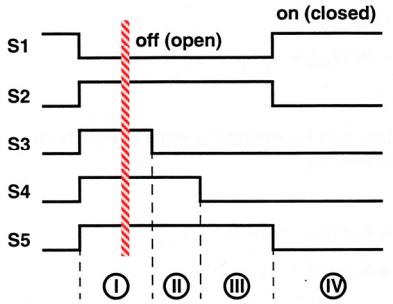


1- S1→ open, S2,3,4,5 closed

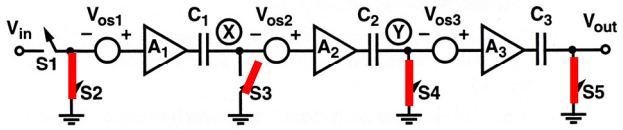
$V_{C1}=A_1xV_{os1}$

$V_{C2}=A_2xV_{os2}$

$V_{C3}=A_1xV_{os3}$



Offset Cancellation
Cascaded Output Series Cancellation



2- S3→ open first

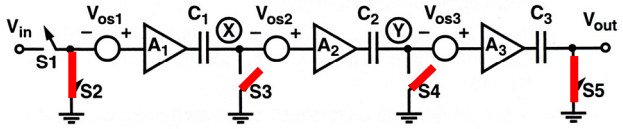
- Feedthrough from S3 → offset on X
- Switch offset , ε_3 induced on node X
- Since S4 remains closed, offset associated with ε_3 → stored on C2

$V_X=\varepsilon_3$

$V_{C1}=A_1xV_{os1}-\varepsilon_3$

$V_{C2}=A_2x(V_{os2}+\varepsilon_3)$

Offset Cancellation
Cascaded Output Series Cancellation



3- S4→ open

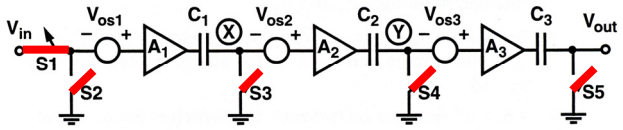
- Feedthrough from S4 → offset on Y
- Switch offset , ε_4 induces error on node Y
- Since S5 remains closed, offset associated with ε_4 → stored on C3

$$V_Y = \varepsilon_4$$

$$V_{C2} = A_2 x (V_{os2} + \varepsilon_3) - \varepsilon_4$$

$$V_{C3} = A_3 x (V_{os3} + \varepsilon_4)$$

Offset Cancellation
Cascaded Output Series Cancellation



4- S2→ open, S5→ open , S1→ closed

- S2 open & S1 closed → since input connected to low impedance source charge injection not of major concern
- Switch offset , ε_5 introduced due to S5 opening

$$V_X = A_1 x (V_{in} + V_{os1}) - V_{C1}$$

$$= A_1 x (V_{in} + V_{os1}) - (A_1 . V_{os1} - \varepsilon_3)$$

$$= A_1 . V_{in} + \varepsilon_3$$

Offset Cancellation
Cascaded Output Series Cancellation

$$V_y = A_2x(V_x+V_{os2}) - V_{C2}$$
$$= A_2x(A_1V_{in} + \varepsilon_3 + V_{os2}) - [A_2.(V_{os2}+\varepsilon_3) - \varepsilon_4]$$
$$= A_1.A_2.V_{in} + \varepsilon_4$$

$$V_{out} = A_3x(V_y+V_{os3}) - V_{C3}$$
$$= A_3.(A_2xA_1V_{in} + \varepsilon_4 + V_{os3}) - [A_3.(V_{os3}+\varepsilon_4) - \varepsilon_5]$$
$$= A_1.A_2.A_3.V_{in} + \varepsilon_5$$

Offset Cancellation
Cascaded Output Series Cancellation

$$V_{out} = A_1.A_2.A_3.(V_{in} + \varepsilon_5/A_1.A_2.A_3)$$
Input-Referred Offset = $\varepsilon_5/A_1.A_2.A_3$

Example:
3-stage open-loop differential amplifier with series offset cancellation + output amplifier (see Ref.)

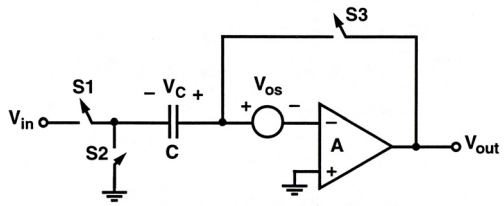
$A_{Total}(DC) = 2x10^6 = 126dB$
Input-referred offset < $5\mu V$

Ref: :R. Poujois and J. Borel, "A low drift fully integrated MOSFET operational amplifier," *IEEE Journal of Solid-State Circuits,* vol. 13, pp. 499 - 503, August 1978.

Offset Cancellation
Output Series Cancellation

- Advantages:
  - Almost compete cancellation
  - Closed-loop stability not required
- Disadvantages:
  - Gain per stage must be small
  - Offset storage C in the signal path → could slow down overall performance

Offset Cancellation
Input Series Cancellation

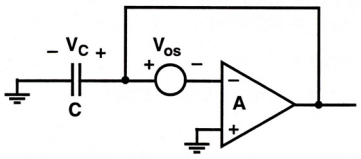


Ref: :R. Poujois and J. Borel, "A low drift fully integrated MOSFET operational amplifier," *IEEE Journal of Solid-State Circuits,* vol. 13, pp. 499 - 503, August 1978.

Offset Cancellation
Input Series Cancellation

1- Store offset

S1 = 0 (off)
S2, S3 = 1 (conducting)



Note: Mandates closed-loop stability

$$V_C = -A(V_C - V_{os})$$

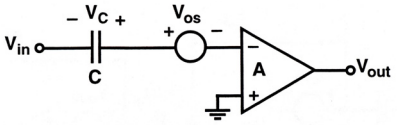
$$= \left(\frac{A}{A+1}\right)V_{os}$$

Ref: :R. Poujois and J. Borel, "A low drift fully integrated MOSFET operational amplifier," *IEEE Journal of Solid-State Circuits,* vol. 13, pp. 499 - 503, August 1978.

Offset Cancellation
Input Series Cancellation

2- Amplify

S2, S3 → open
S1→ closed



$$V_{out} = -A(V_{in} + V_C - V_{os}) = -A\left[V_{in} + V_{os}\left(\frac{A}{A+1} - 1\right)\right]$$

$$\therefore\ V_{out} = -A\left(V_{in} - \frac{V_{os}}{A+1}\right)$$

and

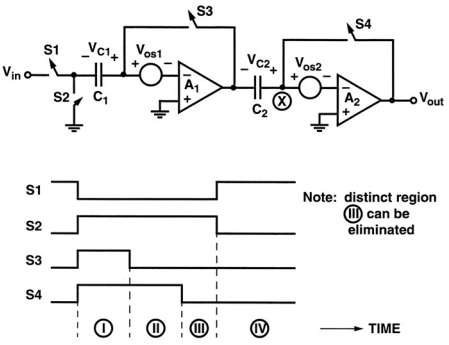
$$\textbf{Input-Referred Offset} = \frac{V_{os}}{A+1}$$

Example: A=4
→Input-referred offset =V_{os}/5

Offset Cancellation
Cascaded Input Series Cancellation

$$V_{out} = A_1 A_2\left[V_{in} + \frac{V_{os2}}{A_1(A_2+1)} - \frac{\varepsilon_2}{A_1}\right]$$

$$\text{Input-Referred Offset} = \frac{V_{os2}}{A_1(A_2+1)} - \frac{\varepsilon_2}{A_1}$$



ε_2 →charge injection associated with opening of S4

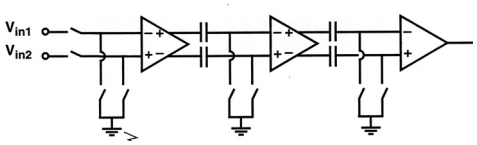
Offset Cancellation
Input Series Cancellation

- Advantages:
  - In applications such as C-array successive approximation ADCs can use C-array to store offset
- Disadvantages:
  - Cancellation not complete
  - Requires closed loop stability
  - Offset storage C in the signal path- could slow down overall performance

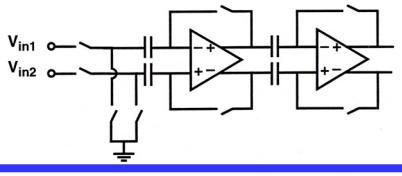
CMOS Comparators
Cascade of Gain Stages

Fully differential gain stages → 1st order cancellation of switch feedthrough offset

1- Output series offset cancellation

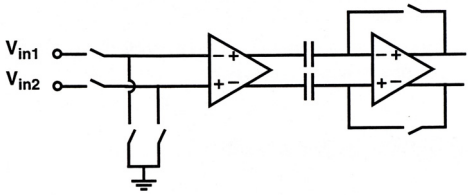


2- Input series offset cancellation



CMOS Comparators
Cascade of Gain Stages

3-Combined input & output series offset cancellation

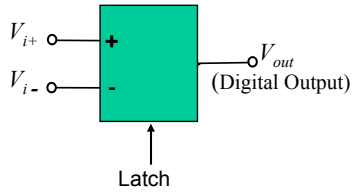


V_{os1} & V_{os2} are both stored on a single pair of coupling capacitors

Offset Cancellation

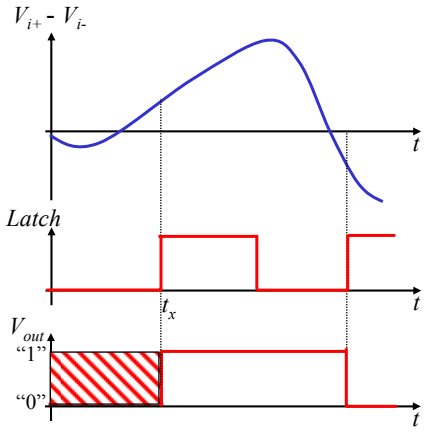
- Cancel offset by additional pair of inputs + offset storage Cs + an extra clock phase for offset storage (Lecture 18 slide 46 -48)

Latched Comparators



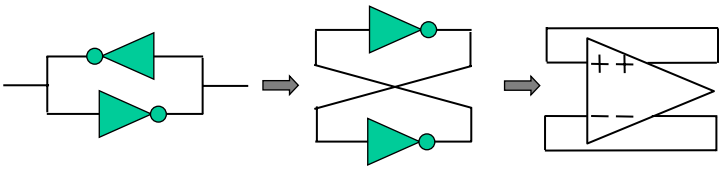
Compares two input voltages at time t_x & generates a digital output:

If $V_{i+} - V_{i-} > 0 \rightarrow V_{out}$="1"
If $V_{i+} - V_{i-} < 0 \rightarrow V_{out}$="0"



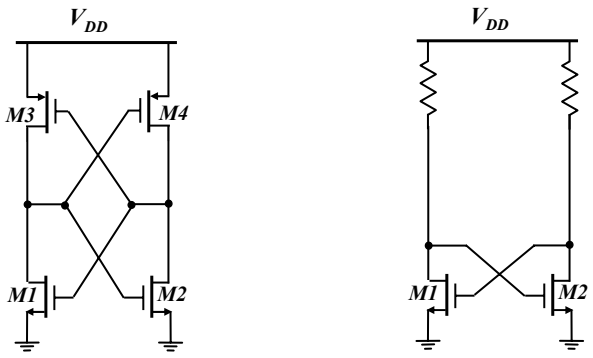
CMOS Latched Comparators

Comparator amplification need not be linear
→ can use a latch → regeneration



Latch→ Amplification + positive feedback

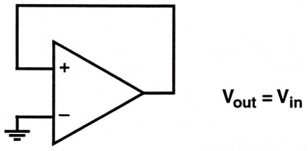
Simplest Form of CMOS Latch



CMOS Latched Comparators
Small Signal Model

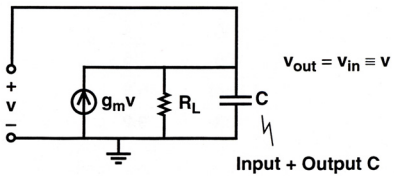
Latch can be modeled as a:

→ Single-pole amp + positive feedback



$V_{out} = V_{in}$

Small signal ac half circuit



CMOS Latched Comparator
Latch Delay

$$g_m V = \frac{V}{R_L} + C\frac{dV}{dt}$$

$$\frac{g_m}{C}\left(1 - \frac{1}{g_m R_L}\right)V = \frac{dV}{dt} \qquad \frac{g_m}{C}\left(1 - \frac{1}{g_m R_L}\right)dt = \frac{dV}{V}$$

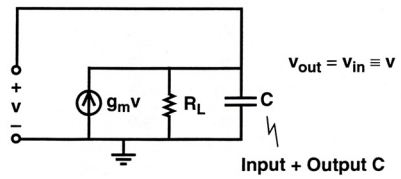
Integrating both sides: $\frac{g_m}{C}\left(1 - \frac{1}{g_m R_L}\right)\int_{t1}^{t2} dt = \int_{V1}^{V2}\frac{1}{V}dV$ $\qquad \left(\int_b^a \frac{1}{x}dx = \ln x\Big|_b^a = \ln a - \ln b = \ln\frac{a}{b}\right)$

Latch Delay:

$$t_D = t_2 - t_1 = \frac{C}{g_m}\left(\frac{1}{1 - \frac{1}{g_m R_L}}\right)\ln\left(\frac{V_2}{V_1}\right)$$

For $g_m R_L >> 1$

$$t_D \approx \frac{C}{g_m}\ln\left(\frac{V_2}{V_1}\right)$$



CMOS Latched Comparators

$$t_D \approx \frac{C}{g_m}\ln\left(\frac{V_2}{V_1}\right)$$

$$\frac{V_2}{V_1} \rightarrow Latch\ Gain = A_L$$

$$\rightarrow t_D \approx \frac{C}{g_m}\ln A_L$$

Normalized Latch Delay

τ_D(3-stage amp)= $18.2(C/g_m)$

A_L	$\frac{t_D}{C/g_m}$
10	2.3
100	4.6
1000	6.9
10K	9.2

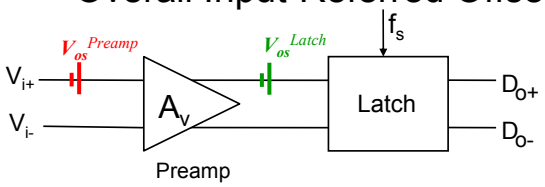
Compared to a 3-stage open-loop cascade of amps for equal overall gain of 1000

→Latch faster by about x3

Latch-Only Comparator

- Much faster compared to cascade of open-loop amplifiers
- Main problem associated with latch-only comparator topology:
  - High input-referred offset voltage (as high as 100mV!)
    - Solution:
      - Use preamplifier to amplify the signal and reduce overall input-referred offset

Pre-Amplifier + Latch
Overall Input-Referred Offset



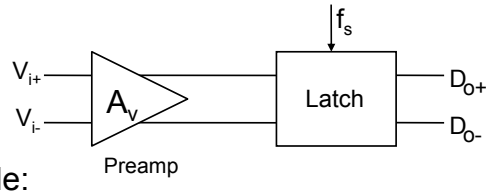
Latch offset attenuated by preamp gain when referred to preamp input.
Assuming the two offset sources are uncorrelated:

$$\sigma_{Input-Referred\_Offset} = \sqrt{\sigma^2_{Vos\_Preamp} + \frac{1}{A^2_{Preamp}}\sigma^2_{Vos\_Latch}}$$

$$Example: \ \sigma_{Vos\_Preamp} = 4mV \ \ \& \ \ \sigma_{Vos\_Latch} = 50mV \ \ \& \ \ A_{Preamp} = 10$$

$$\sigma_{Input-Referred\_Offset} = \sqrt{4^2 + \frac{1}{10^2}50^2} = 6.4mV$$

Pre-Amplifier Tradeoffs



- Example:
  - Latch offset 50 to 100mV
  - Preamp DC gain 10X
  - Preamp input-referred latch offset 50 to 100mV
  - Input-referred preamplifier offset 2 to 10mV
  - Overall input-referred offset 5.5 to 14mV

→ Addition of preamp reduces the latch input-referred offset reduced by ~7 to 9X → ~allows extra 3-bit resolution for ADC!

Comparator Preamplifier Gain-Speed Tradeoffs

• Amplifier maximum Gain-Bandwidth product (f_u)for a given technology, typically a function of maximum device f_t

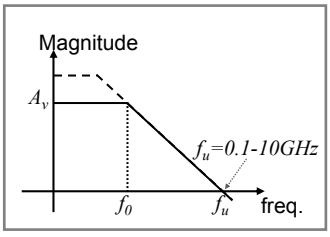
f_u =unity gain frequency, f_0 $= -3dB$ frequency & τ_0 = settling time

$$f_0 = \frac{f_u}{A_{preamp}}$$

For example assuming preamp has a gain of 10:

$$f_0 = \frac{f_u}{A_{preamp}} = \frac{1GHz}{10} = 100MHz$$

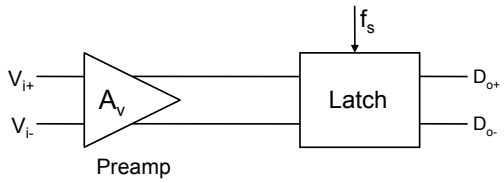
$$\tau_0 = \frac{1}{2\pi f_0} = \frac{A_{preamp}}{2\pi f_u} = 1.6n\sec$$



- Tradeoff:
  - To reduce the effect of latch offset → high preamp gain desirable
  - Fast comparator → low preamp gain

  → Choice of preamp gain: compromise speed v.s. input-referred latch offset

Latched Comparator

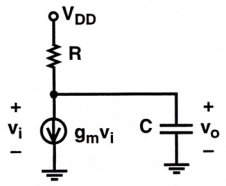


Important features:

– Maximum clock rate f_s → settling time, slew rate, small signal bandwidth
– Resolution→ gain, offset
– Overdrive recovery
– Input capacitance (and linearity of input capacitance!)
– Power dissipation
– Input common-mode range and CMR
– Kickback noise
– …

Comparator Overdrive Recovery

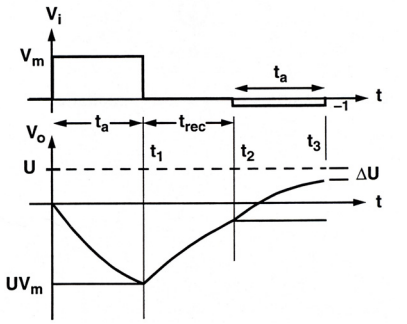
Linear model for a single-pole amplifier:



U→ amplification after time t_a

During reset amplifier settles exponentially to its zero input condition with τ_0=RC

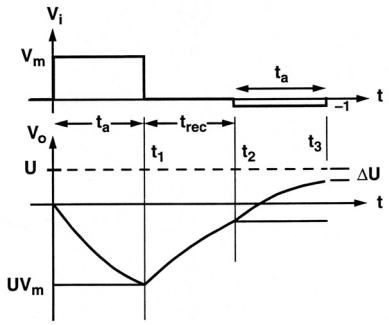
Assume Vm → maximum input normalized to 1/2lsb (=1)



Example: Worst case input/output waveforms

Previous input → max. possible e.g. VFS
Current input → min. input-referred signal (0.5LSB)

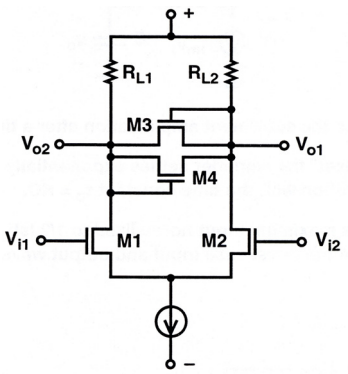
Comparators Overdrive Recovery



Example: Worst case input/output waveforms

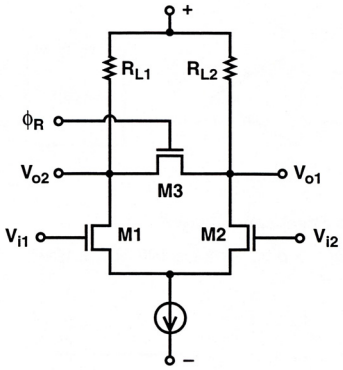
- If recovery time is not long enough to allow output to discharge (recover) from previous state- then it may not be able to resolve the current input → error
- To minimize this effect:
  1. Passive clamp
  2. Active restore
  3. Low gain/stage

Comparators Overdrive Recovery
Limiting Output Voltage



Clamp

Adds parasitic capacitance



Active Restore

After outputs are latched by following stage

→ Activate ϕ_R & equalize output nodes

CMOS Preamplifier + Latched Comparator
Delay in Response

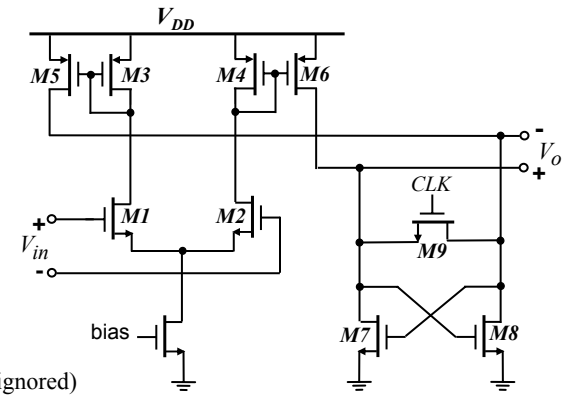
Latch delay previously found:

$$\tau_D \approx \frac{C}{g_m}\ln\left(\frac{V_2}{V_1}\right)$$

Assuming gain of A_v for the preamplifier then : $V_1 = A_v \times V_{in}$

$$\tau_D \approx \frac{C}{g_m}\ln\left(\frac{V_0}{A_v V_{in}}\right)$$

Latched Comparator Including Preamplifier Example



Preamplifier gain:

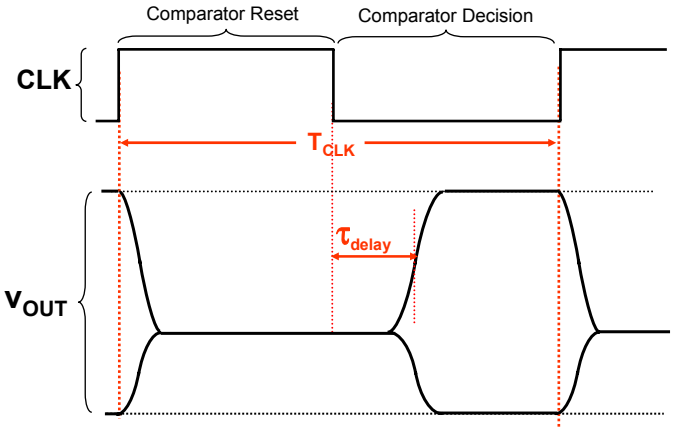
$$A_v = \frac{g_m^{M1}}{g_m^{M3}} = \frac{\left(V_{GS}^{M3} - V_{th}^{M3}\right)}{\left(V_{GS}^{M1} - V_{th}^{M1}\right)}$$

Comparator delay:

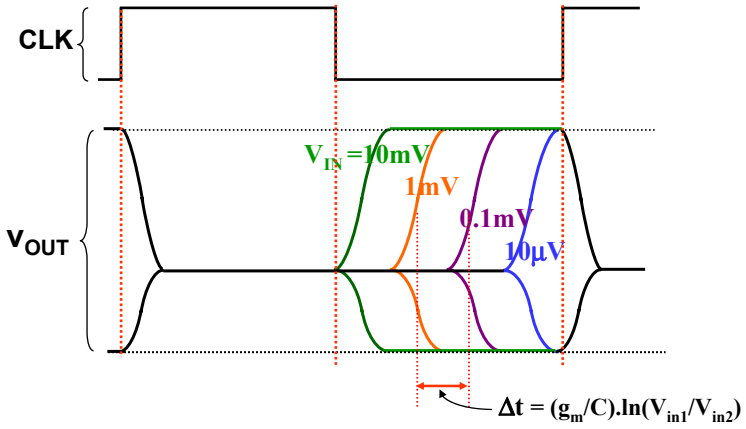
(for simplicity, preamp delay ignored)

$$\tau_D \approx \frac{C}{g_m} \ln\left(\frac{V_0}{A_v Vin}\right)$$

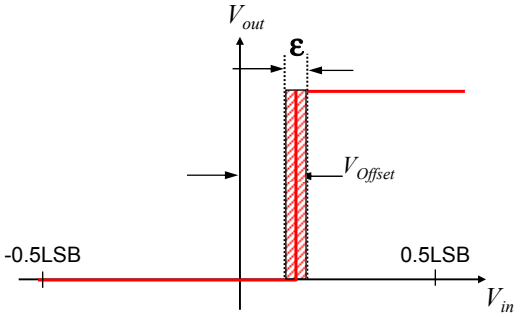
Comparator Dynamic Behavior



Comparator Resolution



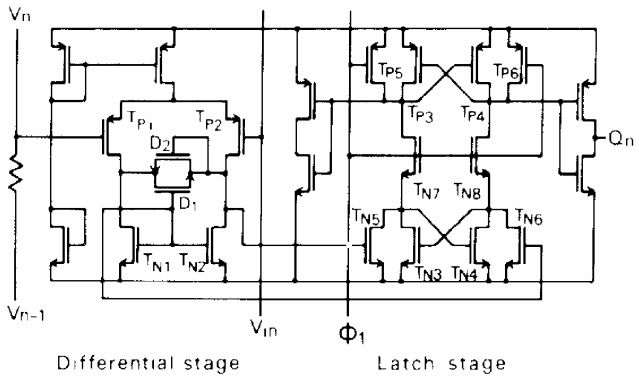
Comparator Voltage Transfer Function Non-Idealities



V_{Offset} → Comparator offset voltage

ε → Meta-Stable region (output ambiguous)

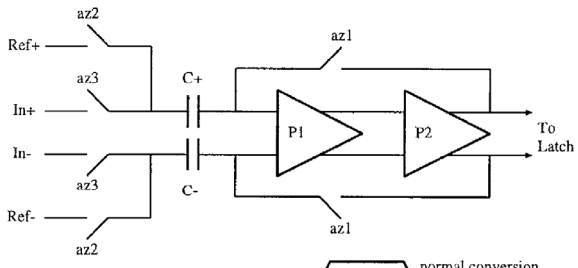
CMOS Comparator Example



- Flash ADC: 8bits, +-1/2LSB INL @ fs=15MHz (Vref=3.8V, LSB~15mV)
- No offset cancellation

Ref: A. Yukawa, "A CMOS 8-Bit High-Speed A/D Converter IC," JSSC June 1985, pp. 775-9

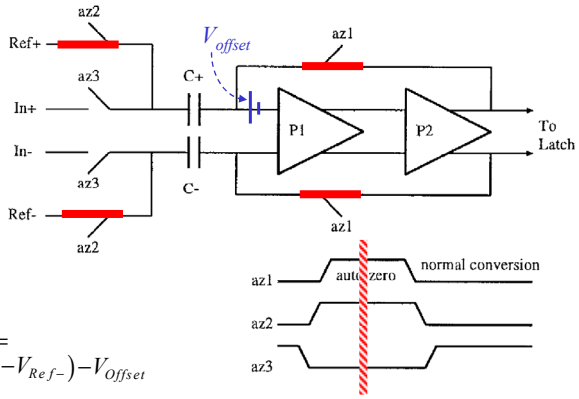
Comparator with Auto-Zero



Note:
Reference & input
both differential

Ref: I. Mehr and L. Singer, "A 500-Msample/s, 6-Bit Nyquist-Rate ADC for Disk-Drive Read-Channel Applications," JSSC July 1999, pp. 912-20.

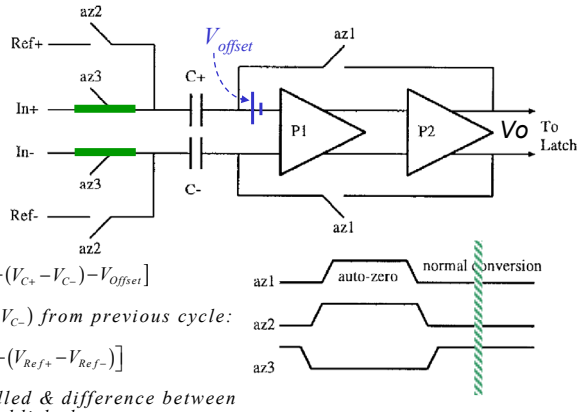
Flash ADC
Comparator with Auto-Zero



$$V_{C+} - V_{C-} = (V_{Ref+} - V_{Ref-}) - V_{Offset}$$

Ref: I. Mehr and D. Dalton, "A 500-Msample/s, 6-Bit Nyquist-Rate ADC for Disk-Drive Read-Channel Applications," JSSC July 1999, pp. 912-20.

Flash ADC
Comparator with Auto-Zero



$$V_o = A_{P1} * A_{P2}\left[(V_{In+} - V_{In-}) - (V_{C+} - V_{C-}) - V_{Offset}\right]$$

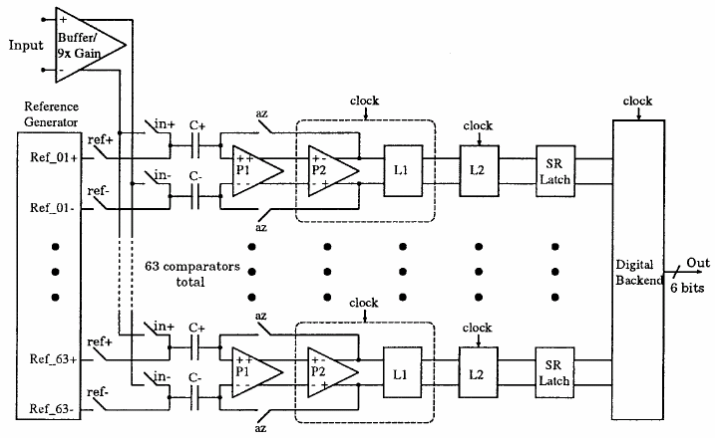
Substituting for $(V_{C+} - V_{C-})$ *from previous cycle:*

$$V_o = A_{P1} * A_{P2}\left[(V_{In+} - V_{In-}) - (V_{Ref+} - V_{Ref-})\right]$$

Note: Offset is cancelled & difference between input & reference established

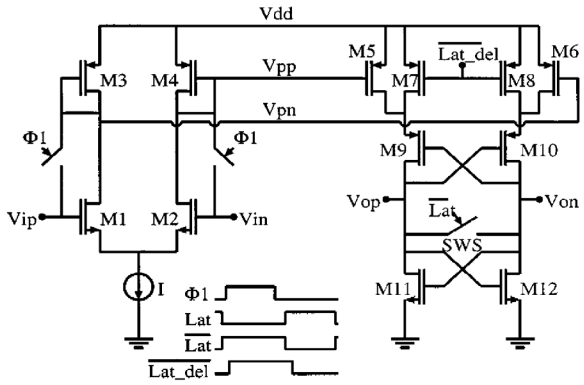
Ref: I. Mehr and D. Dalton, "A 500-Msample/s, 6-Bit Nyquist-Rate ADC for Disk-Drive Read-Channel Applications," JSSC July 1999, pp. 912-20.

Flash ADC
Using Comparator with Auto-Zero



Ref: I. Mehr and D. Dalton, "A 500-Msample/s, 6-Bit Nyquist-Rate ADC for Disk-Drive Read-Channel Applications," JSSC July 1999, pp. 912-20.

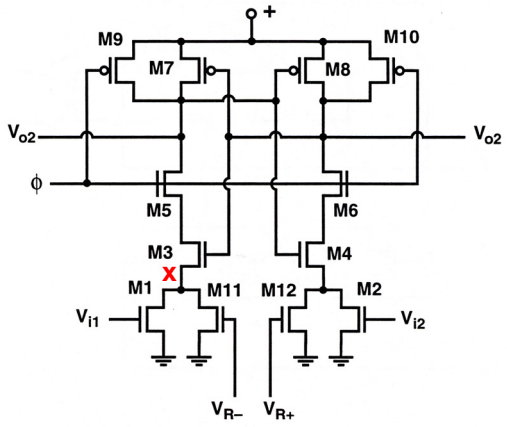
Auto-Zero Implementation



Ref:I. Mehr and L. Singer, "A 55-mW, 10-bit, 40-Msample/s Nyquist-Rate CMOS ADC," JSSC March 2000, pp. 318-25

Comparator Example

- Variation on Yukawa latch used w/o preamp
- Good for low resolution ADCs (in this case 1.5bit/stage for a pipeline)
- Note: M1, M2, M11, M12 operate in triode mode
- M11 & M12 added to vary comparator threshold
- Conductance at node X is sum of G_{M1} & G_{M11}



Ref: T. B. Cho and P. R. Gray, "A 10 b, 20 Msample/s, 35 mW pipeline A/D converter," *IEEE Journal of Solid-State Circuits,* vol. 30, pp. 166 - 172, March 1995

Comparator Example (continued)

- M1, M2, M11, M12 operate in triode mode with all having equal L
- Conductance of input devices:

$$G_1 = \frac{\mu C_{ox}}{L} \times \left[W_1 (V_{I1} - V_{th}) + W_{11} (V_{R-} - V_{th}) \right]$$

$$G_2 = \frac{\mu C_{ox}}{L} \times \left[W_1 (V_{I2} - V_{th}) + W_{11} (V_{R+} - V_{th}) \right]$$

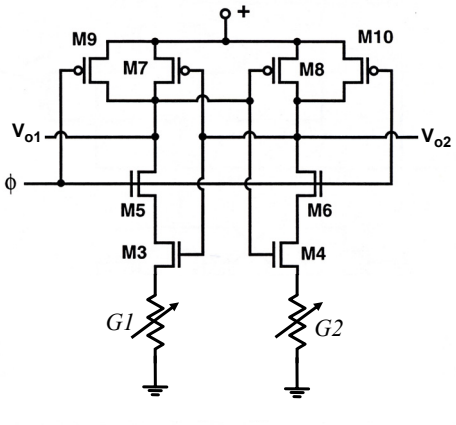
$$\rightarrow \Delta G = \frac{\mu C_{ox} W_1}{L} \times \left[(V_{I1} - V_{I2}) - \frac{W_{11}}{W_1} (V_{R+} - V_{R-}) \right]$$

- To 1st order, for $W1 = W2$ & $W11 = W12$

  $V_{th}^{latch} = W11/W1 \times V_R$

  where $V_R = V_{R+} - V_{R-}$

  → V_R fixed $W11, 12$ varied from comparator to comparator → Eliminates need for resistive divider



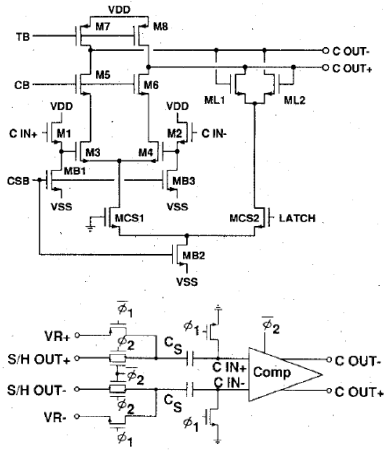
Ref: T. B. Cho and P. R. Gray, "A 10 b, 20 Msample/s, 35 mW pipeline A/D converter," *IEEE Journal of Solid-State Circuits,* vol. 30, pp. 166 - 172, March 1995

Comparator Example

- Used in a pipelined ADC with digital correction
  →no offset cancellation required

Differential reference & input

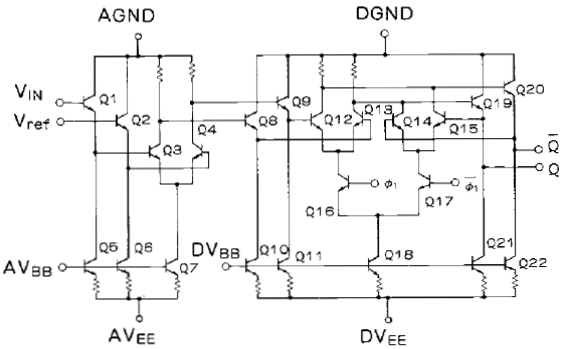
- M7, M8 operate in triode region
- Preamp gain ~10
- Input buffers suppress kick-back
- ϕ_1 high → C_s charged to VR & ϕ_{2B} is also high → current diverted to latch→ comparator output in hold mode
- ϕ_2 high→ C_s connected to S/Hout & comparator input (VR-S/Hout), current sent to preamp → comparator in amplify mode



Ref: S. Lewis, et al., "A Pipelined 5-Msample/s 9-bit Analog-to-Digital Converter" IEEE JSSC ,NO. 6, Dec. 1987

Bipolar Comparator Example

- Used in 8bit 400Ms/s & 6bit 2Gb/s flash ADC
- Signal amplification during ϕ1 high, latch operates when ϕ1 low
- Input buffers suppress kick-back & input current
- Separate ground and supply buses for front-end preamp → kick-back noise reduction



Ref: Y. Akazawa, et al., "A 400MSPS 8b flash AD conversion LSI," *IEEE International Solid-State Circuits Conference,* vol. XXX, pp. 98 - 99, February 1987

Ref: T. Wakimoto, et al, "Si bipolar 2GS/s 6b flash A/D conversion LSI," *IEEE International Solid-State Circuits Conference,* vol. XXXI, pp. 232 - 233, February 1988