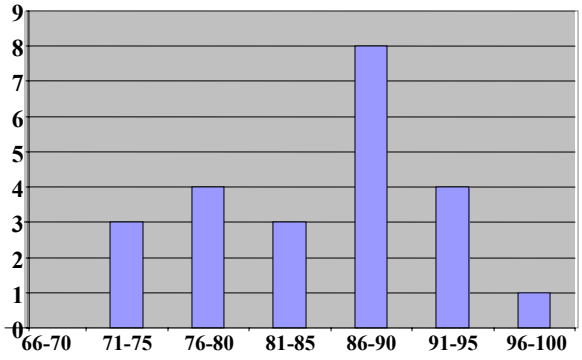
EE247
Lecture 19

ADC Converters

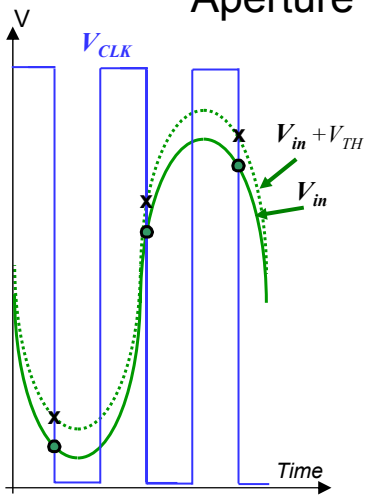
- Track & hold (continued)
  - T/H aperture uncertainty
- ADC architectures and design
  - Serial- slope type
  - Successive approximation
  - Flash ADC and its sources of error: comparator offset, sparkle code & meta-stability
- Comparator design
  - Single-stage open-loop amplifier
  - Cascade of open-loop amplifiers
  - Problem associated with DC offset
    - Cascaded output series cancellation
    - Input series cancellation
    - Offset cancellation through additional input pair plus offset storage capacitors

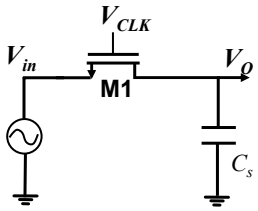
EE247
Midterm Exam Results

Average→ 85.5/100
Standard Deviation→ 6.5
Maximum=97/100
Minimum=71/100



Track & Hold
Aperture Time Error

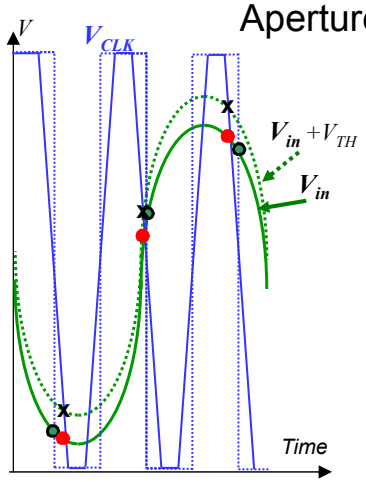




Transition from track to hold:
Occurs when device turns fully off
→ $V_{CLK}=V_{in}+V_{TH}$

Sharp fall-time wrt signal change
→ no aperture error

Track & Hold
Aperture Time Error



Slow falling clock → aperture error

$V_{in}=A\ sin(2\pi f_{in}t)$

$\varepsilon=f_{in}xAx\ \ t_{fall}\ /V_{CLK}$

$SDR=-20log\varepsilon-4\ [dB]$ (imperical see Ref.)

Example:
Nyquist rate *10-bit ADC* & $A=V_{CLK}/4$
→$SQNR=62dB$
for distortion due to aperture error < quant noise
→ $t_{fall}< 2x10^{-3}/f_{in}$
→ *Worst case:* $f_{in}=f_s/2$
→ $t_{fall}< 4x10^{-3}/f_s$
→*e.g.* $f_s=100MHz$, $t_{fall}<40psec$

Ref: P. J. Lim and B. A. Wooley, "A high-speed sample-and-hold technique using a Miller hold capacitance," *IEEE Journal of Solid-State Circuits*, vol. 26, pp. 643 - 651, April 1991.

Track & Hold
Aperture Time Error

- Aperture error analysis applies to simple sampling network
- Bottom plate sampling → minimizes aperture error
- Boosted clock → reduces aperture error

→ Clock edge fall/rise trade-off between switch charge injection versus aperture error

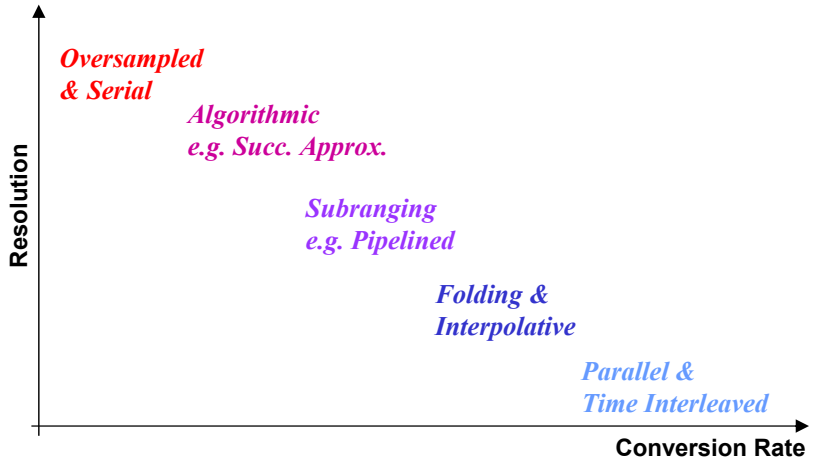
Ref: P. J. Lim and B. A. Wooley, "A high-speed sample-and-hold technique using a Miller hold capacitance," *IEEE Journal of Solid-State Circuits,* vol. 26, pp. 643 - 651, April 1991.

ADC
Architecture & Design

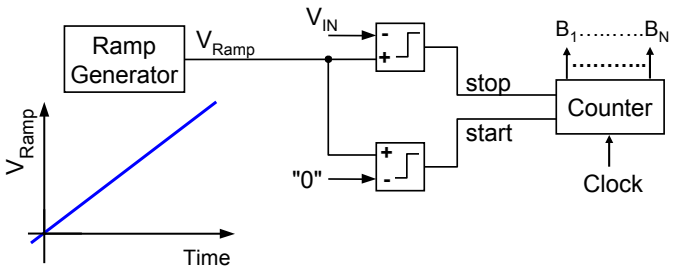
ADC Architectures

- Slope type converters
- Successive approximation
- Flash
- Time-interleaved / parallel converter
- Folding
- Residue type ADCs
  - Two-step
  - Pipeline
  - …
- Oversampled ADCs

Various ADC Architectures
Resolution/Conversion Rate



Serial ADC
Single Slope

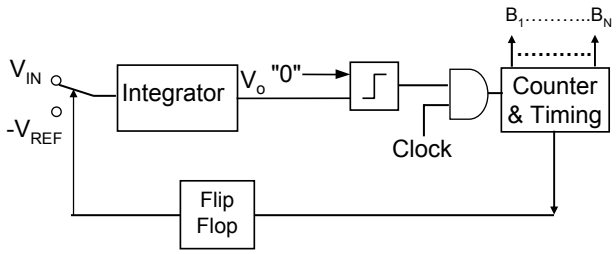


- Counter starts counting @ V_{Ramp}=0
- Counter stops counting for V_{IN}=V_{Ramp}
  → Counter output proportional to V_{IN}

Single Slope ADC

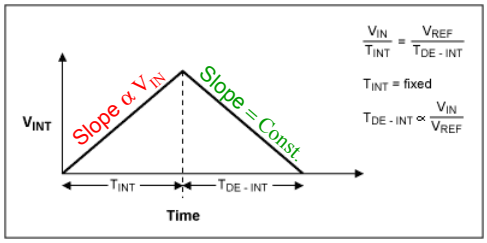
- Advantages:
  - Low complexity & simple
  - INL depends on ramp linearity & not component matching
  - Inherently monotonic
- Disadvantages:
  - Slow (2^N clock pulses for N-bit conversion) (e.g. N=16 f_{clock}=*1MHz* → needs *65000x1*μ*s=65ms*/conversion)
  - Hard to generate precise ramp required for high resolution ADCs
  - Need to calibrate ramp slope versus V_{IN}
- Better: Dual Slope, Multi-Slope

Serial ADC
Dual Slope



- First: V_{IN} is integrated for a fixed time ($2^N x T_{CLK}$)
  → $V_o = 2^N x T_{CLK}\ V_{IN}/\tau_{intg}$
- Next: V_o is de-integrated with V_{REF} until $V_o=0$
  → Counter output = $2^N\ V_{IN}/V_{REF}$

Dual Slope ADC



http://www.maxim-ic.com/appnotes.cfm/appnote_number/1041

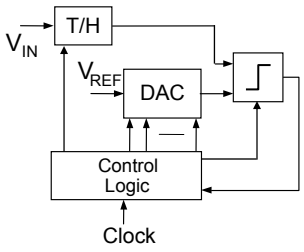
- Integrate V_{in} for fixed time (T_{INT}), de-integrate with V_{REF} applied → $T_{De\text{-}Int} \sim 2^N x T_{CLK} x V_{in}/V_{REF}$
- Most laboratory DVMs use this type of ADC

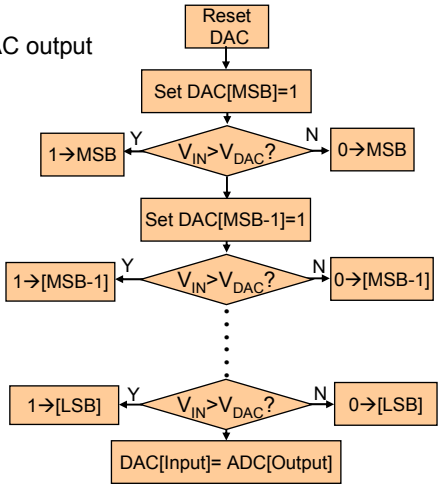
Dual Slope ADC

- Advantage:
  - Accuracy to 1st order independent of integrator time-constant and clock period
  - Comparator offset referred to input is attenuated by integrator high DC gain
  - Insensitive to most linear error sources
  - DNL is a function of clock jitter
  - Power line (60Hz) xtalk effect on reading can be canceled by: choosing conversion time multiple of 1/60Hz
  - High accuracy achievable (16+bit)
- Disadvantage:
  - Slow (maximum $2x2^{N}xT_{clk}$ per conversion)
  - Integrator opamp offset results in ADC offset (can cancel)
  - Finite opamp gain gives rise to INL

Successive Approximation ADC SAR

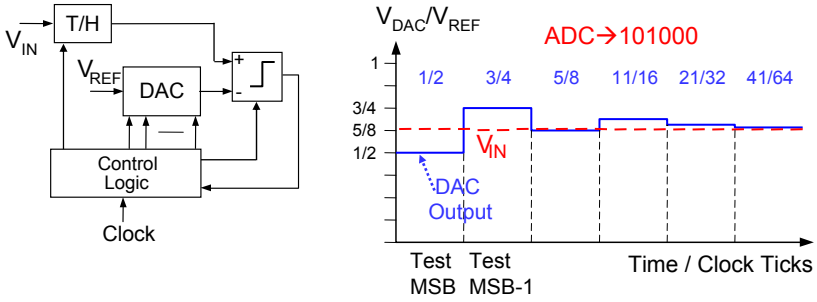
- Algorithmic type ADC
- Based on binary search over DAC output





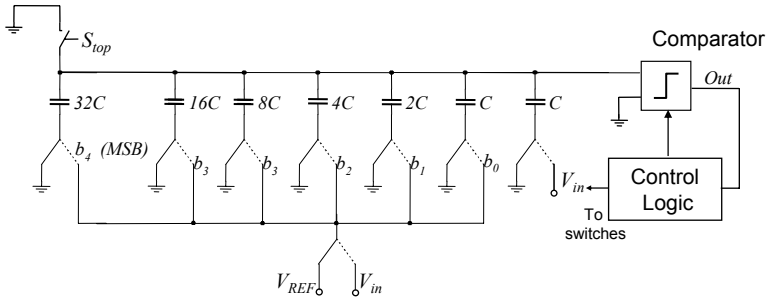
Successive Approximation ADC

Example: 6-bit ADC & $V_{IN}=5/8V_{REF}$



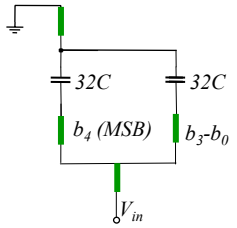
- High accuracy achievable (16+ Bits)
- Required N clock cycles for N-bit conversion (much faster than slope type)
- Moderate speed proportional to N (typically MHz range)

Example: SAR ADC
Charge Redistribution Type

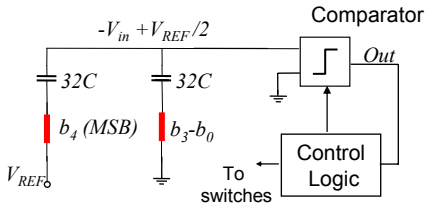


- Built with binary weighted capacitors, switches, comparator & control logic
- T/H inherent in DAC

Charge Redistribution Type SAR DAC Operation: MSB



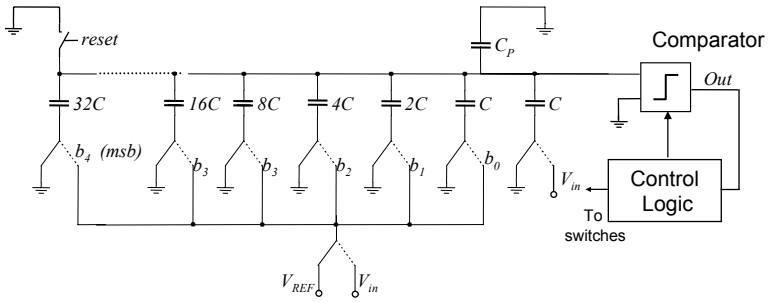
Phase 1



Phase 2

- Operation starts by connecting all top plate to gnd and all bottom plates to V_{in}
- To test the MSB all top plate are opened bottom plate of 32C connected to V_{REF} & rest of bottom plates connected to ground → input to comparator= $-V_{in}+V_{REF}/2$
- Comparator is strobed to determine the polarity of input signal:
  - If negative MSB=1, else MSB=0
- The process continues until all bits are determined

Example: SAR ADC Charge Redistribution Type

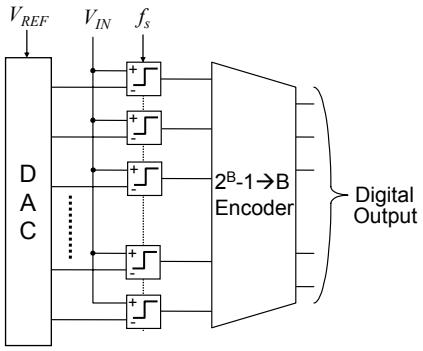


- To 1st order parasitic (C_p) insensitive since top plate driven from initial 0 to final 0 by the global negative feedback
- Linearity is a function of accuracy of C ratios
- Possible to add a C ratio calibration cycle (see Ref.)

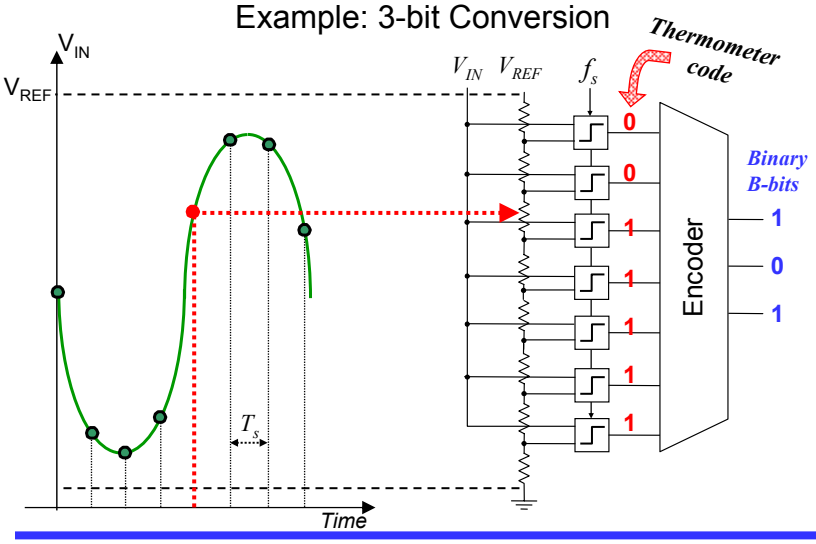
Ref: H. Lee, D. A. Hodges, and P. R. Gray, "A self-calibrating 15 bit CMOS A/D converter," *IEEE Journal of Solid-State Circuits,* vol. 19, pp. 813 - 819, December 1984.

Flash ADC

- B-bit flash ADC:
  - DAC generates all possible $2^B - 1$ levels
  - $2^B - 1$ comparators compare V_{IN} to DAC outputs
  - Comparator output:
    - If $V_{DAC} < V_{IN} \rightarrow 1$
    - If $V_{DAC} > V_{IN} \rightarrow 0$
  - Comparator outputs form thermometer code
  - Encoder converts thermometer to binary code

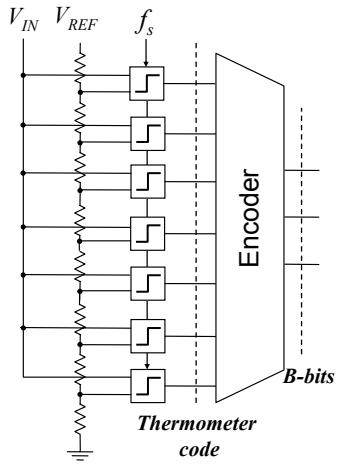


Flash ADC Converter Example: 3-bit Conversion



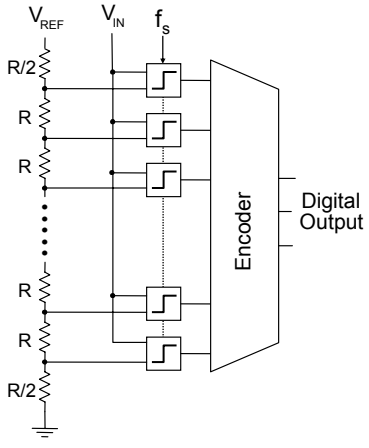
Flash Converter Characteristics

- Very fast: only 1 clock cycle per conversion
  - ½ clock cycle→ V_{IN} & V_{DAC} comparison
  - ½ clock cycle→ 2^B-1 to B encoding
- High complexity: 2^B-1 comparators
- Input capacitance of 2^B-1 comparators connected to the input node:
  - → High capacitance @ input node



Flash Converter
Example: 8-bit ADC Design Considerations

- 8-bit→ 255 comparators
- V_{REF}=1V → 1LSB=4mV
- DNL<1/2LSB → Comparator input referred offset < 2mV
- Assuming close to 100% yield, 2mV =6σ_{offset}
  → σ_{offset} < 0.33mV



Flash ADC Converter
Example: 8-bits ADC (continued)

→ $1\sigma_{Offset} < 0.33mV$

- Let us assume in the technology used:
  - Voffset-per-unit-sqrt(WxL)=$3\ mVx\ \mu$

$$V_{0\,ffset} = \frac{3mV}{\sqrt{W \times L}} = 0.33mV \quad \rightarrow W \times L = 83\mu^2$$

$$\text{Assuming: } C_{ox} = 9\,fF/\mu^2 \quad \rightarrow C_{GS} = \frac{2}{3} C_{ox} W \times L = 496\,fF$$

$$\rightarrow \text{Total input capacitance: } 255 \times 0.496 = 126.5\,pF!$$

  - Issues:
    - Si area quite large
    - Large ADC input capacitance
    - Since depending on input voltage different number of comparator input transistors would be on/off- total input capacitance varies as input varies

    → Nonlinear input capacitance could give rise to signal distortion

Ref: M. J. M. Pelgrom, A. C. J. Duinmaijer, and A. P. G. Welbers, "Matching properties of MOS transistors," *IEEE Journal of Solid-State Circuits,* vol. 24, pp. 1433 - 1439, October 1989.

Flash ADC Converter
Example (continued)

Trade-offs:

- Allowing larger DNL e.g. 1LSB instead of 0.5LSB:
  - Increases the maximum allowable input-referred offset voltage by a factor of 2
  - Decreases the required device WxL by a factor of 4
  - Reduces the input device area by a factor of 4
  - Reduces the input capacitance by a factor of 4!
- Reducing the ADC resolution by 1-bit
  - Increases the maximum allowable input-referred offset voltage by a factor of 2
  - Decreases the required device WxL by a factor of 4
  - Reduces the input device area by a factor of 4
  - Reduce the input capacitance by a factor of 4

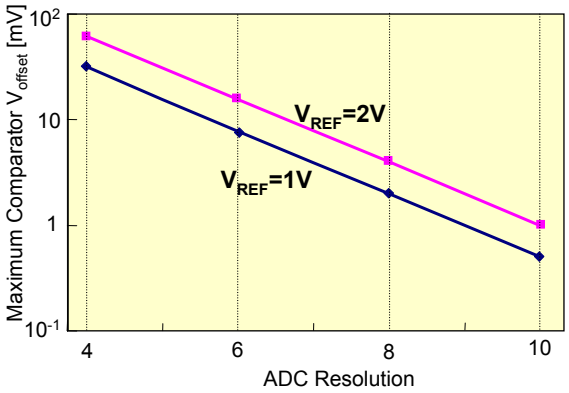
Flash Converter
Maximum Tolerable Comparator Offset versus ADC Resolution

Assumption:

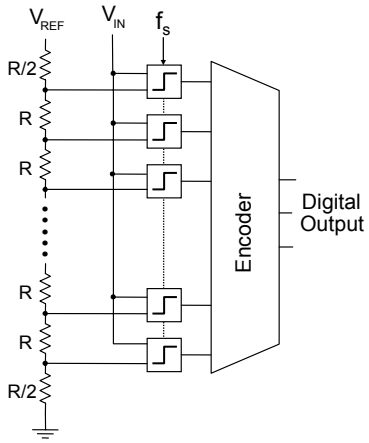
DNL=0.5LSB

Note:

Graph shows max. tolerable offset, note that depending on min acceptable yield, the derived offset numbers are associated with 2σ to 6σ offset voltage

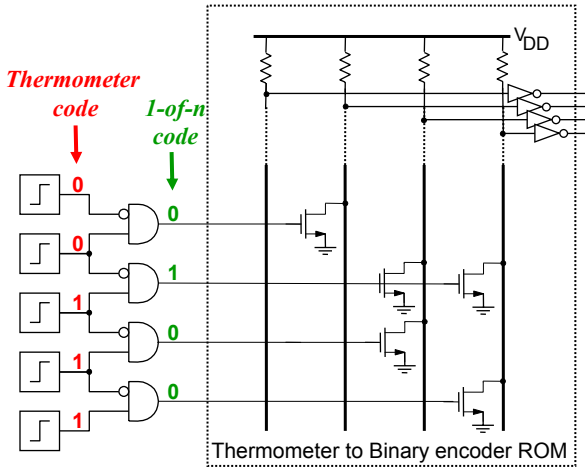


Flash Converter Sources of Error



- Comparator input:
  - Offset
  - Nonlinear input capacitance
  - Feedthrough of input signal to reference ladder
  - Kickback noise (disturbs reference)
  - Signal dependent sampling time
- Comparator output:
  - Sparkle codes (… 111101000 …)
  - Metastability

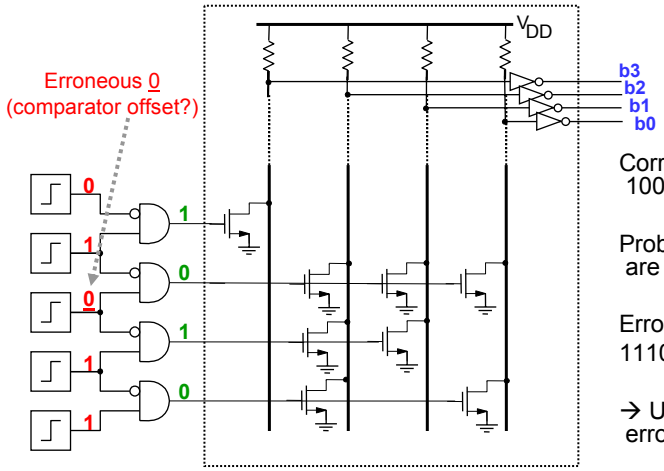
Typical Flash Output Encoder



- Thermometer code → 1-of-n decoding
- Final encoding → NOR ROM
- Ideally, for each code, only one ROM row is on

	b3	b2	b1	b0
Output→	0	0	1	1

Sparkle Codes



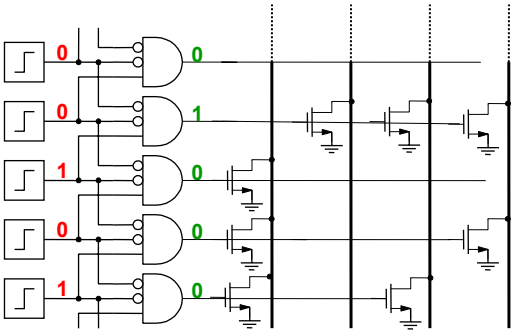
Correct Output: 1000

Problem: Two rows are on

Erroneous Output: 1110

→ Up to ~ ½ FS error!!

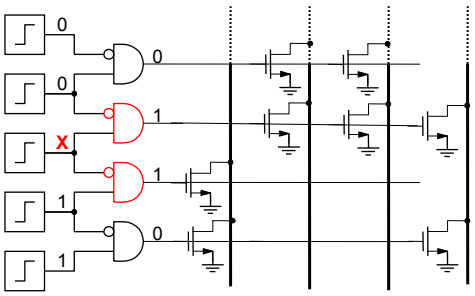
Sparkle Tolerant Encoder



- Protects against a *single* sparkle.
- Possible to improve level of sparkle protection by increasing # of NAND gate inputs

Ref: C. Mangelsdorf et al, "A 400-MHz Flash Converter with Error Correction," JSSC February 1990, pp. 997-1002

Meta-Stability



Different gates interpret metastable output X differently

Correct output: 1000

Erroneous output: 0000

Solutions:
- –Latches (high power)
- –Gray encoding

Ref: C. Portmann and T. Meng, "Power-Efficient Metastability Error Reduction in CMOS Flash A/D Converters," JSSC August 1996, pp. 1132-40

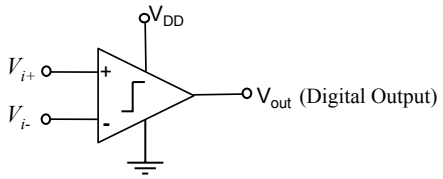
Gray Encoding
Example: 3bit ADC

Thermometer Code							Gray			Binary		
T_7	T_6	T_5	T_4	T_3	T_2	T_1	G_3	G_2	G_1	B_3	B_2	B_1
0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	0	0	1	0	0	1
0	0	0	0	0	1	1	0	1	1	0	1	0
0	0	0	0	1	1	1	0	1	0	0	1	1
0	0	0	1	1	1	1	1	1	0	1	0	0
0	0	1	1	1	1	1	1	1	1	1	0	1
0	1	1	1	1	1	1	1	0	1	1	1	0
1	1	1	1	1	1	1	1	0	0	1	1	1

$$G_1 = T_1\overline{T_3} + T_5\overline{T_7}$$
$$G_2 = T_2\overline{T_6}$$
$$G_3 = T_4$$

- Each T_i affects only one G_i
  → Avoids disagreement of interpretation by multiple gates
- Protects also against sparkles
- Follow Gray encoder by (latch and) binary encoder

Voltage Comparators



Play an important role in majority of ADCs

Function: Compare the instantaneous value of two analog signals & generate a digital output voltage based on the sign of the difference:

If $V_{i+} - V_{i-} > 0 \rightarrow V_{out} = \text{“1”}$
If $V_{i+} - V_{i-} < 0 \rightarrow V_{out} = \text{“0”}$

Voltage Comparator Architectures

Comparator architectures:

- High gain amplifier with differential analog input & single-ended large swing output
  - Output swing has to be compatible with driving digital logic circuits
  - Open-loop amplification→ no frequency compensation required
  - Precise gain not required
- Latched comparators; in response to a strobe (clock edge), input stage disabled & digital output stored in a latch till next strobe
  - Two options for implementation :
    - Latch-only comparator
    - Low-gain preamplifier + high-sensitivity latch
- Sampled-data comparators
  - T/H input
  - Offset cancellation

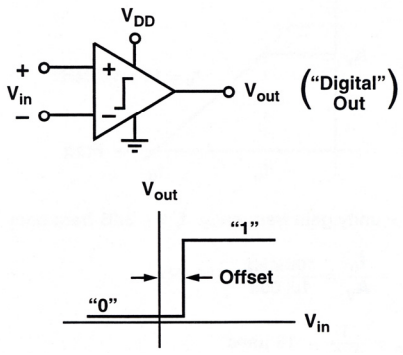
Comparators Built with High-Gain Amplifier

Amplify V_{in}(min) to V_{DD}
→ V_{in}(min) determined by ADC resolution

Example: 12-bit ADC with:
- V_{FS}= 1.5V→ 1LSB=0.36mV
- V_{DD}=1.8V

→ For 1.8V output & 0.5LSB precision:

$$A_v^{Min} = \frac{1.8V}{0.18mV} \approx 10{,}000$$



Comparators
1-Single-Stage Amplification

$f_u = unity\text{-}gain\ frequency,\ f_o = -3dB\ frequency$

$$f_o = \frac{f_u}{A_V}$$

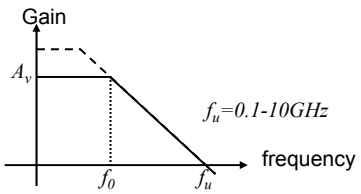
$Example:\ f_u = 10GHz\ \ \&\ \ A_V = 10{,}000$

$$f_o = \frac{10GHz}{10{,}000} \approx 1MHz$$

$$\tau_{settling} = \frac{1}{2\pi f_o} = 0.16\mu sec$$

$Allow\ a\ few\ \tau\ for\ output\ to\ settle$

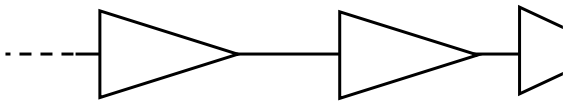
$$f_{Clock}^{Max.} \rightarrow \frac{1}{5\tau_{settling}} \approx 1.26MHz$$



Assumption: Single pole amplifier

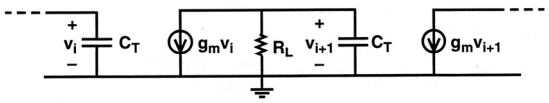
Too slow for majority of applications!
→ Try cascade of lower gain stages to broaden frequency of operation

Comparators
2- Cascade of Open Loop Amplifiers



The stages identical → small-signal model for the cascades:

One stage:



$|A_V(0)| = g_m R_L$

ω_o = – 3dB frequency = $\frac{1}{R_L C_T}$

ω_u = – unity gain frequency = G×BW = $\frac{g_m}{C_T}$

$\therefore\ \omega_o = \frac{\omega_u}{|A_V(0)|}$

Open Loop Cascade of Amplifiers

For an N-stage cascade:

$$A_T(j\omega) = [A_V(j\omega)]^N = \frac{[A_V(0)]^N}{\left(1+j\frac{\omega}{\omega_0}\right)^N}$$

Define

$\omega_{oN} \equiv$ **–3dB frequency of the N-stage cascade**

Then

$$|A_T(j\omega_{oN})| = \frac{|A_V(0)|^N}{\sqrt{2}}$$

and

$$\omega_{oN} = \omega_o\sqrt{2^{1/N}-1} = \frac{\omega_u}{|A_V(0)|}\sqrt{2^{1/N}-1}$$

Example: N=4 → $\omega_{oN}=0.43\omega_o$

∴ **For a specified $|A_T(0)|$**

$$|A_V(0)| = |A_T(0)|^{1/N}$$

$$\Rightarrow \omega_{oN} = \frac{\omega_u}{|A_T(0)|^{1/N}}\sqrt{2^{1/N}-1}$$

Thus,

$$\frac{\omega_{oN}}{\omega_{o1}} = \left[\frac{\omega_u}{|A_T(0)|^{1/N}}\sqrt{2^{1/N}-1}\right] \Big/ \left[\frac{\omega_u}{|A_T(0)|}\right]$$

$$= |A_T(0)|^{\left(\frac{N-1}{N}\right)}\sqrt{2^{1/N}-1}$$

Example: N=4, A_T=10000→ $\omega_{oN}=430\omega_{o1}$

Open Loop Cascade of Amplifiers

For $|A_T(DC)|$=10,000

N	ω_{oN}/ω_{o1}	$\lvert A_V(0)\rvert$
1	1	10,000
2	64	100
3	236	21.5
4	435	10
5	611	6.3
10	1067	2.5
20	1185	1.6

Example:

$N=3,\ f_u=10GHz\ \&\ |A_T(0)|=10000$

$$f_{oN} = \frac{10GHz}{(10{,}000)^{1/3}}\sqrt{2^{1/3-1}} \approx 237MHz$$

$$\tau_{settling} = \frac{1}{2\pi f_o} = 0.7nsec$$

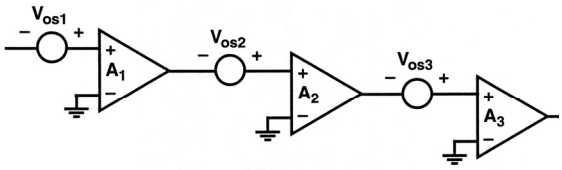
Allow a few τ for output to settle

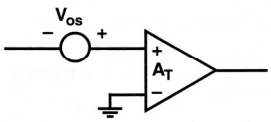
$$f_{Clock}^{Max} \rightarrow \frac{1}{5\tau_{settling}} \approx 290MHz$$

f_{max} improved from *1.26MHz to 290MHz* → *X236*

Open Loop Cascade of Amplifiers Offset Voltage

- **From offset point of view: high gain/stage is preferred**
- **Choice of # of stage**
  →bandwidth vs offset tradeoff



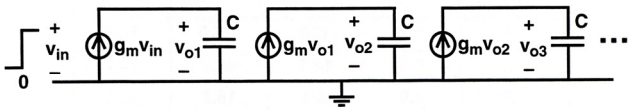


$$A_T = A_1 \cdot A_2 \cdot A_3$$

Input-referred offset $\rightarrow V_{os} = V_{os1} + \frac{V_{os2}}{A_1} + \frac{V_{os3}}{A_1 \cdot A_2}$

Open Loop Cascade of Amplifiers Step Response

- **Assuming linear behavior (not slew limited)**



$$v_{o1} = \frac{1}{C}\int_0^t g_m v_{in} dt = \frac{g_m}{C} v_{in} t$$

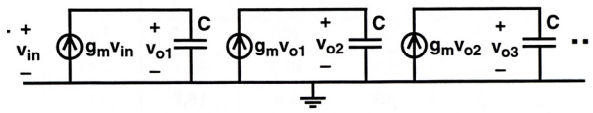
$$v_{o2} = \frac{1}{C}\int_0^t g_m v_{o1} dt = \frac{g_m}{C}\int_0^t \frac{g_m}{C} v_{in} t\, dt = \frac{1}{2}\left(\frac{g_m}{C}\right)^2 v_{in} t^2$$

$$v_{o3} = \frac{1}{C}\int_0^t g_m v_{o2} dt = \frac{g_m}{C}\int_0^t \left[\frac{1}{2}\left(\frac{g_m}{C}\right)^2 v_{in} t^2\right] dt$$

$$= \frac{1}{3}\left(\frac{1}{2}\right)\left(\frac{g_m}{C}\right)^3 v_{in} t^3$$

Open Loop Cascade of Amplifiers Step Response

•**Assuming linear behavior**



N Stages

$$v_{oN} = \left(\frac{g_m}{C}\right)^N \left(\frac{t^N}{N!}\right) v_{in}$$

For the output to reach a specified v_{out} (i.e., $v_{oN} = v_{out}$) the delay is

$$\tau_D = \left(\frac{C}{g_m}\right)\left[(N!)\left(\frac{v_{out}}{v_{in}}\right)\right]^{1/N}$$

Open Loop Cascade of Amplifiers Delay/(C/g_m)

- **Minimum total delay broad function of N**
- **Relationship between # of stages resulting in minimize delay (N_{op}) and gain (V_{out}/V_{in}) approximately:**

$$N_{opt} \approx 1 + \log_2 A_T \quad for \ A < 1000$$

$$N_{opt} \approx 1.2 \ln A_T \quad for \ A \geq 1000$$

Delay/(C/g_m)

N \ v_{out}/v_{in}	10	100	1000	10K
1	10	100	1000	10K
2	4.5	14.1	44.7	141
3	3.9	8.4	18.2	39.1
4	3.9	7.0	12.4	22.1
5	4.1	6.5	10.4	16.4
6	4.4	6.4	9.5	13.9
7	4.7	6.5	9.1	12.6
8	5.0	6.7	8.9	11.9
9	5.4	6.9	8.9	11.5
10	5.7	7.2	9.0	11.4
11	6.1	7.5	9.2	11.3
12	6.4	7.8	9.4	11.4
20	9.3	10.5	11.7	13.2

Ref: J.T. Wu, et al., "A 100-MHz pipelined CMOS comparator " *IEEE Journal of Solid-State Circuits,* vol. 23, pp. 1379 - 1385, December 1988.

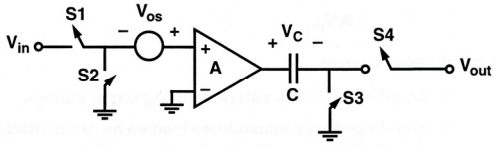
Offset Cancellation

- **In sampled-data cascade of amplifiers Vos can be cancelled**
  → Store on ac-coupling caps in series with amp stages
- **Offset associated with a specific amp can be cancelled by storing it in series with either the input or the output of that stage**
- **Offset can be cancelled by adding a pair of auxiliary inputs to the amplifier and storing the offset on capacitors connected to the aux. inputs during offset cancellation phase**

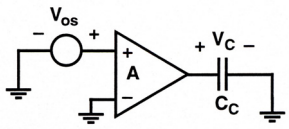
Ref: J.T. Wu, et al., "A 100-MHz pipelined CMOS comparator " *IEEE Journal of Solid-State Circuits,* vol. 23, pp. 1379 - 1385, December 1988.

Offset Cancellation
Output Series Cancellation

- **Amp modeled as ideal + V_{os} (input referred)**



- **Store offset:**
  - **S1, S4→ open**
  - **S2, S3→ closed**
    → V_C=AxV_{OS}



$V_C = A \cdot V_{os}$

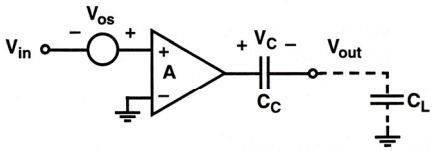
Ref: J.T. Wu, et al., "A 100-MHz pipelined CMOS comparator " *IEEE Journal of Solid-State Circuits,* vol. 23, pp. 1379 - 1385, December 1988.

Offset Cancellation
Output Series Cancellation

Amplify:

- **S2, S3→ open**
- **S1, S4→ closed**

  →V_C=AxV_{OS}

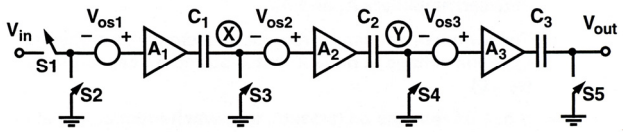


Circuit requirements:

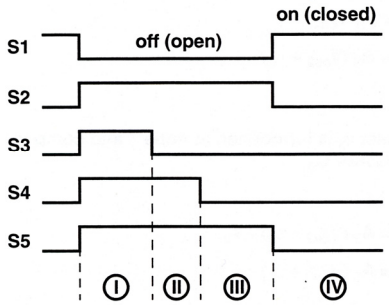
- **Amp not saturate during offset storage**
- **High-impedance (C) load → C_c not discharged**
- **C_c >> C_L to avoid attenuation**
- **C_c >> C_{switch} avoid excessive offset due to charge injection**

$$V_{out} = A\cdot(V_{in} + V_{os}) - V_C$$
$$= A\cdot(V_{in} + V_{os}) - A\cdot V_{os}$$
$$= A\cdot V_{in}$$

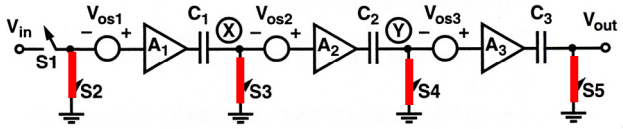
Offset Cancellation
Cascaded Output Series Cancellation



Note: Offset storage capacitors in series with the amplifier outputs

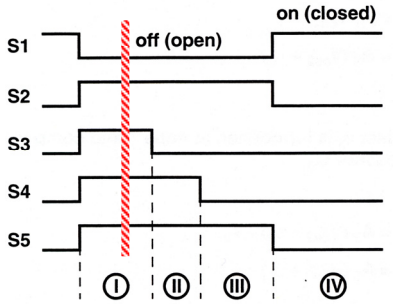


Offset Cancellation
Cascaded Output Series Cancellation

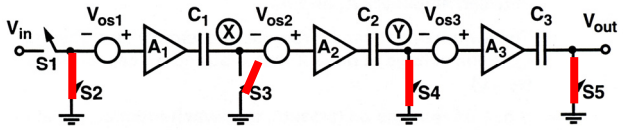


1- S1→ open, S2,3,4,5 closed

$V_{C1}=A_1xV_{os1}$
$V_{C2}=A_2xV_{os2}$
$V_{C3}=A_1xV_{os3}$



Offset Cancellation
Cascaded Output Series Cancellation

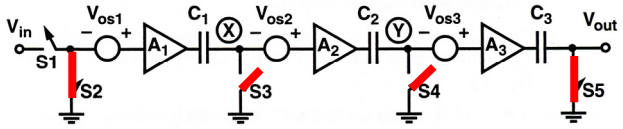


2- S3→ open first

- Feedthrough from S3 → offset on X
- Switch offset , ε_3 induced on node X
- Since S4 remains closed, offset associated with ε_3 → stored on C2

$V_X= \varepsilon_3$
$V_{C1}=A_1xV_{os1}- \varepsilon_3$
$V_{C2}=A_2x(V_{os2}+ \varepsilon_3)$

Offset Cancellation
Cascaded Output Series Cancellation



3- S4→ open

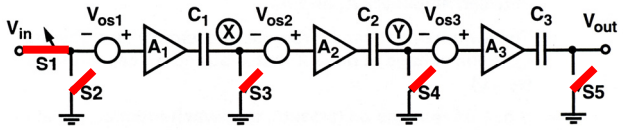
- Feedthrough from S4 → offset on Y
- Switch offset , ε_4 induces error on node Y
- Since S5 remains closed, offset associated with ε_4 → stored on C3

$$V_Y = \varepsilon_4$$

$$V_{C2} = A_2 x (V_{os2} + \varepsilon_3) - \varepsilon_4$$

$$V_{C3} = A_3 x (V_{os3} + \varepsilon_4)$$

Offset Cancellation
Cascaded Output Series Cancellation



4- S2→ open, S1→ closed, S5→ open

- S1 closed & S2 open → since input connected to low impedance source charge injection not of major concern
- Switch offset , ε_5 introduced due to S5 opening

$$V_X = A_1 x (V_{in} + V_{os1}) - V_{C1}$$

$$= A_1 x (V_{in} + V_{os1}) - (A_1 . V_{os1} - \varepsilon_3)$$

$$= A_1 . V_{in} + \varepsilon_3$$

Offset Cancellation
Cascaded Output Series Cancellation

$$V_y = A_2x(V_x+V_{os2}) - V_{C2}$$
$$= A_2x(A_1V_{in} + \varepsilon_3 + V_{os2}) - [A_2.(V_{os2}+\varepsilon_3) - \varepsilon_4]$$
$$= A_1.A_2.V_{in} + \varepsilon_4$$

$$V_{out} = A_3x(V_y+V_{os3}) - V_{C3}$$
$$= A_3.(A_2xA_1V_{in} + \varepsilon_4 + V_{os3}) - [A_3.(V_{os3}+\varepsilon_4) - \varepsilon_5]$$
$$= A_1.A_2.A_3.V_{in} + \varepsilon_5$$

Offset Cancellation
Cascaded Output Series Cancellation

$$V_{out} = A_1.A_2.A_3.(V_{in} + \varepsilon_5/A_1.A_2.A_3)$$
Input-Referred Offset = $\varepsilon_5/A_1.A_2.A_3$

Example:
3-stage open-loop differential amplifier with offset cancellation + output amplifier (see Ref.)

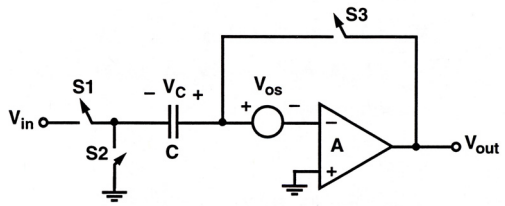
$A_{Total}(DC) = 2x10^6 = 126dB$
Input-referred offset < 5μV

Ref: :R. Poujois and J. Borel, "A low drift fully integrated MOSFET operational amplifier," *IEEE Journal of Solid-State Circuits,* vol. 13, pp. 499 - 503, August 1978.

Offset Cancellation
Output Series Cancellation

- Advantages:
  - Almost compete cancellation
  - Closed-loop stability not required
- Disadvantages:
  - Gain per stage must be small
  - Offset storage C in the signal path- could slow down overall performance

Offset Cancellation
Input Series Cancellation

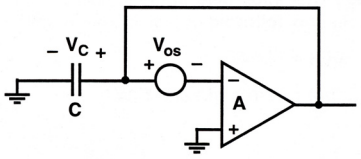


Ref: :R. Poujois and J. Borel, "A low drift fully integrated MOSFET operational amplifier," *IEEE Journal of Solid-State Circuits,* vol. 13, pp. 499 - 503, August 1978.

Offset Cancellation
Input Series Cancellation

Store offset

S1 = 0 (off)
S2, S3 = 1 (conducting)



Note: Mandates closed-loop stability

$$V_C = -A(V_C - V_{os})$$

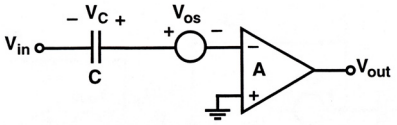
$$= \left(\frac{A}{A+1}\right)V_{os}$$

Ref: :R. Poujois and J. Borel, "A low drift fully integrated MOSFET operational amplifier," *IEEE Journal of Solid-State Circuits,* vol. 13, pp. 499 - 503, August 1978.

Offset Cancellation
Input Series Cancellation

Amplify

S2, S3 → open
S1→ closed



$$V_{out} = -A(V_{in} + V_C - V_{os}) = -A\left[V_{in} + V_{os}\left(\frac{A}{A+1} - 1\right)\right]$$

$$\therefore\ V_{out} = -A\left(V_{in} - \frac{V_{os}}{A+1}\right)$$

and

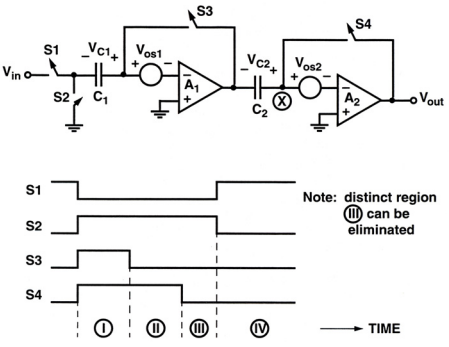
$$\textbf{Input-Referred Offset} = \frac{V_{os}}{A+1}$$

Example: A=4
→Input-referred offset =V_{os}/5

Offset Cancellation
Cascaded Input Series Cancellation

$$V_{out} = A_1 A_2\left[V_{in} + \frac{V_{os2}}{A_1(A_2+1)} - \frac{\varepsilon_2}{A_1}\right]$$

$$\text{Input-Referred Offset} = \frac{V_{os2}}{A_1(A_2+1)} - \frac{\varepsilon_2}{A_1}$$



ε_2 →charge injection associated with opening of S4

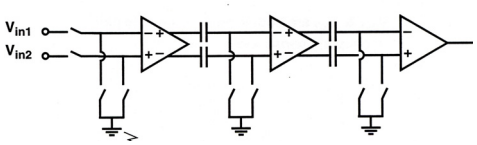
Offset Cancellation
Input Series Cancellation

- Advantages:
  - In applications such as C-array successive approximation ADCs can use C-array to store offset
- Disadvantages:
  - Cancellation not complete
  - Requires closed loop stability
  - Offset storage C in the signal path- could slow down overall performance

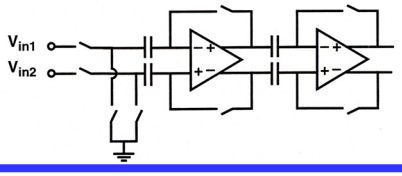
CMOS Comparators
Cascade of Gain Stages

Fully differential gain stages → 1st order cancellation of switch feedthrough offset

1- Output series offset cancellation

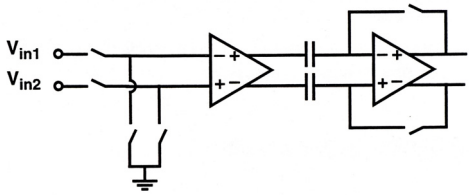


2- Input series offset cancellation



CMOS Comparators
Cascade of Gain Stages

3-Combined input & output series offset cancellation

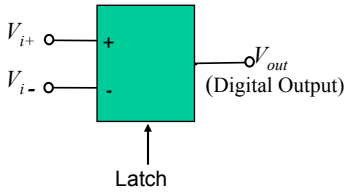


V_{os1} & V_{os2} are both stored on a single pair of coupling capacitors

Offset Cancellation

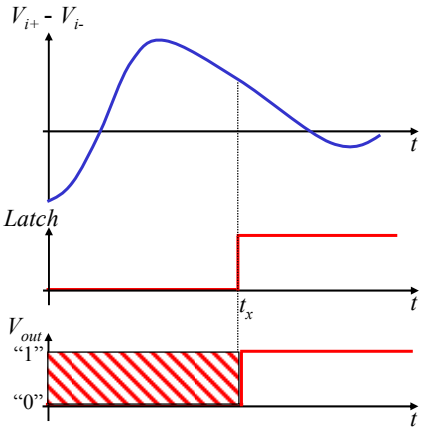
- Cancel offset by additional pair of inputs (Lecture 18 slide 46 -48)

Latched Comparators



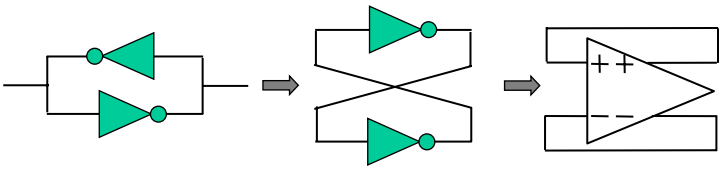
Compares two input voltages at time t_x & generates a digital output:

If $V_{i+} - V_{i-} > 0 \rightarrow V_{out}$="1"
If $V_{i+} - V_{i-} < 0 \rightarrow V_{out}$="0"



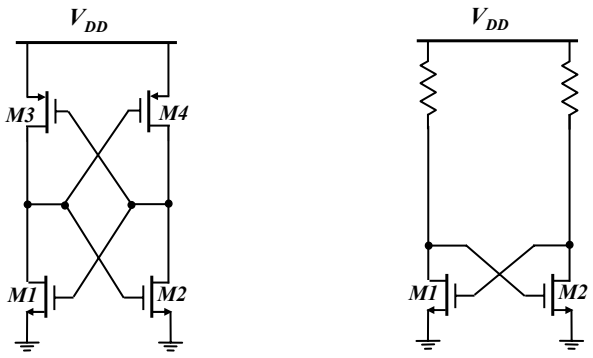
CMOS Latched Comparators

Comparator amplification need not be linear
→ can use a latch → regeneration



Latch→ Amplification + positive feedback

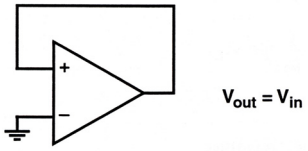
Simplest Form of CMOS Latch



CMOS Latched Comparators
Small Signal Model

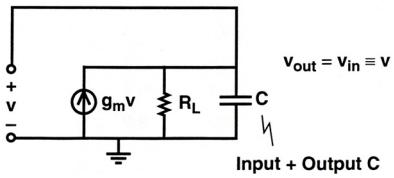
Latch can be modeled as a:

→ Single-pole amp + positive feedback



$V_{out} = V_{in}$

Small signal ac half circuit



CMOS Latched Comparator
Latch Delay

$$g_m V = \frac{V}{R_L} + C\frac{dV}{dt}$$

$$\frac{g_m}{C}\left(1 - \frac{1}{g_m R_L}\right)V = \frac{dV}{dt} \qquad \frac{g_m}{C}\left(1 - \frac{1}{g_m R_L}\right)dt = \frac{dV}{V}$$

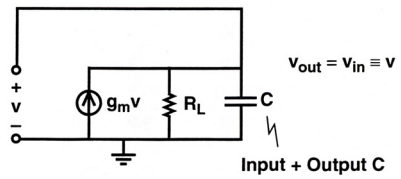
Integrating both sides: $\frac{g_m}{C}\left(1 - \frac{1}{g_m R_L}\right)\int_{t1}^{t2} dt = \int_{V1}^{V2}\frac{1}{V}dV$ $\qquad \left(\int_b^a \frac{1}{x}dx = \ln x\Big|_b^a = \ln a - \ln b = \ln\frac{a}{b}\right)$

Latch Delay:

$$t_D = t_2 - t_1 = \frac{C}{g_m}\left(\frac{1}{1 - \frac{1}{g_m R_L}}\right)\ln\left(\frac{V_2}{V_1}\right)$$

For $g_m R_L >> 1$

$$t_D \approx \frac{C}{g_m}\ln\left(\frac{V_2}{V_1}\right)$$



CMOS Latched Comparators

$$t_D \approx \frac{C}{g_m}\ln\left(\frac{V_2}{V_1}\right)$$

$$\frac{V_2}{V_1} \rightarrow Latch\ Gain = A_L$$

$$\rightarrow t_D \approx \frac{C}{g_m}\ln A_L$$

Normalized Latch Delay

τ_D(3-stage amp)= $18.2(C/g_m)$

A_L	$\frac{t_D}{C/g_m}$
10	2.3
100	4.6
1000	6.9
10K	9.2

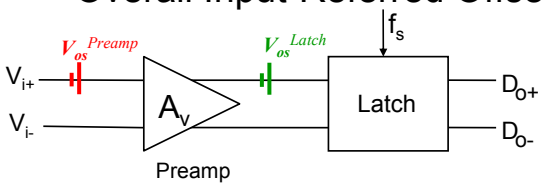
Compared to a 3-stage open-loop cascade of amps for equal overall gain of 1000

→Latch faster by about x3

Latch-Only Comparator

- Much faster compared to cascade of open-loop amplifiers
- Main problem associated with latch-only comparator topology:
  - High input-referred offset voltage (as high as 100mV!)
    - Solution:
      - Use preamplifier to amplify the signal and reduce overall input-referred offset

Pre-Amplifier + Latch
Overall Input-Referred Offset



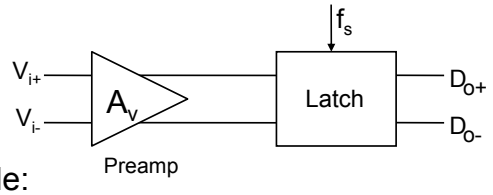
Latch offset attenuated by preamp gain when referred to preamp input.
Assuming the two offset sources are uncorrelated:

$$\sigma_{Input-Referred\_Offset} = \sqrt{\sigma^2_{Vos\_Preamp} + \frac{1}{A^2_{Preamp}}\sigma^2_{Vos\_Latch}}$$

$$Example: \ \sigma_{Vos\_Preamp} = 4mV \ \ \& \ \ \sigma_{Vos\_Latch} = 50mV \ \ \& \ \ A_{Preamp} = 10$$

$$\sigma_{Input-Referred\_Offset} = \sqrt{4^2 + \frac{1}{10^2}50^2} = 6.4mV$$

Pre-Amplifier Tradeoffs



- Example:
  - Latch offset 50 to 100mV
  - Preamp DC gain 10X
  - Preamp input-referred latch offset 5 to 10mV
  - Input-referred preamplifier offset 2 to 10mV
  - Overall input-referred offset 5.5 to 14mV

→ Addition of preamp reduces the latch input-referred offset reduced by ~7 to 9X → ~allows extra 3-bit resolution!