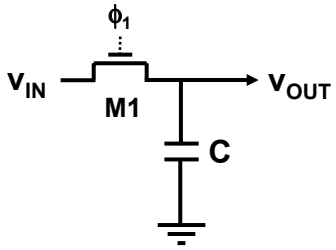
EE247
Lecture 17

- **Nyquist rate ADC converters**
  - Sampling
    - Sampling switch considerations
      - Thermal noise due to switch resistance (last lecture)
      - Clock jitter related non-idealities
      - Sampling switch bandwidth limitations
      - Switch induced distortion
        - Sampling switch conductance dependence on input voltage
        - Clock voltage boosters
      - Sampling switch charge injection & clock feedthrough

Practical Sampling Issues

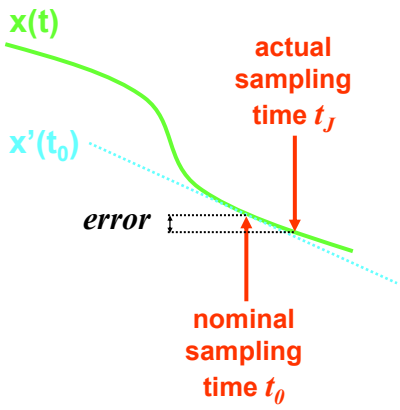


- Switch induced noise due to M1 finite channel resistance
- Clock jitter
- Finite R_{sw} → limited bandwidth → finite acquisition time
- $R_{sw} = f(V_{in})$ → distortion
- Switch charge injection & clock feedthrough

Clock Jitter

- The error voltage is

$$e = x'(t_0)(t_J - t_0)$$



Effect of Clock Jitter on Sampling of a Sinusoidal Signal

Sinusoidal input

$Amplitude: \quad A$
$Frequency: \quad f_x$
$Jitter: \quad dt$

$$x(t) = A\sin(2\pi f_x t)$$

$$x'(t) = 2\pi f_x \, A\cos(2\pi f_x t)$$

$$|x'(t)|_{max} \le 2\pi f_x A$$

$Requirement:$

$$|e(t)| \le |x'(t)|_{max} \, dt$$

$$|e(t)| \le 2\pi f_x A dt$$

Worst case

$$A = A_{FS}/2 \qquad f_x = f_s/2$$

$$|e(t)| << \frac{\Delta}{2} \cong \frac{A_{FS}}{2^{B+1}}$$

$$dt << \frac{1}{2^B \pi f_s}$$

# of Bits	f_s	dt <<
12	1 MHz	78 ps
16	20 MHz	0.24 ps
10	1000 MHz	0.3 ps

Law of Jitter

- The worst case looks pretty stringent …
  what about the "average"?
- Let's calculate the mean squared jitter error (variance)
- If we're sampling a sinusoidal signal

  $x(t) = A\sin(2\pi f_x t)$,

  then
  - $x'(t) = 2\pi f_x A\cos(2\pi f_x t)$
  - $E\{[x'(t)]^2\} = 2\pi^2 f_x^2 A^2$
- Assume the jitter has variance $E\{(t_J - t_0)^2\} = \tau^2$

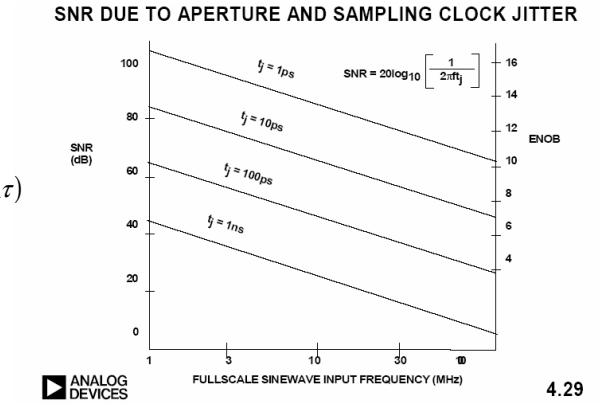
Law of Jitter

- If $x'(t)$ and the jitter are independent
  - $E\{[x'(t)(t_J - t_0)]^2\} = E\{[x'(t)]^2\}\, E\{(t_J - t_0)^2\}$
- Hence, the jitter error power is

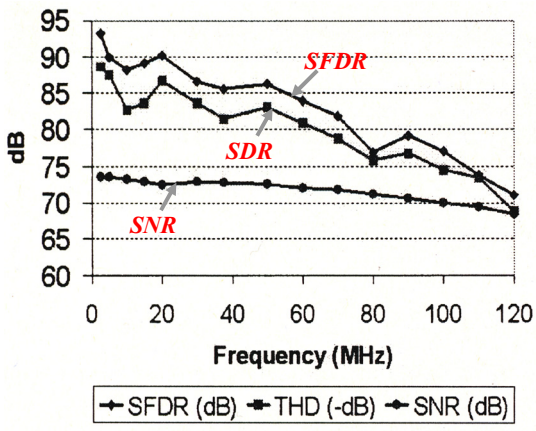
  $$\mathbf{E\{e^2\} = 2\pi^2 f_x^2 A^2 \tau^2}$$
- If the jitter is uncorrelated from sample to sample, this "jitter noise" is white

Law of Jitter

$$DR_{\text{jitter}} = \frac{A^2/2}{2\pi^2 f_x^2 A^2 \tau^2} = \frac{1}{2\pi^2 f_x^2 \tau^2} = -20\log_{10}(2\pi f_x \tau)$$



Example: ADC Spectral Tests



Ref: W. Yang et al., "A 3-V 340-mW 14-b 75-Msample/s CMOS ADC with 85-dB SFDR at Nyquist input," *IEEE J. of Solid-State Circuits*, Dec. 2001

More on Jitter

- In cases where clock signal is provided from off-chip→ have to choose a source with low enough jitter
- On-chip precautions to keep the clock jitter less than single-digit pico-second :
  - Separate supplies as much as possible
  - Separate analog and digital clocks
  - Short inverter chains between clock source and destination
- Few, if any, other analog-to-digital conversion non-idealities have the same symptoms as sampling jitter:
  - RMS noise proportional to input signal frequency
  - RMS noise proportional to input signal amplitude

  →In cases where clock jitter limits the dynamic range, it's easy to tell, but may be difficult to fix...

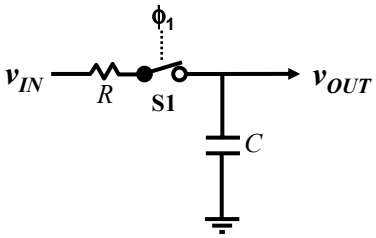
Sampling Acquisition Bandwidth

- The resistance R of switch S1 turns the sampling network into a lowpass filter with finite time constant:

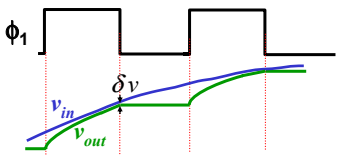
  $\tau = RC$

- Assuming V_{in} is constant during the sampling period and C is initially discharged

- Need to allow enough time for the output to settle to less than 1 ADC LSB → determines minimum duration for ϕ_1 or maximum clock frequency



$$v_{out}(t) = v_{in}\left(1 - e^{-t/\tau}\right)$$



Sampling: Effect of Switch On-Resistance

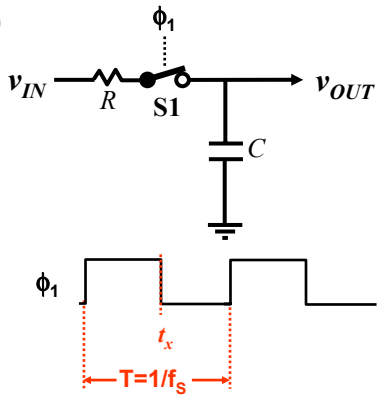
$$V_{in}^{tx} - V_{out}^{tx} << \Delta \quad \text{since} \quad V_{out} = V_{in}\left(1 - e^{-t/\tau}\right)$$

$$\rightarrow V_{in} e^{-T_s/2\tau} << \Delta \quad or \quad \tau << \frac{T_s}{2} \frac{1}{\ln\left(V_{in}/\Delta\right)}$$

Worst Case: $V_{in} = V_{FS}$

$$\tau << \frac{T_s}{2} \frac{1}{\ln\left(2^B - 1\right)} \approx \frac{0.72 \times T_s}{B}$$

$$R << \frac{1}{2 f_s C} \frac{1}{\ln\left(2^B - 1\right)} \approx \frac{0.72}{B f_s C}$$



Example:

$B = 14, \quad C = 13pF, \quad f_s = 100MHz$

$T_s/\tau >> 19.4$, or $10\tau << T_s/2 \rightarrow R << 40\ \Omega$

Switch On-Resistance

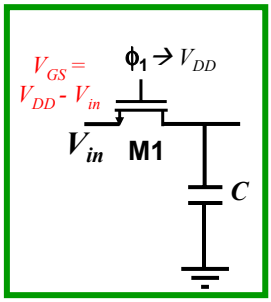
Switch→ MOS operating in triode mode:

$$I_{D(triode)} = \mu C_{ox} \frac{W}{L}\left(V_{GS} - V_{TH} - \frac{V_{DS}}{2}\right) V_{DS}, \qquad \frac{1}{R_{ON}} \cong \left.\frac{dI_{D(triode)}}{dV_{DS}}\right|_{V_{DS} \rightarrow 0}$$

$$R_{ON} = \frac{1}{\mu C_{ox} \frac{W}{L}\left(V_{GS} - V_{th}\right)} = \frac{1}{\mu C_{ox} \frac{W}{L}\left(V_{DD} - V_{th} - V_{in}\right)}$$

Let us call R @ V_{in}=0 R_o then $R_o = \frac{1}{\mu C_{ox} \frac{W}{L}\left(V_{DD} - V_{th}\right)}$

$$R_{ON} = \frac{R_o}{1 - \frac{V_{in}}{V_{DD} - V_{th}}}$$



Sampling Distortion

Simulated 10-Bit ADC &

$T_s/2 = 5\tau$

$V_{DD} - V_{th} = 2V$

$V_{FS} = 1V$

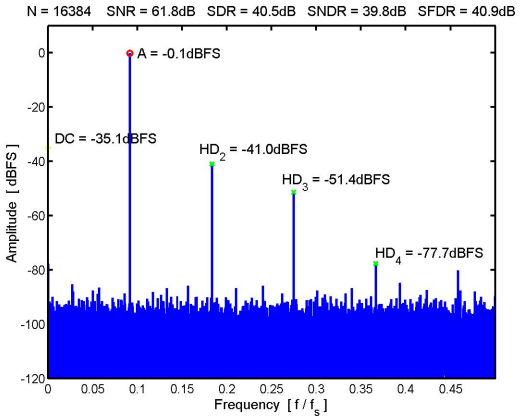
Sampling switch modeled:

$$v_{out} = v_{in}\left(1 - e^{-\frac{T}{2\tau}\left(1-\frac{V_{in}}{V_{DD}-V_{th}}\right)}\right)$$

→Results in

HD2=-41dBFS &

HD3=-51.4dBFS



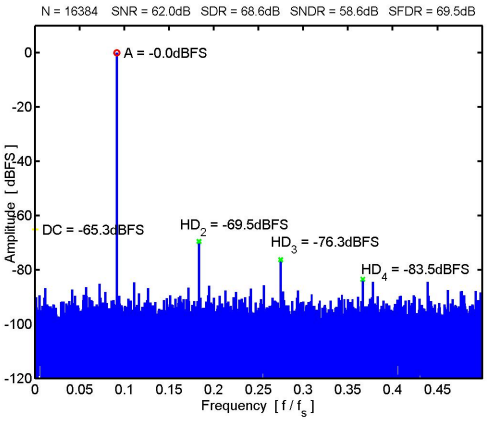
Sampling Distortion

Doubling sampling time (or ½ time constant)
Results in:

HD2 improved from -41dBFS to -70dBFS ~30dB

HD3 improved from -51.4dBFS to -76.3dBFS ~25dB

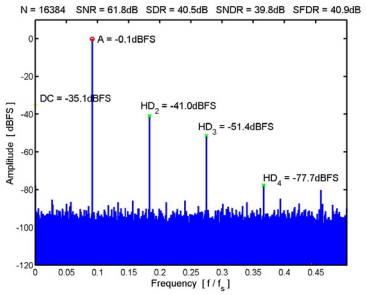
Allowing enough time for the sampling network settling → Reduces distortion due to switch R non-linear behavior to a tolerable level



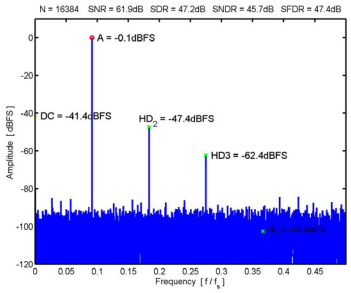
10bit ADC $T_s/2 = 10\tau$

$V_{DD} - V_{th} = 2V$ $V_{FS} = 1V$

Sampling Distortion
Effect of Supply Voltage



10bit ADC & $T_s/2 = 5\tau$
VDD – Vth = 2V V_{FS} = 1V

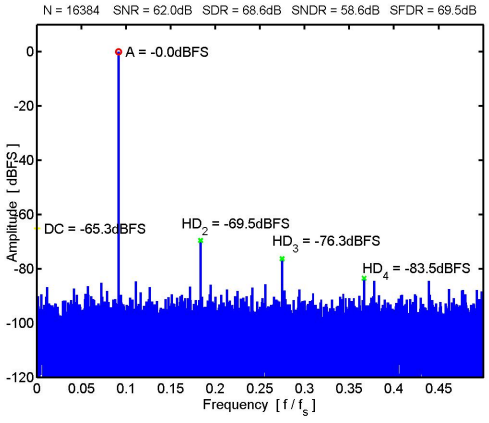


10bit ADC & $T_s/2 = 5\tau$
$V_{DD} - V_{th}$ = 4V V_{FS} = 1V

- Effect of higher supply voltage on sampling distortion
  - → HD3 decrease by $(V_{DD1}/V_{DD2})^2$
  - → HD2 decrease by (V_{DD1}/V_{DD2})

Sampling Distortion

- SFDR → sensitive to sampling distortion - improve linearity by:
  - Larger V_{DD}/V_{FS} ?
    - →Decreased dynamic range if V_{DD} const.
  - Larger switches?
    - Issue:
      - → Increased switch charge injection
      - → Increased nonlinear $S\&D$ junction cap.
  - Complementary switch
  - Constant & max. $V_{GS} \neq f(V_{in})$



10bit ADC T_s/τ = **20**
$V_{DD} - V_{th}$ = 2V V_{FS} = 1V

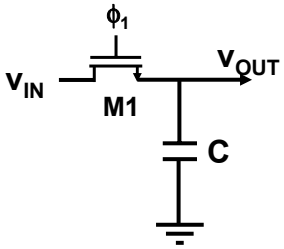
Practical Sampling Summary So Far!

- kT/C noise

$$C \geq 12 k_B T \frac{2^{2B}}{V_{FS}{}^2}$$

- Finite R_{sw} → limited bandwidth

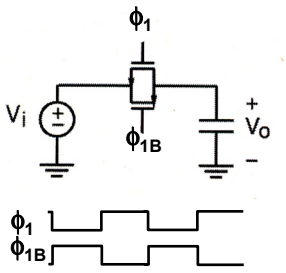
$$R << \frac{0.72}{B f_s C}$$

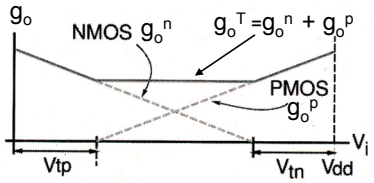


- $g_{sw} = f(V_{in})$ → distortion

$$g_{ON} = g_o\left(1 - \frac{V_{in}}{V_{DD} - V_{th}}\right) \quad \text{for} \quad g_o = \mu C_{ox}\frac{W}{L}(V_{DD} - V_{th})$$

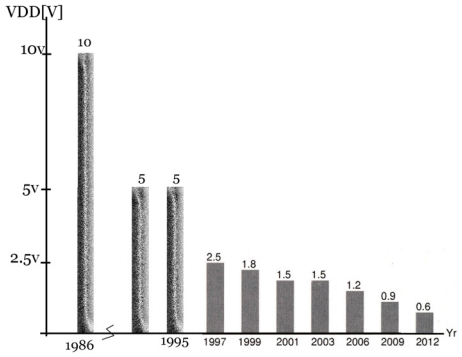
Sampling: Use of Complementary Switches





- Complementary n & p switch advantages:
  - ✓Increase in the overall conductance
  - ✓Linearize the switch conductance for the range $|V_{th}{}^p| < Vin < Vdd - |V_{th}{}^n|$

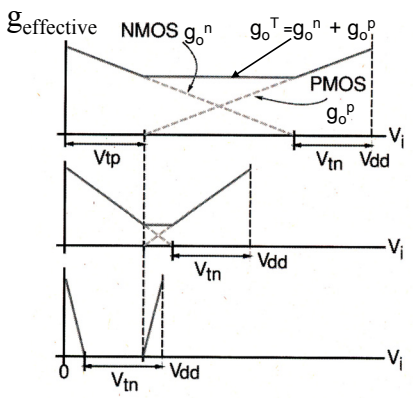
Complementary Switch Issues
Supply Voltage Evolution

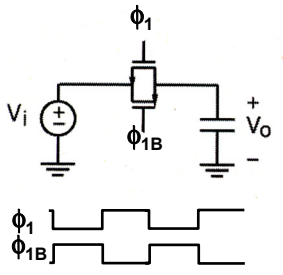


- Supply voltage has scaled down with technology scaling
- Threshold voltages do not scale accordingly

Ref: A. Abo et al, "A 1.5-V, 10-bit, 14.3-MS/s CMOS Pipeline Analog-to-Digital Converter," JSSC May 1999, pp. 599.

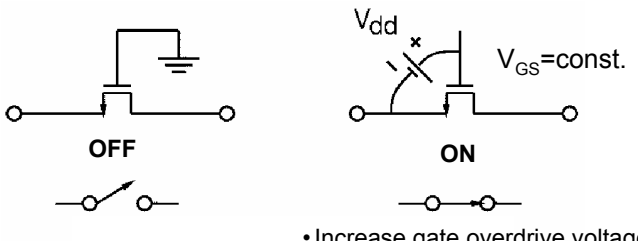
Complementary Switch
Effect of Supply Voltage Scaling





•As supply voltage scales down input voltage range for constant g_o shrinks
→ Complementary switch not effective when V_{DD} becomes comparable to $2xV_{th}$

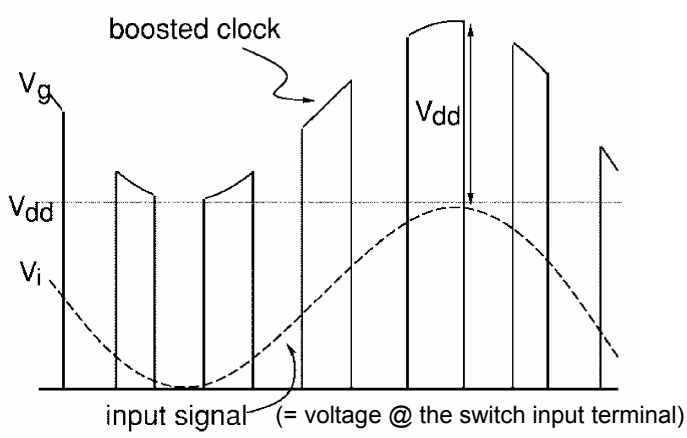
Boosted & Constant V_{GS} Sampling



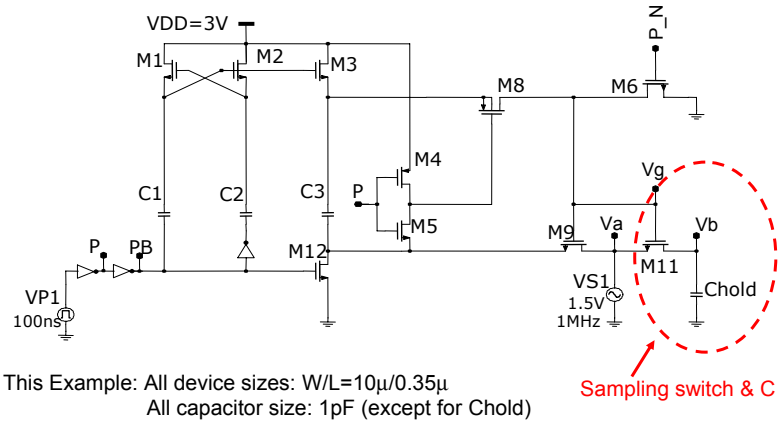
- Gate voltage V_{GS} =low
  - ➢ Device off
  - ➢ Beware of signal feedthrough due to parasitic capacitors

- Increase gate overdrive voltage as much as possible + keep V_{GS} constant
  - ➢ Switch overdrive voltage independent of signal level
  - ➢ Error due to finite R_{ON} linear (to 1st order)
  - ➢ Lower R_{on} → lower time constant

Constant V_{GS} Sampling



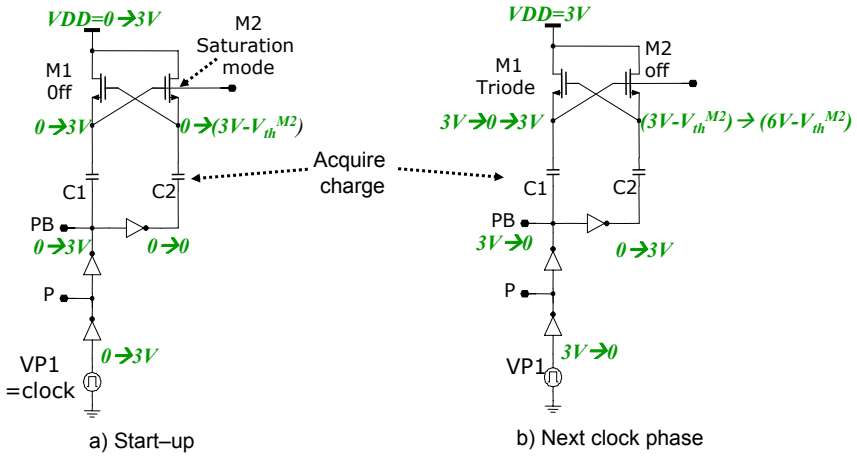
Constant V_{GS} Sampling Circuit



This Example: All device sizes: W/L=10µ/0.35µ
All capacitor size: 1pF (except for Chold)
Note: Each critical switch requires a separate clock booster

Ref: A. Abo et al, "A 1.5-V, 10-bit, 14.3-MS/s CMOS Pipeline Analog-to-Digital Converter," JSSC May 1999, pp. 599.

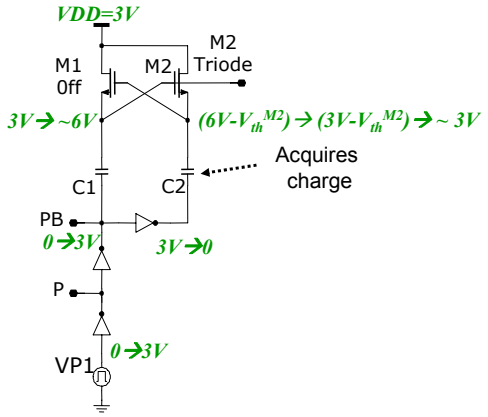
Clock Voltage Doubler



a) Start–up

b) Next clock phase

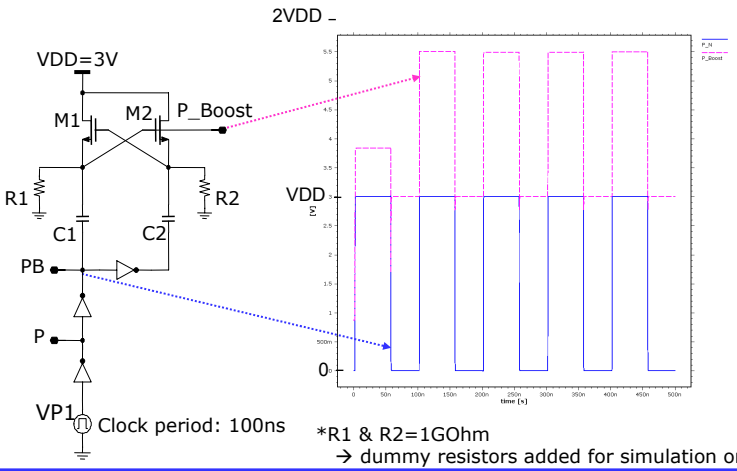
Clock Voltage Doubler



c) Next clock phase

- Both C1 & C2 → charged to VDD after one clock cycle
- Note that bottom plate of C1 & C2 is either 0 or VDD while top plates are at VDD or 2VDD

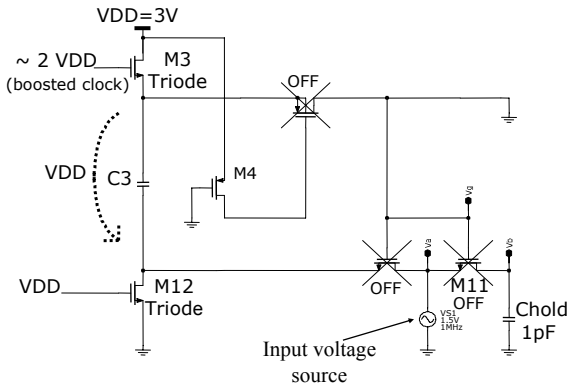
Clock Voltage Doubler



Clock period: 100ns

*R1 & R2=1GOhm
→ dummy resistors added for simulation only

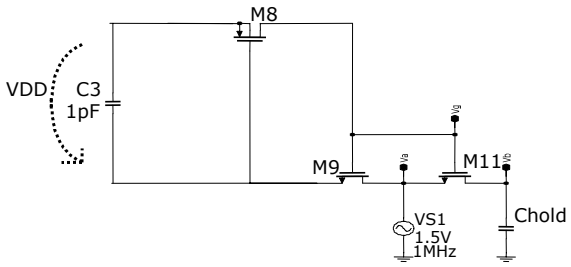
Constant V_{GS} Sampler: Φ Low



- Sampling switch M11 is OFF

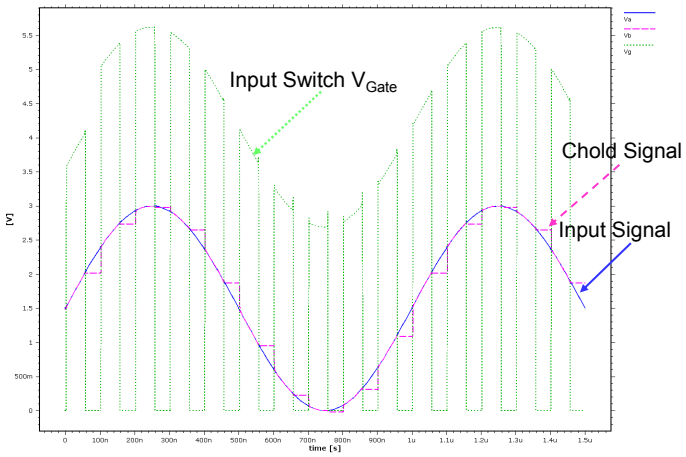
- C3 charged to ~VDD

Constant V_{GS} Sampler: Φ High



- C3 previously charged to VDD
- M8 & M9 are on: C3 across G-S of M11
- M11 on with constant VGS = VDD

Constant V_{GS} Sampling



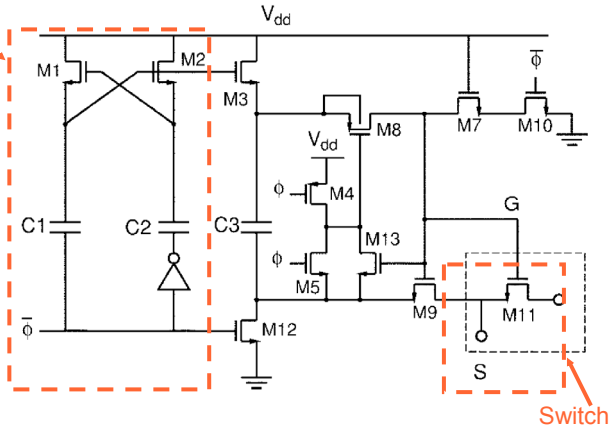
Boosted Clock Sampling Complete Circuit

Clock Multiplier

M13 added for reliability

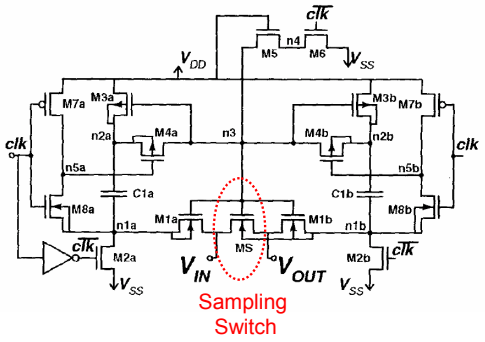
Remaining issues:

- V_{GS} constant only for $V_{in} < V_{out}$
- Nonlinearity due to Vth dependence of M11on body-source voltage
- Choice of size of C3 …..



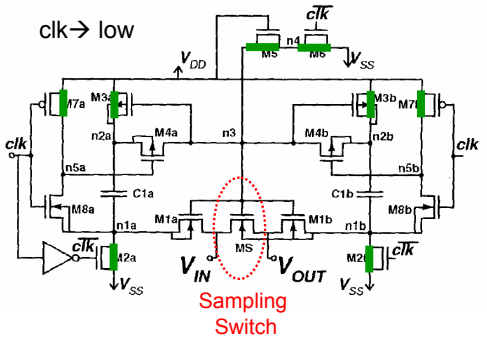
Ref: A. Abo et al, "A 1.5-V, 10-bit, 14.3-MS/s CMOS Pipeline Analog-to-Digital Converter," JSSC May 1999, pp. 599.

Advanced Clock Boosting Technique



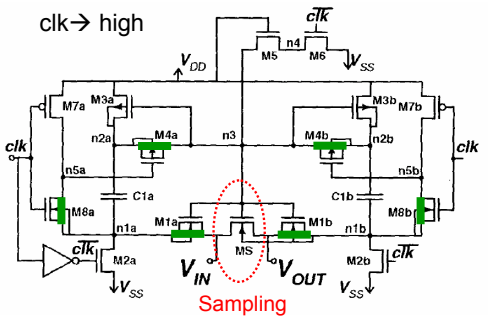
Ref: M. Waltari et al., "A self-calibrated pipeline ADC with 200MHz IF-sampling frontend," ISSCC 2002, Dig. Tech. Papers, pp. 314

Advanced Clock Boosting Technique



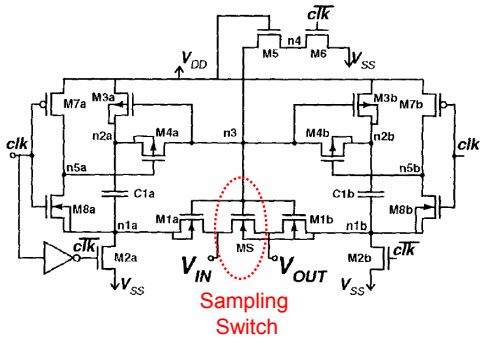
- clk→ low
  - Capacitors C1a & C1b → charged to VDD
  - MS → off
  - Hold mode

Advanced Clock Boosting Technique



- clk→ high
  - Top plate of C1a & C1b connected to gate of sampling switch
  - Bottom plate of C1a connected to V_{IN}
  - Bottom plate of C1b connected to V_{OUT}
  - VGS & VGD of MS both @ VDD & ac signal on G of MS → average of V_{IN} & V_{OUT}

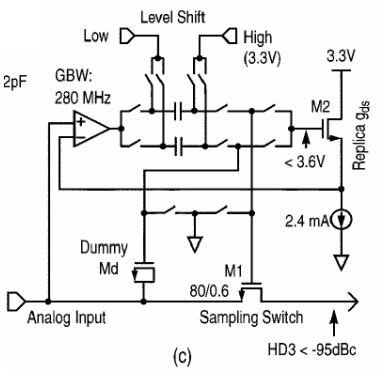
Advanced Clock Boosting Technique



Ref: M. Waltari et al., "A self-calibrated pipeline ADC with 200MHz IF-sampling frontend," ISSCC 2002, Dig. Tech. Papers, pp. 314

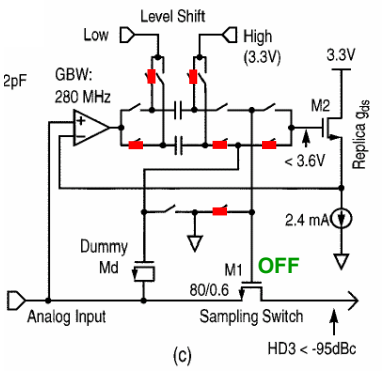
- Gate tracks *average* of input and output, reduces effect of I·R drop at high frequencies
- Bulk also tracks signal ⇒ reduced body effect (technology used allows connecting bulk to S)
- Reported measured SFDR = 76.5dB at f_{in}=200MHz

Constant Conductance Switch



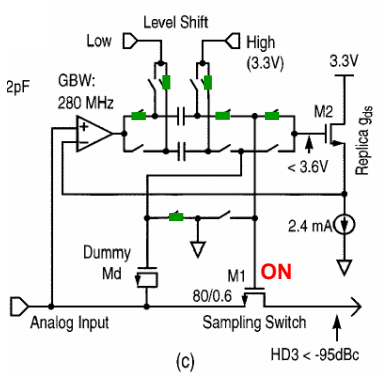
Ref: H. Pan et al., "A 3.3-V 12-b 50-MS/s A/D converter in 0.6um CMOS with over 80-dB SFDR," *IEEE J. Solid-State Circuits*, pp. 1769-1780, Dec. 2000

Constant Conductance Switch



Ref: H. Pan et al., "A 3.3-V 12-b 50-MS/s A/D converter in 0.6um CMOS with over 80-dB SFDR," *IEEE J. Solid-State Circuits*, pp. 1769-1780, Dec. 2000

Constant Conductance Switch



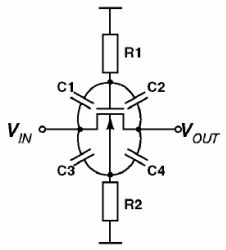
M2→ Constant current
→ constant g_{ds}

M1→ replica of M2
& same VGS
as M2
→ M1 also
constant g_{ds}

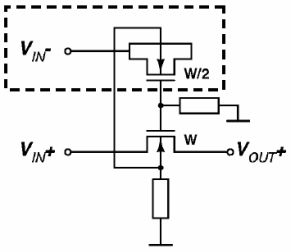
- Note: Authors report requirement of 280MHz GBW for the opamp for 12bit 50Ms/s ADC
- Also, opamp common-mode compliance for full input range required

Ref: H. Pan et al., "A 3.3-V 12-b 50-MS/s A/D converter in 0.6um CMOS with over 80-dB SFDR," *IEEE J. Solid-State Circuits*, pp. 1769-1780, Dec. 2000

Switch Off-Mode Feedthrough Cancellation



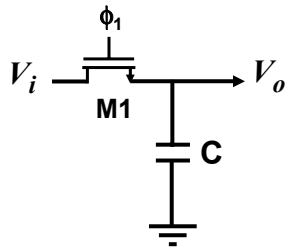
High-pass feedthrough paths past an open switch



Feedthrough cancellation with a dummy switch

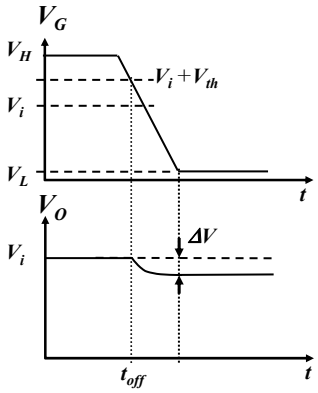
Ref: M. Waltari et al., "A self-calibrated pipeline ADC with 200MHz IF-sampling frontend," ISSCC 2002, Dig. Techn. Papers, pp. 314

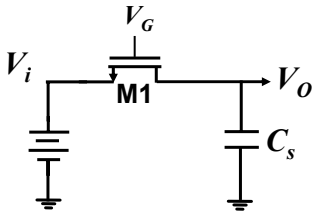
Practical Sampling



- $R_{sw} = f(V_i) \rightarrow$ distortion
- Switch charge injection & clock feedthrough

Sampling Switch Charge Injection & Clock Feedthrough
Switching from Track to Hold

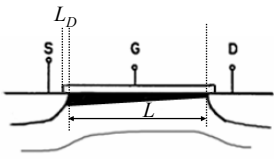




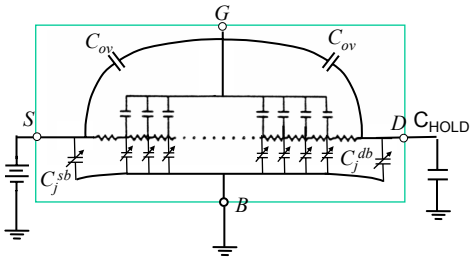
- First assume V_i is a DC voltage
- When switch turns off → offset voltage induced on C_s
- Why?

Sampling
Switch Charge Injection

MOS xtor operating in triode region
Cross section view

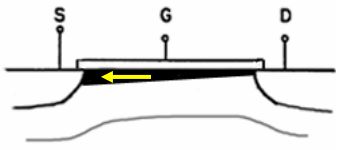


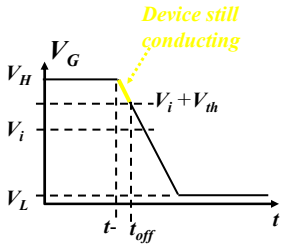
Distributed channel resistance &
gate & junction capacitances



- Channel → distributed RC network formed between G,S, and D
- Channel to substrate junction capacitance → distributed & voltage dependant
- Drain/Source junction capacitors to substrate → voltage dependant
- Over-lap capacitance $C_{ov} = L_D x W x C_{ox}'$ associated with G-S & G-D overlap

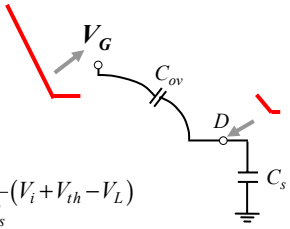
Switch Charge Injection
Slow Clock

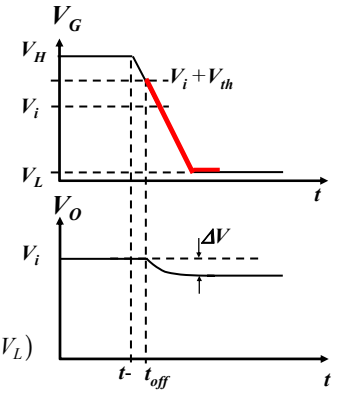




- Slow clock→ clock fall time >> device speed
  → During the period (t- to t_{off}) current in channel discharges channel charge into low impedance signal source
- Only source of error → Clock feedthrough from C_{ov} to C_s

Switch Clock Feedthrough Slow Clock





$$\Delta V = -\frac{C_{ov}}{C_{ov}+C_s}(V_i+V_{th}-V_L)$$

$$\approx -\frac{C_{ov}}{C_s}(V_i+V_{th}-V_L)$$

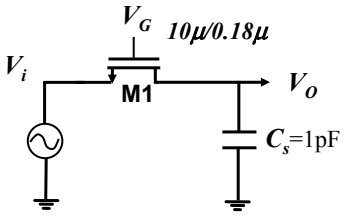
$$V_o = V_i + \Delta V$$

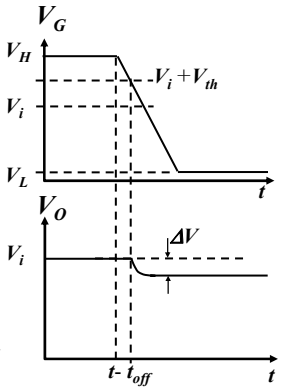
$$V_o = V_i - \frac{C_{ov}}{C_s}(V_i+V_{th}-V_L) = V_i\left(1-\frac{C_{ov}}{C_s}\right) - \frac{C_{ov}}{C_s}(V_{th}-V_L)$$

$$V_o = V_i(1+\varepsilon)+V_{os}$$

$$where\ \varepsilon = -\frac{C_{ov}}{C_s};\ V_{os} = -\frac{C_{ov}}{C_s}(V_{th}-V_L)$$

Switch Charge Injection & Clock Feedthrough Slow Clock- Example





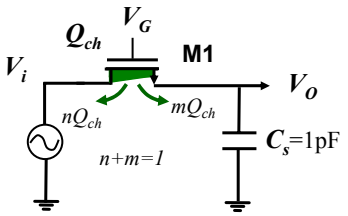
$$C'_{ov} = 0.1fF/\mu \quad C_{ox} = 9fF/\mu^2 \quad V_{th} = 0.4V \quad V_L = 0$$

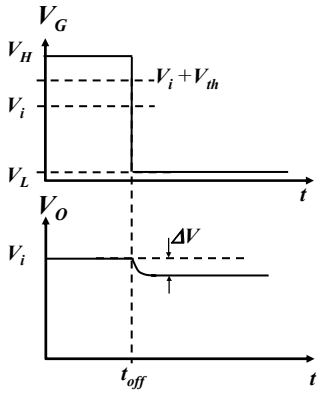
$$\varepsilon = -\frac{C_{ov}}{C_s} = -\frac{10\mu x 0.1fF/\mu}{1pF} = -.1\%$$

$$Allowing\ \varepsilon = 1/2LSB \rightarrow ADC\ resolution <\sim 9bit$$

$$V_{os} = -\frac{C_{ov}}{C_s}(V_{th}-V_L) = -0.4mV$$

Switch Charge Injection & Clock Feedthrough Fast Clock





- Sudden gate voltage drop → no gate voltage to establish current in channel → channel charge has no choice but to escape out towards S & D

Switch Charge Injection & Clock Feedthrough Fast Clock

Clock Fall-Time << Device Speed:

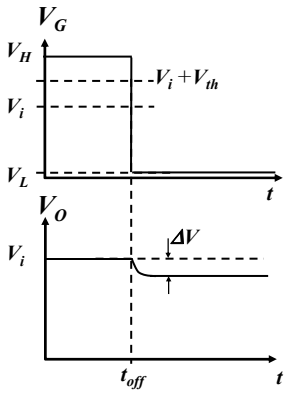
$$\Delta V_o = -\frac{C_{ov}}{C_{ov}+C_s}(V_H - V_L) - \frac{1}{2}\times\frac{Q_{ch}}{C_s}$$

$$\approx -\frac{C_{ov}}{C_{ov}+C_s}(V_H - V_L) - \frac{1}{2}\times\frac{WC_{ox}L\left((V_H - V_i - V_{th})\right)}{C_s}$$

$$V_o = V_i(1+\varepsilon) + V_{os}$$

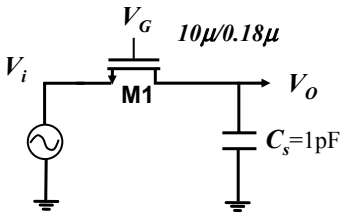
$$where\ \varepsilon = \frac{1}{2}\times\frac{WC_{ox}L}{C_s}$$

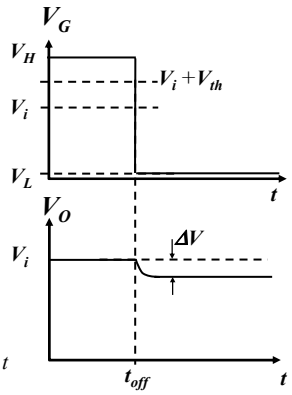
$$V_{os} = -\frac{C_{ov}}{C_s}(V_H - V_L) - \frac{1}{2}\times\frac{WC_{ox}L(V_H - V_{th})}{C_s}$$



- For simplicity it is assumed channel charge divided equally between S & D
- Source of error → channel charge transfer + clock feedthrough via C_{ov} to C_s

Switch Charge Injection & Clock Feedthrough Fast Clock- Example



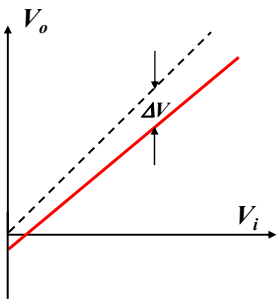


$$C_{ov}=0.1\frac{fF}{\mu},\ C_{ox}=9\frac{fF}{\mu^2},\ V_{th}=0.4V, V_{DD}=1.8V,\ V_L=0$$

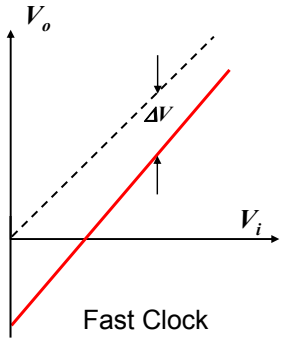
$$\varepsilon=1/2\frac{WLC_{ox}}{C_s}=\frac{10\mu x0.18\mu x9fF/\mu^2}{1pF}=1.6\%\rightarrow\sim 5-bit$$

$$V_{os}=-\frac{C_{ov}}{C_s}(V_H-V_L)-\frac{1}{2}\times\frac{WC_{ox}L(V_H-V_{th})}{C_s}=-1.8mV-14.6mV=-16.4mV$$

Switch Charge Injection & Clock Feedthrough Slow Clock versus Fast Clock

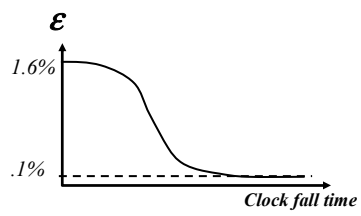


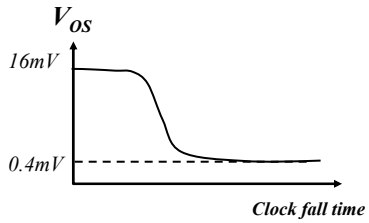
Slow Clock



Fast Clock

Switch Charge Injection & Clock Feedthrough Example-Summary





Error function of:

- → Clock fall time
- → Input voltage level
- → Source impedance
- → Sampling capacitance size
- → Switch size
  - 🗝 Clock fall/rise should be controlled not to be faster (sharper) than necessary

Switch Charge Injection Error Reduction

- How do we reduce the error?
  → Reduce switch size to reduce channel charge?

$$\Delta V_o = -\frac{1}{2}\frac{Q_{ch}}{C_s} \downarrow$$

$$\tau = R_{ON}C_s = \frac{C_s}{\mu C_{ox}\frac{W}{L}(V_{GS}-V_{th})} \uparrow \qquad (note: \frac{T_s}{2} = k\tau)$$

Consider the figure of merit (FOM):

$$FOM = \frac{1}{\tau \times \Delta V_o} \approx \frac{\mu C_{ox}\frac{W}{L}(V_{GS}-V_{th})}{C_s} \times 2 \times \frac{C_s}{WC_{ox}L\left((V_H - V_i - V_{th})\right)}$$

$$\rightarrow FOM \propto \mu / L^2$$

- ❖ Reducing switch size increases τ → increased distortion→ not a viable solution
- ❖ Small τ and small ΔV → use minimum chanel length (mandated by technology)
- ❖ For a given technology τ x ΔV ~ constant

Sampling Switch Charge Injection & Clock Feedthrough Summary

- Extra charge injected onto sampling capacitor @ switch device turn-off
  - Channel charge injection
  - Clock feedthrough to C_s via C_{ov}
- Issues due to charge injection & clock feedthrough:
  - DC offset induced on hold C
  - Input dependant error voltage → distortion
- Solutions:
  - Complementary switch?
  - Addition of dummy switches?
  - Bottom-plate sampling?