EE247
Lecture 16

- **DAC Converters** (continued)
  - DAC design considerations
  - Self calibration techniques
    - Current copiers
    - Dynamic element matching
  - DAC reconstruction filter
- **ADC Converters**
  - Sampling
    - Sampling switch considerations
      - Thermal noise due to switch resistance
      - Sampling switch bandwidth limitations
      - Switch induced distortion
        - Sampling switch conductance dependence on input voltage
        - Clock voltage boosters

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. SC-21, NO. 6, DECEMBER 1986

An 80-MHz 8-bit CMOS D/A Converter

TAKAHIRO MIKI, YASUYUKI NAKAMURA, MASAO NAKAYA, SOTOJU ASAI,
YOICHI AKASAKA, AND YASUTAKA HORIBA

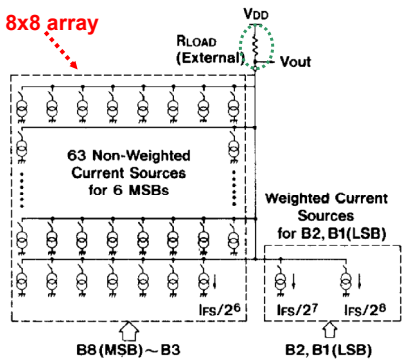


Fig. 1. Basic architecture of the DAC.

2μ tech., 5Vsupply
6+2 segmented

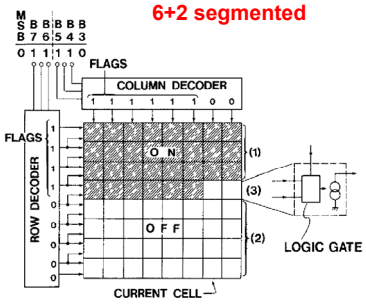


Fig. 2. Two-step decoding.

Current-Switched DACs in CMOS

Assumptions:
RxI small compared to transistor gate-overdrive
To simplify analysis: Initially, all device currents assumed to be equal to *I*

$$V_{GS_{M2}} = V_{GS_{M1}} - 4RI$$

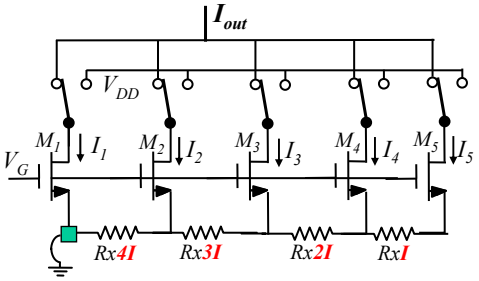
$$V_{GS_{M3}} = V_{GS_{M1}} - 7RI$$

$$V_{GS_{M4}} = V_{GS_{M1}} - 9RI$$

$$V_{GS_{M5}} = V_{GS_{M1}} - 10RI$$

$$I_2 = k\left(V_{GS_{M2}} - V_{th}\right)^2$$

$$I_2 = I_1\left(1 - \frac{4RI}{V_{GS_{M1}} - V_{th}}\right)^2$$



Example: 5 unit element current sources

Current-Switched DACs in CMOS

$$I_2 = k\left(V_{GS_{M2}} - V_{th}\right)^2 = I_1\left(1 - \frac{4RI}{V_{GS_{M1}} - V_{th}}\right)^2$$

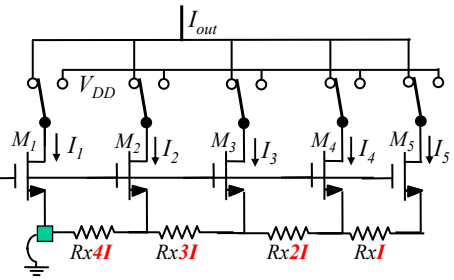
$$g_{m_{M1}} = \frac{2I_1}{V_{GS_{M1}} - V_{th}}$$

$$\rightarrow I_2 = I_1\left(1 - \frac{4Rg_{m_{M1}}}{2}\right)^2 \approx I_1\left(1 - 4Rg_{m_{M1}}\right)$$

$$\rightarrow I_3 = I_1\left(1 - \frac{7Rg_{m_{M1}}}{2}\right)^2 \approx I_1\left(1 - 7Rg_{m_{M1}}\right)$$

$$\rightarrow I_4 = I_1\left(1 - \frac{9Rg_{m_{M1}}}{2}\right)^2 \approx I_1\left(1 - 9Rg_{m_{M1}}\right)$$

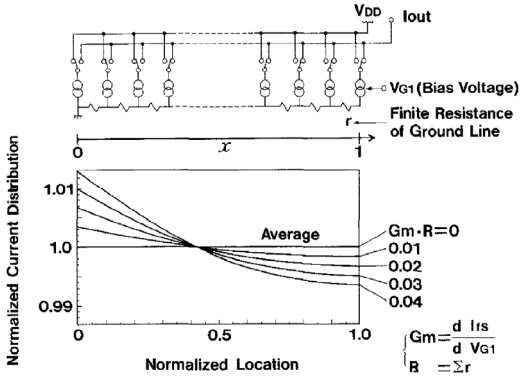
$$\rightarrow I_5 = I_1\left(1 - \frac{10Rg_{m_{M1}}}{2}\right)^2 \approx I_1\left(1 - 10Rg_{m_{M1}}\right)$$



Example: 5 unit element current sources

→ Desirable to have g_m small

Two sources of systematic error:
- **Finite current source output resistance**
- **Voltage drop due to finite ground bus resistance**



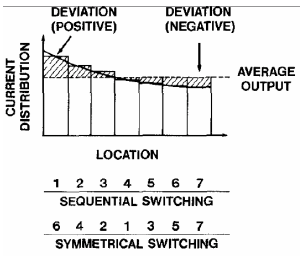
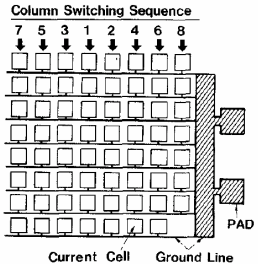
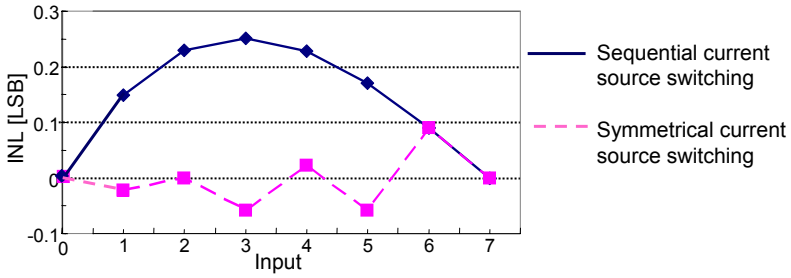


Fig. 9. Symmetrical switching.



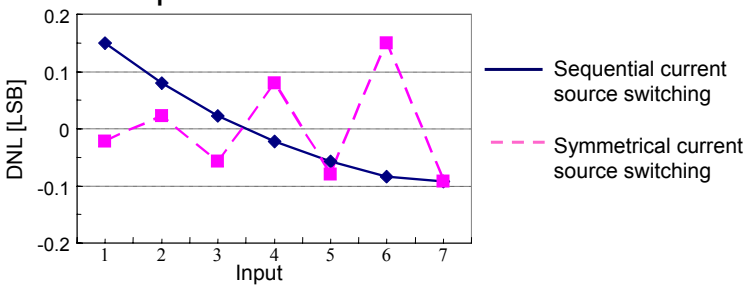
Current-Switched DACs in CMOS
Example: INL of 3-Bit unit element DAC



Example: 7 unit element current source DAC- assume $g_m R = 1/100$

- If switching of current sources arranged sequentially (1-2-3-4-5-6-7)
  → $INL = +0.25LSB$
- If switching of current sources symmetrical (4-3-5-2-6-1-7)
  → $INL = +0.09, -0.058LSB$ → INL reduced by a factor of 2.6

Current-Switched DACs in CMOS
Example: DNL of 7 unit element DAC



Example: 7 unit element current source DAC- assume $g_m R = 1/100$

- If switching of current sources arranged sequentially (1-2-3-4-5-6-7)
  → $DNL_{max} = +0.15LSB$
- If switching of current sources symmetrical (4-3-5-2-6-1-7)

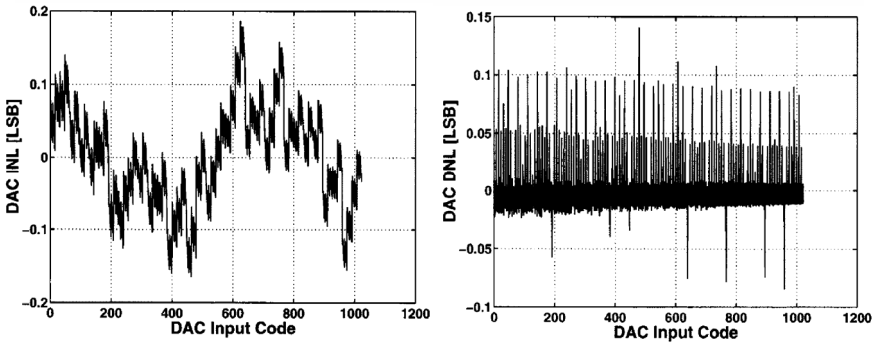
  → $DNL_{max} = +0.15LSB$ → DNL_{max} unchanged

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 36, NO. 3, MARCH 2001 315

A 10-bit 1-GSample/s Nyquist Current-Steering CMOS D/A Converter

(5+5)

Anne Van den Bosch, *Student Member, IEEE*, Marc A. F. Borremans, *Student Member, IEEE*, Michel S. J. Steyaert, *Senior Member, IEEE*, and Willy Sansen, *Fellow, IEEE*

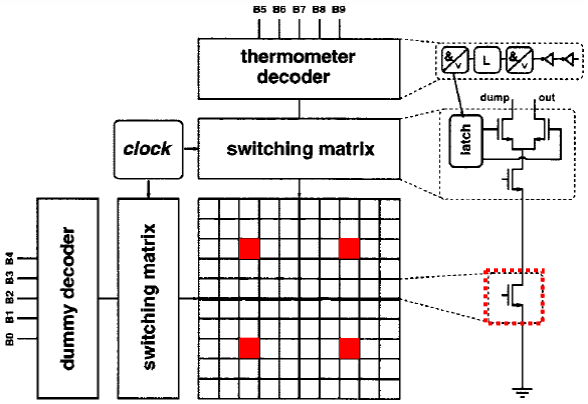


More recent published DAC using symmetrical switching built in 0.35µ/3V analog/1.9V digital, area x10 smaller compared to previous example

A 10-bit 1-GSample/s Nyquist Current-Steering CMOS D/A Converter

Anne Van den Bosch, *Student Member, IEEE*, Marc A. F. Borremans, *Student Member, IEEE*, Michel S. J. Steyaert, *Senior Member, IEEE*, and Willy Sansen, *Fellow, IEEE*

- Layout of Current sources -each current source made of 4 devices in parallel each located in one of the 4 quadrants
- Thermometer decoder used to convert incoming binary digital control for the 5 MSB bits
- Dummy decoder used on the LSB side to match the latency due to the MSB decoder



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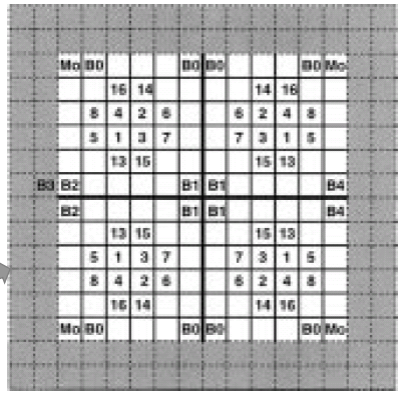
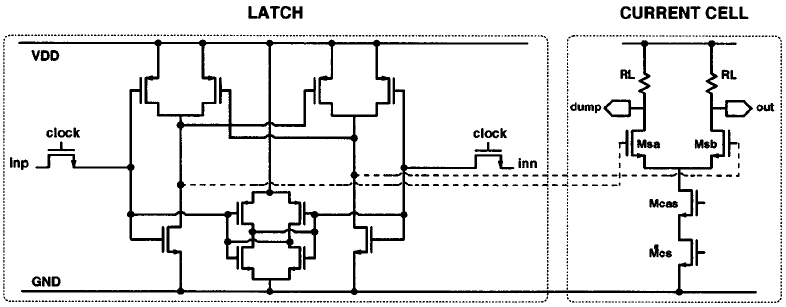
- Current source layout
  - MSB current sources layout in the mid sections of the four quad
  - LSB current sources mostly in the periphery
  - Two rows of dummy current sources added @ the periphery to create identical environment for devices in the center versus the ones on the outer sections



EECS 247- Lecture 16 DAC Design (continued)- Introduction to ADCs © 2008 H.K. Page 10

A 10-bit 1-GSample/s Nyquist Current-Steering CMOS D/A Converter

Anne Van den Bosch, *Student Member, IEEE*, Marc A. F. Borremans, *Student Member, IEEE*, Michel S. J. Steyaert, *Senior Member, IEEE*, and Willy Sansen, *Fellow, IEEE*



- Note that each current cell has its clocked latch and clock signal laid out to be close to its switch to ensure simultaneous switching of current sources
- Special attention paid to the final latch to have the cross point of the complementary switch control signal such that the two switches are not both turned off during transition

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 36, NO. 3, MARCH 2001 315

A 10-bit 1-GSample/s Nyquist Current-Steering CMOS D/A Converter

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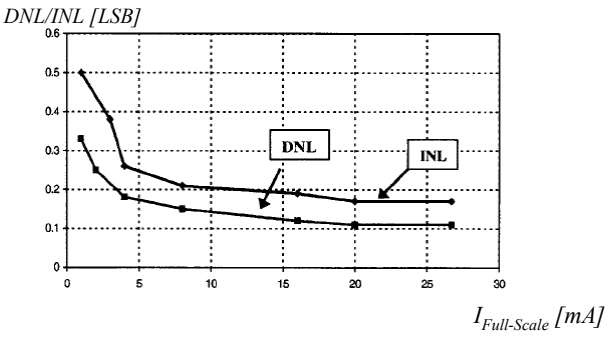


- Measured DNL/INL with current associated with the current cells as variable

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 24, NO. 6, DECEMBER 1989

A Self-Calibration Technique for Monolithic High-Resolution D/A Converters

D. WOUTER J. GROENEVELD, HANS J. SCHOUWENAARS, SENIOR MEMBER, IEEE, HENK A. H. TERMEER, AND CORNELIS A. A. BASTIAANSEN

Called:
Current Copier

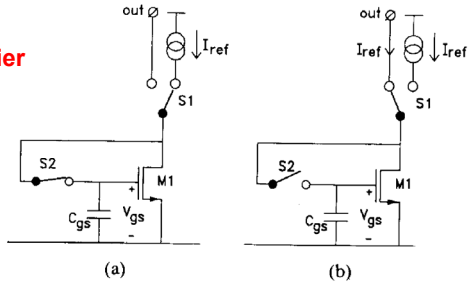
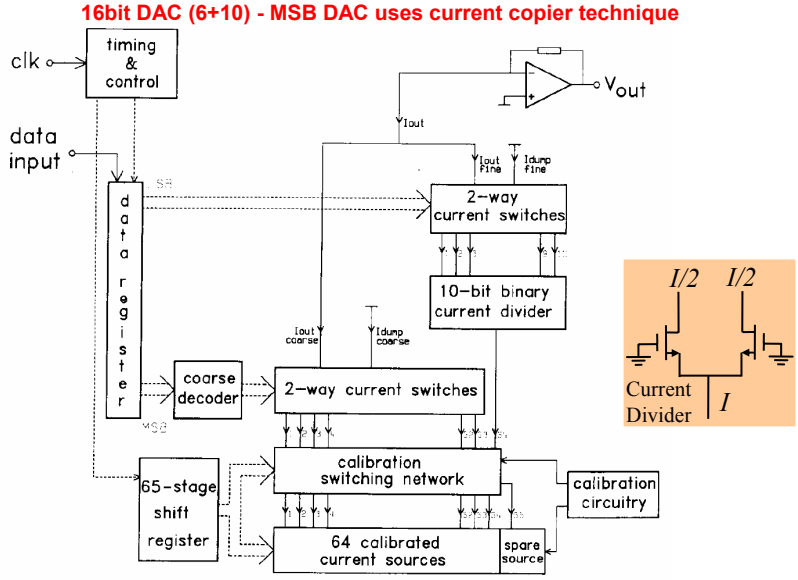


Fig. 2. Calibration principle. (a) Calibration. (b) Operation.

16bit DAC (6+10) - MSB DAC uses current copier technique



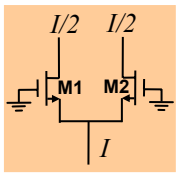
Current Divider Inaccuracy due to Device Mismatch

M1 & M2 mismatch results in the two output currents not being exactly equal:

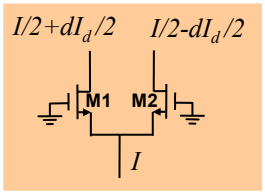
$$I_d = \frac{I_{d1} + I_{d2}}{2}$$

$$\frac{dI_d}{I_d} = \frac{I_{d1} - I_{d2}}{I_d}$$

$$\frac{dI_d}{I_d} = \frac{2}{V_{GS} - V_{th}} \times \left[\left(\frac{d W/L}{W/L} \right) + dV_{th} \right]$$



Ideal Current Divider



Real Current Divider
M1& M2 mismatched

→Problem: Device mismatch could severely limit DAC accuracy
→ Use of dynamic element matching (next few pages)

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. SC-11, NO. 6, DECEMBER 1976

Dynamic Element Matching for High-Accuracy Monolithic D/A Converters

RUDY J. VAN DE PLASSCHE

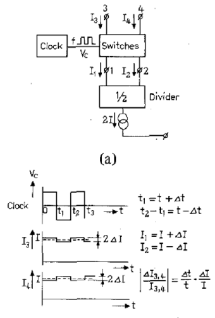


Fig. 2. (a) New current divider schematic diagram. (b) Time dependence of various currents in the new divider.

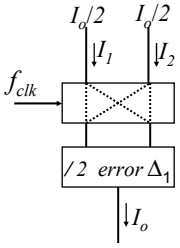
Dynamic Element Matching

During Φ_1

$$I_1^{(1)} = \frac{1}{2} I_o (1+\Delta_1)$$
$$I_2^{(1)} = \frac{1}{2} I_o (1-\Delta_1)$$

During Φ_2

$$I_1^{(2)} = \frac{1}{2} I_o (1-\Delta_1)$$
$$I_2^{(2)} = \frac{1}{2} I_o (1+\Delta_1)$$



Average of I_2:

$$\langle I_2 \rangle = \frac{I_2^{(1)} + I_2^{(2)}}{2}$$
$$= \frac{I_o}{2} \frac{(1-\Delta_1)+(1+\Delta_1)}{2}$$
$$\approx \frac{I_o}{2}$$

Note:
For optimum current division accuracy → clock frequency is divided by two for each finer division
Problem: Frequency of operation drastically reduced

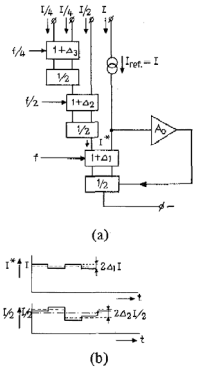
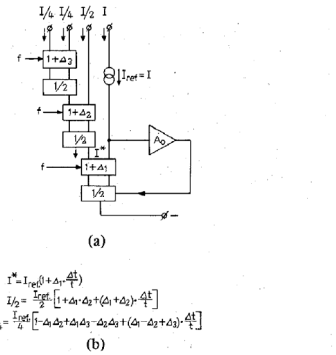


Fig. 4. (a) Binary weighted current network using different switching frequencies. (b) Time dependence of currents flowing in the first and second divider stage.



(a) Binary weighted current network with equal switching frequency. (b) Error analysis results.

Note: What if the same clock frequency is used?

Dynamic Element Matching

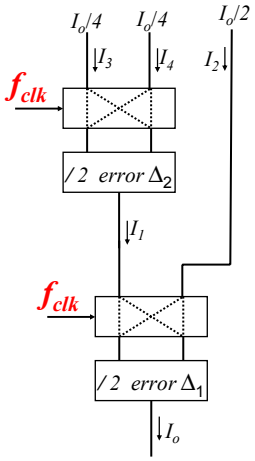
During Φ_1

$$I_1^{(1)} = \tfrac{1}{2} I_o (1+\Delta_1)$$
$$I_2^{(1)} = \tfrac{1}{2} I_o (1-\Delta_1)$$
$$I_3^{(1)} = \tfrac{1}{2} I_1^{(1)} (1+\Delta_2) = \tfrac{1}{4} I_o (1+\Delta_1)(1+\Delta_2)$$

During Φ_2

$$I_1^{(2)} = \tfrac{1}{2} I_o (1-\Delta_1)$$
$$I_2^{(2)} = \tfrac{1}{2} I_o (1+\Delta_1)$$
$$I_3^{(2)} = \tfrac{1}{2} I_1^{(2)} (1-\Delta_2) = \tfrac{1}{4} I_o (1-\Delta_1)(1-\Delta_2)$$

$$\langle I_3 \rangle = \frac{I_3^{(1)} + I_3^{(2)}}{2} = \frac{I_o}{4} \frac{(1+\Delta_1)(1+\Delta_2) + (1-\Delta_1)(1-\Delta_2)}{2} = \frac{I_o}{4}(1+\Delta_1\Delta_2)$$



E.g. $\Delta_1 = \Delta_2 = 1\%$ → matching error is $(1\%)^2 = 0.01\%$

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. SC-11, NO. 6, DECEMBER 1976

Dynamic Element Matching for High-Accuracy Monolithic D/A Converters

RUDY J. VAN DE PLASSCHE

- Bipolar 12-bit DAC using dynamic element matching built in 1976
- Element matching clock frequency 100kHz
- INL <0.25LSB!

12-BIT D/A TEST CHIP

D/A NETWORK DATA	
Resolution:	12 bit
Accuracy:	≤1/4 L.S.B. or $5 \cdot 10^{-5}$ (linearity)
Output current:	2 mA
Temp. Coeff. of output current:	5 ppm/°C
Voltage Coeff. of output current:	1 ppm/V
Chip size:	2.5 × 2.5 mm
Max. clock freq. for dynamic matching:	100 kHz
Power supply:	−15V

20.1 A 3V CMOS 400mW 14b 1.4GS/s DAC for Multi-Carrier Applications

Bernd Schafferer and Richard Adams

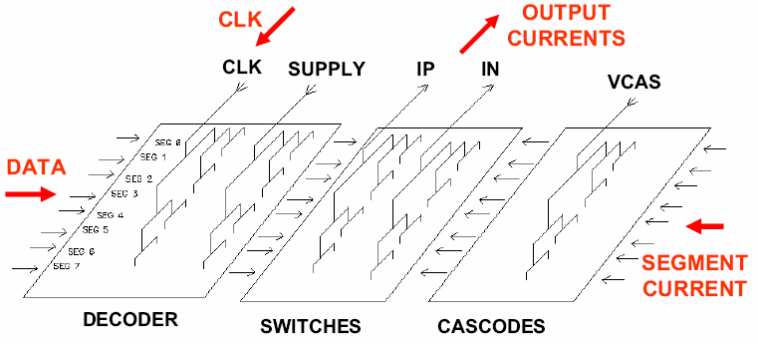
Example: State-of-the-Art current steering DAC

Segmented:
6bit unit-element
8bit binary

Max Sample Frequency	1.4	GSPS
Resolution	14	Bit
DNL	+/- 0.8	LSB
INL	+/- 2.1	LSB
SFDR @ 1.0 GSPS	> 60	dB
IMD @ 1.0 GSPS	> 64	dBc
NSD @ f_{out} = 400MHz	-155	dBm/Hz
Power (Core) @1.4GSPS	200	mW
Power(Total) @ 1.4GSPS	400	mW
Area (Core)	0.8	mm^2
Area (Chip)	6.25	mm^2

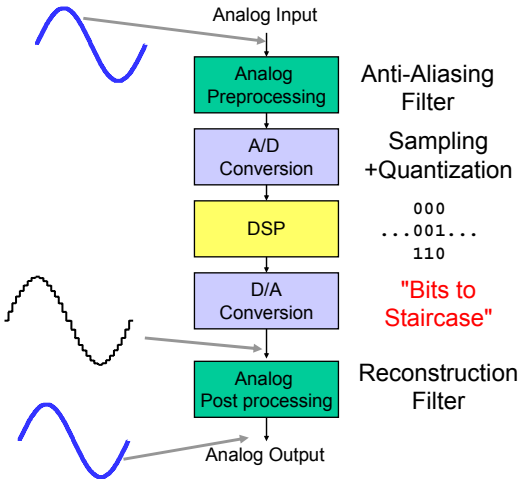
20.1 A 3V CMOS 400mW 14b 1.4GS/s DAC for Multi-Carrier Applications

Layout Tree Structures



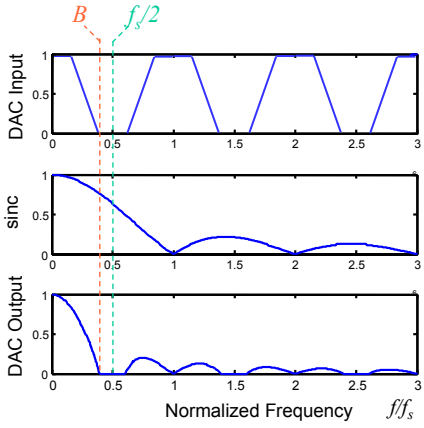
DAC In the Big Picture

- Learned to build DACs
  - Convert the incoming digital signal to analog
- DAC output → staircase form
- Some applications require filtering (smoothing) of DAC output
  → reconstruction filter

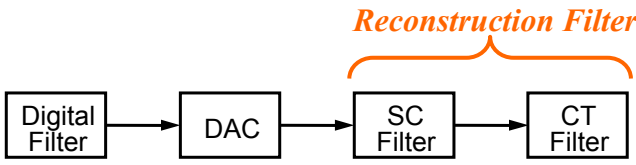


DAC Reconstruction Filter

- Need for and requirements depend on application
- Tasks:
  - Correct for sinc droop
  - Remove "aliases" (stair-case approximation)

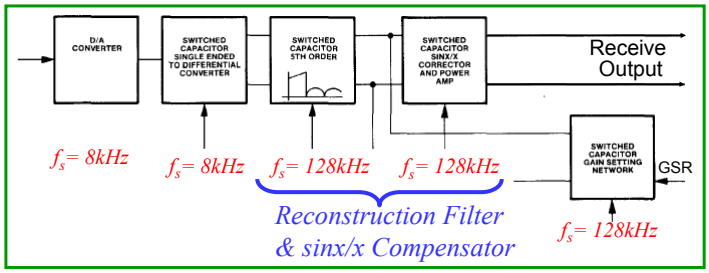


Reconstruction Filter Options



- Reconstruction filter options:
  - Continuous-time filter only
  - CT + SC filter
- SC filter possible only in combination with oversampling (signal bandwidth B << $f_s/2$)
- Digital filter
  - Band limits the input signal → prevent aliasing
  - Could also provide high-frequency pre-emphasis to compensate in-band *sinx/x* amplitude droop associated with the inherent DAC S/H function

DAC Reconstruction Filter
Example: Voice-Band CODEC Receive Path



Note: $f_{sig}^{max} = 3.4kHz$

$f_s^{DAC} = 8kHz$

$\rightarrow sin(\pi f_{sig}^{max} x\ T_s)/(\pi f_{sig}^{max} x T_s)$

$= -2.75$ dB droop due to DAC sinx/x shape

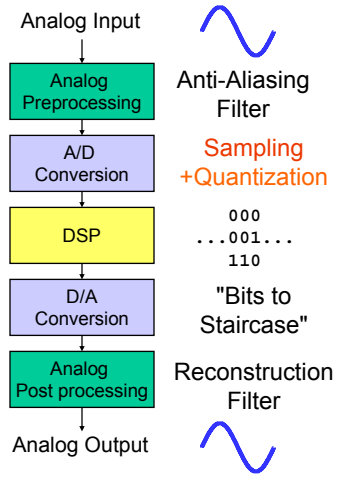
Ref: D. Senderowicz et. al, "A Family of Differential NMOS Analog Circuits for PCM Codec Filter Chip," *IEEE Journal of Solid-State Circuits*, Vol.-SC-17, No. 6, pp.1014-1023, Dec. 1982.

Summary
D/A Converter

- D/A architecture
  - Unit element – complexity proportional to 2^B- excellent DNL
  - Binary weighted- complexity proportional to B- poor DNL
  - Segmented- unit element MSB(B_1)+ binary weighted LSB(B_2)
    - → Complexity proportional ((2^{B1}-1) + B_2) -DNL compromise between the two
- Static performance
  - Component matching
- Dynamic performance
  - Time constants, Glitches
- DAC improvement techniques
  - Symmetrical switching rather than sequential switching
  - Current source self calibration
  - Dynamic element matching
- Depending on the application, reconstruction filter may be needed

What Next?

- ADC Converters:
  - Need to build circuits that "sample“
  - Need to build circuits for amplitude quantization



Analog-to-Digital Converters

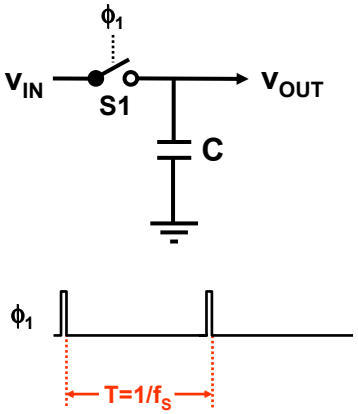
- Two categories:
  - Nyquist rate ADCs → $f_{sig}^{max} \sim 0.5xf_{sampling}$
    - Maximum achievable signal bandwidth higher compared to oversampled type
    - Resolution limited to max. 12-14bits
  - Oversampled ADCs → $f_{sig}^{max} << 0.5xf_{sampling}$
    - Maximum achievable signal bandwidth significantly lower compared to nyquist
    - Maximum achievable resolution high (18 to 20bits!)

MOS Sampling Circuits

Ideal Sampling

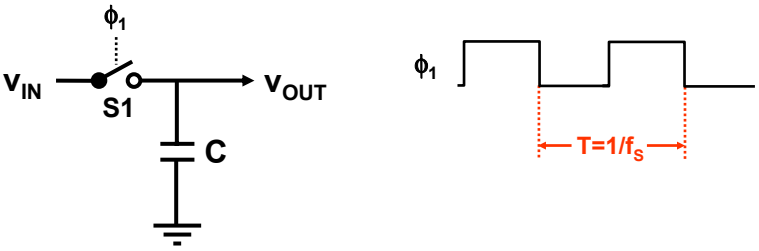
- In an ideal world, zero resistance sampling switches would close for the briefest instant to sample a continuous voltage v_{IN} onto the capacitor C

  →Output Dirac-like pulses with amplitude equal to V_{IN} at the time of sampling



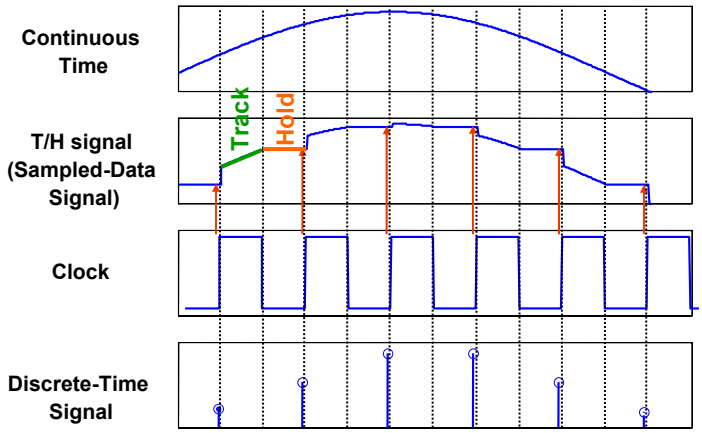
- In practice not realizable!

Ideal Track & Hold Sampling

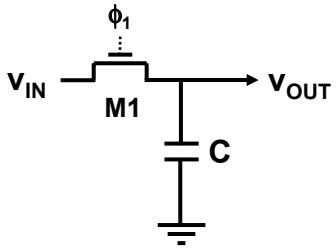


- V_{out} tracks input for ½ clock cycle when switch is closed
- Acquires *exact* value of V_{in} at the instant the switch opens
- "Track and Hold" (T/H) (often called Sample & Hold!)

Ideal T/H Sampling

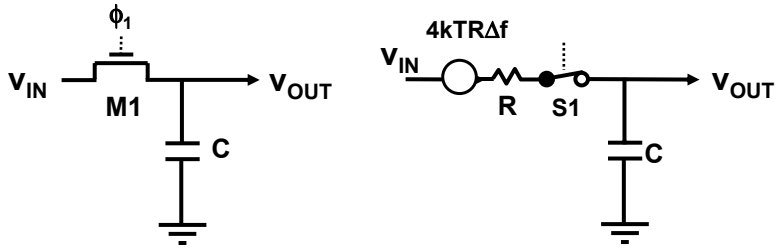


Practical Sampling Issues



- Switch induced noise due to M1 finite channel resistance
- Clock jitter
- Finite R_{sw} → limited bandwidth → finite acquisition time
- $R_{sw} = f(V_{in})$ → distortion
- Switch charge injection & clock feedthrough

Sampling Circuit kT/C Noise



- Switch resistance & sampling capacitor form a low-pass filter
- Noise associated with the switch resistance results in → Total noise variance= kT/C @ the output (see noise analysis in Lecture 1)
- In high resolution ADCs kT/C noise at times dominates overall minimum signal handling capability (power dissipation considerations).

Sampling Network kT/C Noise

For ADCs sampling capacitor size is usually chosen based on having thermal noise smaller or equal or at times larger compared to quantization noise:
Assumption: → Nyquist rate ADC

For a Nyquist rate ADC : Total quantization noise power $\approx \frac{\Delta^2}{12}$

Choose C such that thermal noise level is less (or equal) than Q noise

$$\frac{k_B T}{C} \leq \frac{\Delta^2}{12}$$

$$\rightarrow \quad C \geq 12 k_B T \left(\frac{2^B - 1}{V_{FS}} \right)^2$$

$$\rightarrow \quad \boxed{C \geq 12 k_B T \times \frac{2^{2B}}{{V_{FS}}^2}}$$

Sampling Network kT/C Noise

$$C \geq 12 k_B T \frac{2^{2B}}{V_{FS}{}^2}$$

Required C_{min} as a Function of ADC Resolution		
B	C_{min} (V_{FS} = 1V)	C_{min} (V_{FS} = 0.5V)
8	0.003 pF	0.012 pF
12	0.8 pF	2.4 pF
14	13 pF	52 pF
16	206 pF	824 pF
20	52,800 pF	211,200 pF

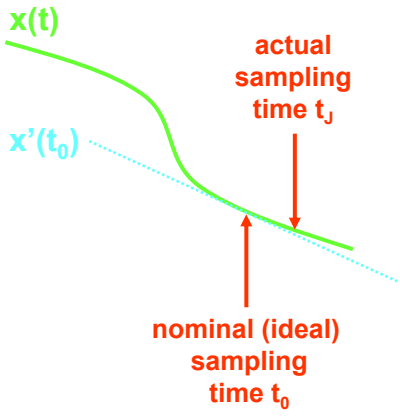
The large area required for C → limit highest achievable resolution for Nyquist rate ADCs
Oversampling results in reduction of required value for C (will be covered in oversampled converter lectures)

Clock Jitter

- So far : clock signal controls sampling instants – which we assumed to be precisely equi-distant in time (period T)
- Real clock generator → some level of variability
- Variability in T causes errors
  - "Aperture Uncertainty" or "Aperture Jitter"
- What is the effect of clock jitter on ADC performance?

Clock Jitter

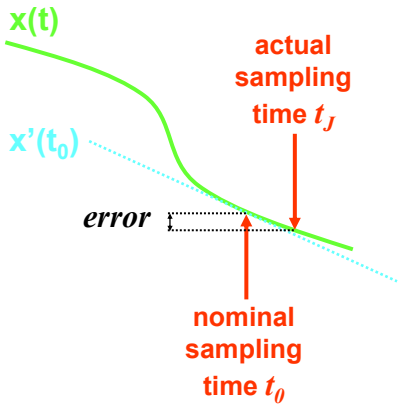
- Sampling jitter adds an error voltage proportional to the product of (t_J-t_0) and the derivative of the input signal at the sampling instant
- Does jitter matter when sampling dc signals ($x'(t_0)$=0)?



Clock Jitter

- The error voltage is

$$e = x'(t_0)(t_J - t_0)$$



Effect of Clock Jitter on Sampling of a Sinusoidal Signal

Sinusoidal input

$Amplitude: \quad A$
$Frequency: \quad f_x$
$Jitter: \quad dt$

$$x(t) = A\sin(2\pi f_x t)$$

$$x'(t) = 2\pi f_x \, A\cos(2\pi f_x t)$$

$$|x'(t)|_{max} \le 2\pi f_x A$$

$Requirement:$

$$|e(t)| \le |x'(t)|_{max} \, dt$$

$$|e(t)| \le 2\pi f_x A dt$$

Worst case

$$A = A_{FS}/2 \qquad f_x = f_s/2$$

$$|e(t)| << \frac{\Delta}{2} \cong \frac{A_{FS}}{2^{B+1}}$$

$$dt << \frac{1}{2^B \pi f_s}$$

# of Bits	f_s	dt <<
12	1 MHz	78 ps
16	20 MHz	0.24 ps
10	1000 MHz	0.3 ps

Law of Jitter

- The worst case looks pretty stringent …
  what about the "average"?
- Let's calculate the mean squared jitter error (variance)
- If we're sampling a sinusoidal signal
  $x(t) = A\sin(2\pi f_x t)$,
  then
  - $x'(t) = 2\pi f_x A\cos(2\pi f_x t)$
  - $E\{[x'(t)]^2\} = 2\pi^2 f_x^2 A^2$
- Assume the jitter has variance $E\{(t_J - t_0)^2\} = \tau^2$

Law of Jitter

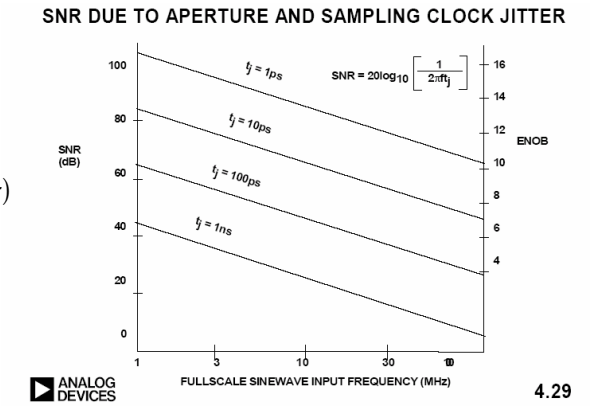
- If x'(t) and the jitter are independent
  - $E\{[x'(t)(t_J-t_0)]^2\} = E\{[x'(t)]^2\}\, E\{(t_J-t_0)^2\}$
- Hence, the jitter error power is

$$\mathbf{E\{e^2\} = 2\pi^2 f_x^2 A^2 \tau^2}$$

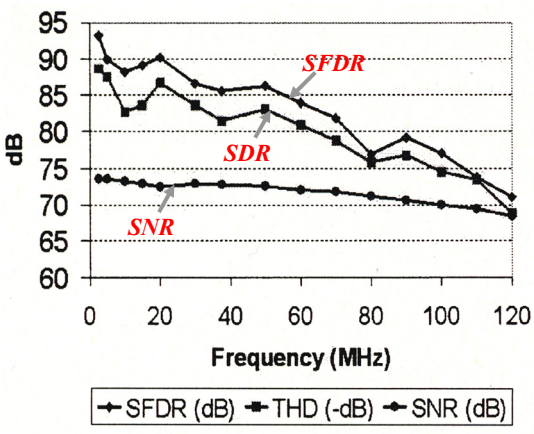
- If the jitter is uncorrelated from sample to sample, this "jitter noise" is white

Law of Jitter

$$DR_{\text{jitter}} = \frac{A^2/2}{2\pi^2 f_x^2 A^2 \tau^2} = \frac{1}{2\pi^2 f_x^2 \tau^2} = -20\log_{10}(2\pi f_x \tau)$$



Example: ADC Spectral Tests



Ref: W. Yang et al., "A 3-V 340-mW 14-b 75-Msample/s CMOS ADC with 85-dB SFDR at Nyquist input," *IEEE J. of Solid-State Circuits,* Dec. 2001

More on Jitter

- In cases where clock signal is provided from off-chip→ have to choose a source with low enough jitter
- On-chip precautions to keep the clock jitter less than single-digit pico-second :
  - Separate supplies as much as possible
  - Separate analog and digital clocks
  - Short inverter chains between clock source and destination
- Few, if any, other analog-to-digital conversion non-idealities have the same symptoms as sampling jitter:
  - RMS noise proportional to input signal frequency
  - RMS noise proportional to input signal amplitude

  →In cases where clock jitter limits the dynamic range, it's easy to tell, but may be difficult to fix...

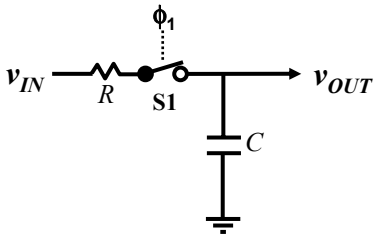
Sampling Acquisition Bandwidth

- The resistance R of switch S1 turns the sampling network into a lowpass filter with finite time constant:

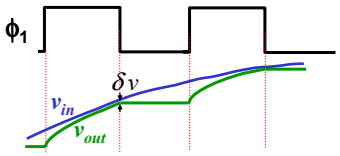
$$\tau = RC$$

- Assuming V_{in} is constant during the sampling period and C is initially discharged

- Need to allow enough time for the output to settle to less than 1 ADC LSB → determines minimum duration for ϕ_1 or maximum clock frequency



$$v_{out}(t) = v_{in}\left(1 - e^{-t/\tau}\right)$$



Sampling: Effect of Switch On-Resistance

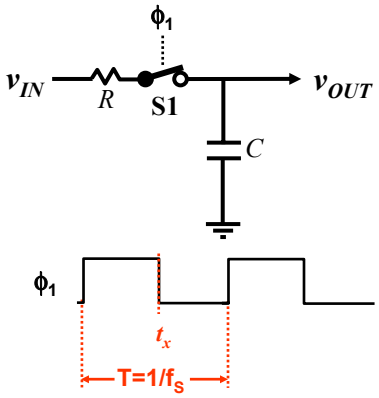
$$V_{in}^{tx} - V_{out}^{tx} << \Delta \quad \text{since} \quad V_{out} = V_{in}\left(1 - e^{-t/\tau}\right)$$

$$\rightarrow V_{in} e^{-T_s/2\tau} << \Delta \quad or \quad \tau << \frac{T_s}{2} \frac{1}{\ln\left(V_{in}/\Delta\right)}$$

Worst Case: $V_{in} = V_{FS}$

$$\tau << \frac{T_s}{2} \frac{1}{\ln\left(2^B - 1\right)} \approx \frac{0.72 \times T_s}{B}$$

$$R << \frac{1}{2 f_s C} \frac{1}{\ln\left(2^B - 1\right)} \approx \frac{0.72}{B f_s C}$$



Example:

$B = 14, \quad C = 13pF, \quad f_s = 100MHz$

$T_s/\tau >> 19.4$, or $10\tau << T_s/2 \rightarrow R << 40\ \Omega$

Switch On-Resistance

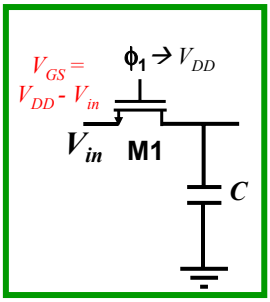
Switch→ MOS operating in triode mode:

$$I_{D(triode)} = \mu C_{ox}\frac{W}{L}\left(V_{GS} - V_{TH} - \frac{V_{DS}}{2}\right)V_{DS}, \qquad \frac{1}{R_{ON}} \cong \left.\frac{dI_{D(triode)}}{dV_{DS}}\right|_{V_{DS}\to 0}$$

$$R_{ON} = \frac{1}{\mu C_{ox}\frac{W}{L}(V_{GS} - V_{th})} = \frac{1}{\mu C_{ox}\frac{W}{L}(V_{DD} - V_{th} - V_{in})}$$

Let us call R @ V_{in}=0 R_o then $R_o = \frac{1}{\mu C_{ox}\frac{W}{L}(V_{DD} - V_{th})}$

$$R_{ON} = \frac{R_o}{1 - \frac{V_{in}}{V_{DD} - V_{th}}}$$



Sampling Distortion

Simulated 10-Bit ADC &

$T_s/2 = 5\tau$

$V_{DD} - V_{th} = 2V$

$V_{FS} = 1V$

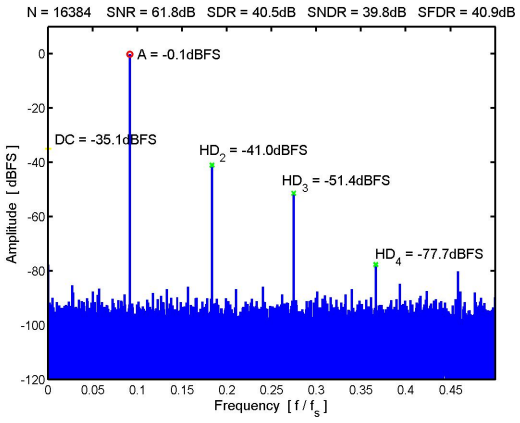
Sampling Switch modeled:

$$v_{out} = v_{in}\left(1 - e^{-\frac{T}{2\tau}\left(1 - \frac{V_{in}}{V_{DD} - V_{th}}\right)}\right)$$

→Results in

HD2=-41dBFS &

HD3=-51.4dBFS



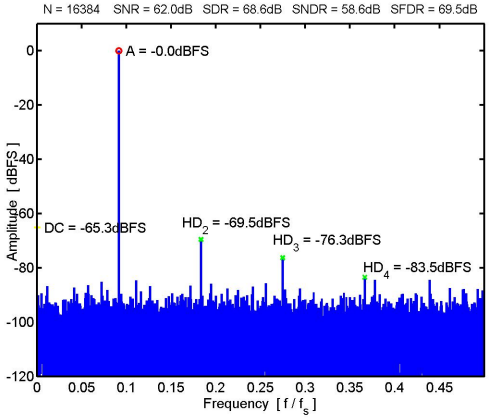
Sampling Distortion

Doubling sampling time (or ½ time constant)
Results in:

HD2 improved from -41dBFS to -70dBFS ~30dB

HD3 improved from -51.4dBFS to -76.3dBFS ~25dB

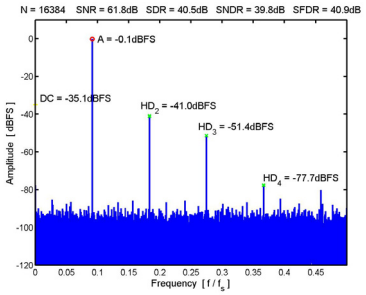
Allowing enough time for the sampling network settling → Reduces distortion due to switch R non-linear behavior to a tolerable level



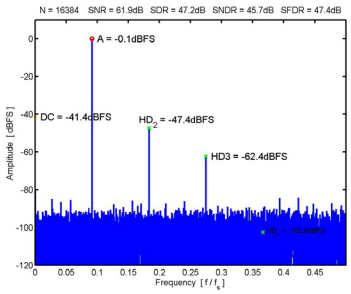
10bit ADC $T_s/2 = 10\,\tau$

$V_{DD} - V_{th} = 2V$ $V_{FS} = 1V$

Sampling Distortion
Effect of Supply Voltage



10bit ADC & $T_s/2 = 5\tau$
VDD – Vth = 2V V_{FS} = 1V

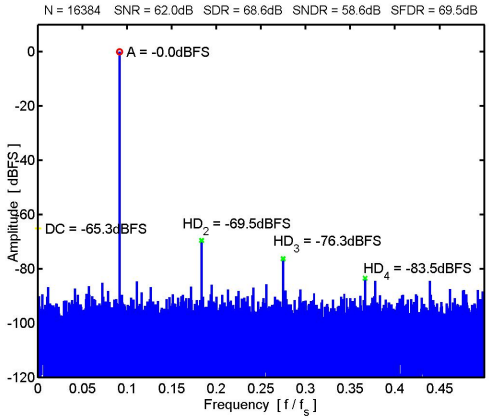


10bit ADC & $T_s/2 = 5\tau$
$V_{DD} - V_{th}$ = 4V V_{FS} = 1V

- Effect of higher supply voltage on sampling distortion
  - → HD3 decrease by $(V_{DD1}/V_{DD2})^2$
  - → HD2 decrease by (V_{DD1}/V_{DD2})

Sampling Distortion

- SFDR → sensitive to sampling distortion - improve linearity by:
  - Larger V_{DD}/V_{FS}
  - Higher sampling bandwidth
- Solutions:
  - Overdesign→ Larger switches Issue:
    - → Increased switch charge injection
    - → Increased nonlinear S &D junction cap.
  - Maximize V_{DD}/V_{FS} →Decreased dynamic range if V_{DD} const.
  - Complementary switch
  - Constant & max. $V_{GS} \neq f(V_{in})$



10bit ADC T_s/τ = **20**
$V_{DD} - V_{th}$ = 2V V_{FS} = 1V

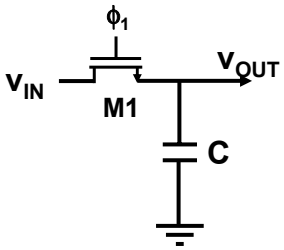
Practical Sampling Summary So Far!

- kT/C noise

$$C \geq 12 k_B T \frac{2^{2B}}{V_{FS}{}^2}$$

- Finite R_{sw} → limited bandwidth

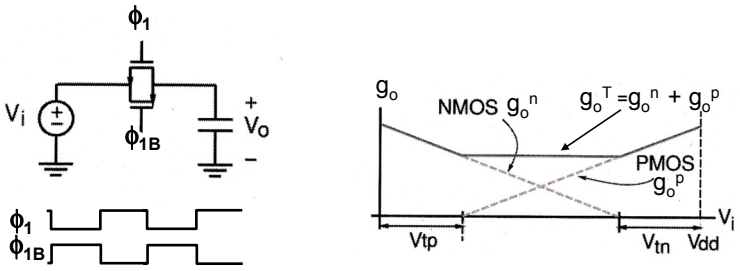
$$R << \frac{0.72}{B f_s C}$$



- $g_{sw} = f(V_{in})$ → distortion

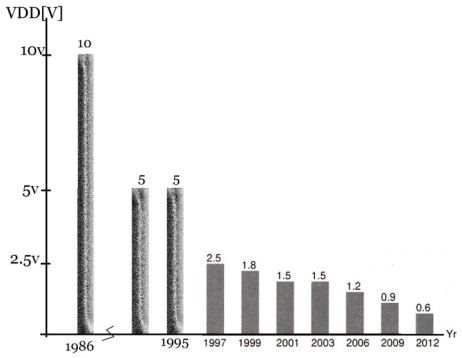
$$g_{ON} = g_o\left(1 - \frac{V_{in}}{V_{DD} - V_{th}}\right) \quad \text{for} \quad g_o = \mu C_{ox} \frac{W}{L}(V_{DD} - V_{th})$$

Sampling: Use of Complementary Switches



- Complementary n & p switch advantages:
  - ✓Increase in the overall conductance
  - ✓Linearize the switch conductance for the range $|V_{th}^p| < Vin < Vdd - |V_{th}^n|$

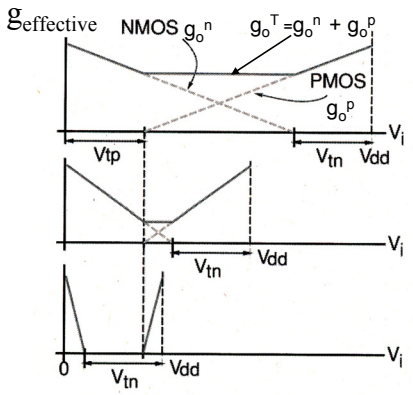
Complementary Switch Issues
Supply Voltage Evolution

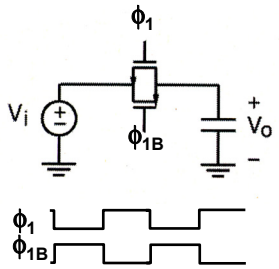


- Supply voltage has scaled down with technology scaling
- Threshold voltages do not scale accordingly

Ref: A. Abo et al, "A 1.5-V, 10-bit, 14.3-MS/s CMOS Pipeline Analog-to-Digital Converter," JSSC May 1999, pp. 599.

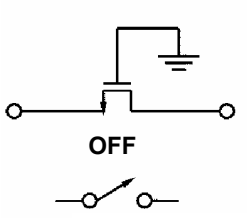
Complementary Switch
Effect of Supply Voltage Scaling

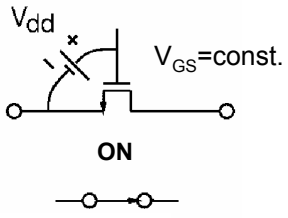




•As supply voltage scales down input voltage range for constant g_o shrinks
→ Complementary switch not effective when V_{DD} becomes comparable to $2xV_{th}$

Boosted & Constant V_{GS} Sampling

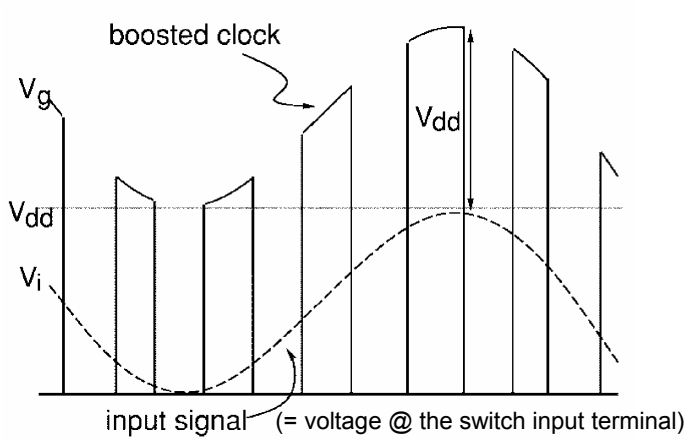




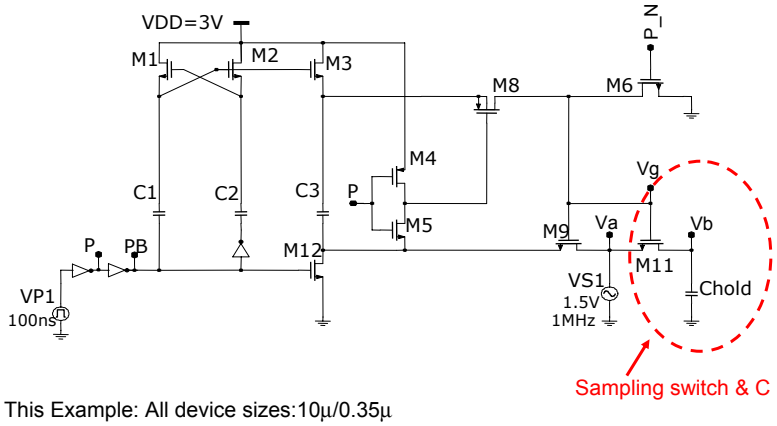
- Gate voltage V_{GS} =low
  - ➢ Device off
  - ➢ Beware of signal feedthrough due to parasitic capacitors

- Increase gate overdrive voltage as much as possible + keep V_{GS} constant
  - ➢ Switch overdrive voltage independent of signal level
  - ➢ Error due to finite R_{ON} linear (to 1st order)
  - ➢ Lower R_{on} → lower time constant

Constant V_{GS} Sampling

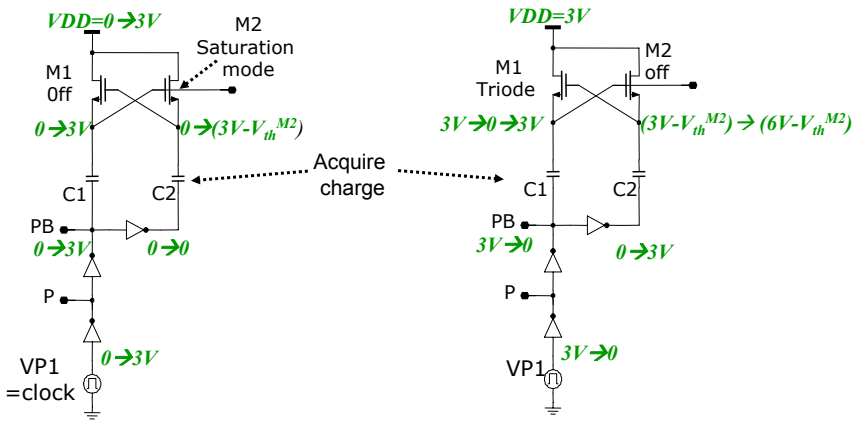


Constant V_{GS} Sampling Circuit



This Example: All device sizes:10µ/0.35µ
All capacitor size: 1pF (except for Chold)
Note: Each critical switch requires a separate clock booster

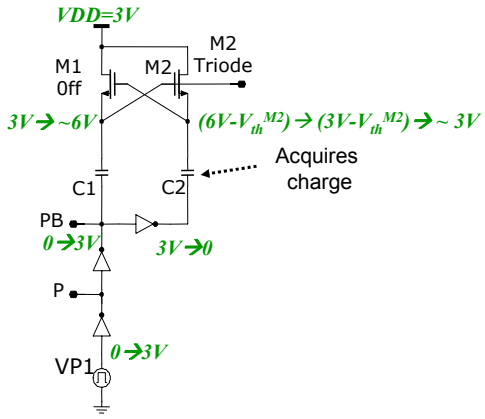
Clock Voltage Doubler



a) Start–up

b) Next clock phase

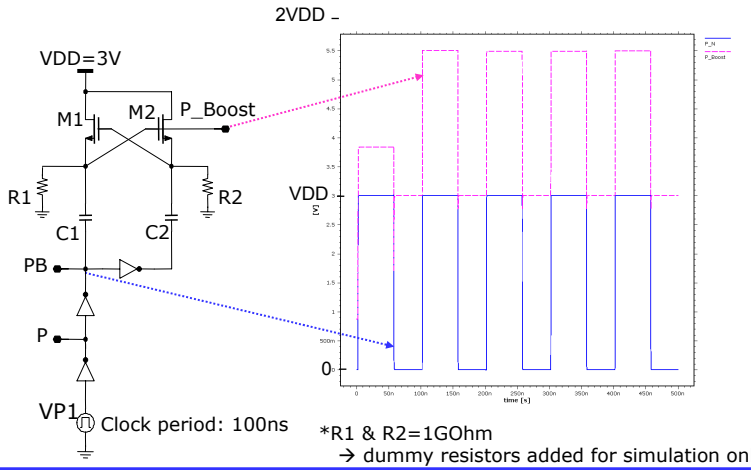
Clock Voltage Doubler



c) Next clock phase

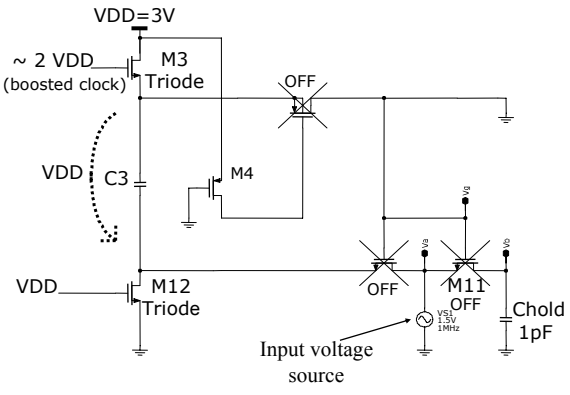
- Both C1 & C2 → charged to VDD after one clock cycle
- Note that bottom plate of C1 & C2 is either 0 or VDD while top plates are at VDD or 2VDD

Clock Voltage Doubler

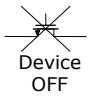


*R1 & R2=1GOhm
→ dummy resistors added for simulation only

Constant V_{GS} Sampler: Φ Low

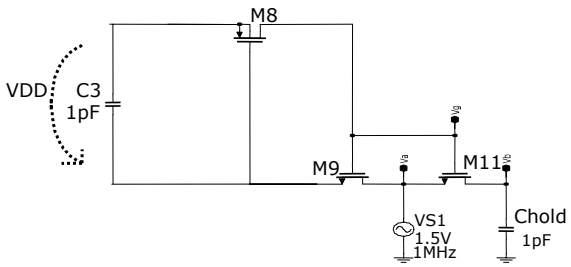


- Sampling switch M11 is OFF



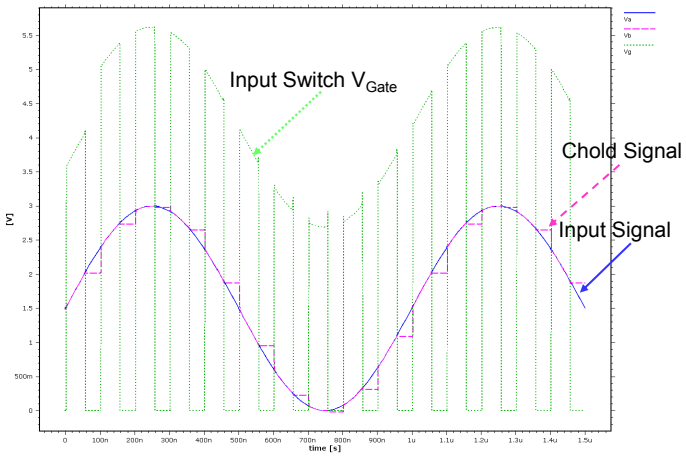
- C3 charged to ~VDD

Constant V_{GS} Sampler: Φ High



- C3 previously charged to VDD
- M8 & M9 are on: C3 across G-S of M11
- M11 on with constant VGS = VDD

Constant V_{GS} Sampling



Boosted Clock Sampling Complete Circuit

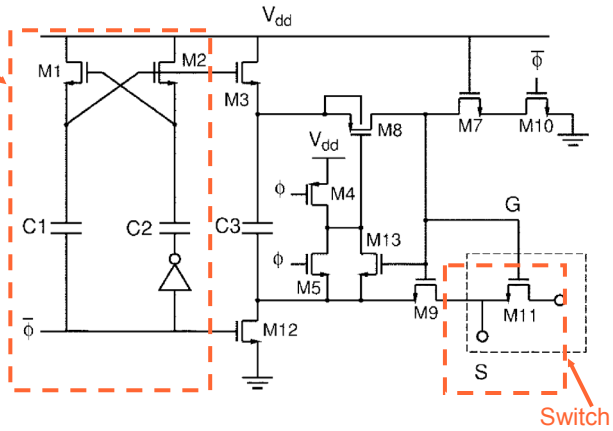
Clock Multiplier

M7 & M13 for reliability

Remaining issues:

-V_{GS} constant only for $V_{in} < V_{out}$

-Nonlinearity due to Vth dependence of M11on body-source voltage



Ref: A. Abo et al, "A 1.5-V, 10-bit, 14.3-MS/s CMOS Pipeline Analog-to-Digital Converter," JSSC May 1999, pp. 599.