• DAC Converters (continued)
  – DAC design considerations
  – Self calibration techniques
    • Current copiers
    • Dynamic element matching
  – DAC reconstruction filter

• ADC Converters
  – Sampling
    • Sampling switch considerations
      – Thermal noise due to switch resistance
      – Sampling switch bandwidth limitations
      – Switch induced distortion
    • Sampling switch conductance dependence on input voltage
    • Clock voltage boosters
Current-Switched DACs in CMOS

Assumptions:
- $R_{x}$ small compared to transistor gate-overdrive
- To simplify analysis: Initially, all device currents assumed to be equal to $I$

\[
V_{GS_{M1}} = V_{GS_{M1}} - 4RI
\]
\[
V_{GS_{M2}} = V_{GS_{M1}} - 7RI
\]
\[
V_{GS_{M3}} = V_{GS_{M1}} - 9RI
\]
\[
V_{GS_{M4}} = V_{GS_{M1}} - 10RI
\]
\[
I_2 = k(V_{GS_{M2}} - V_{th})^2
\]
\[
I_2 = I_1 \left(1 - \frac{4RI}{V_{GS_{M1}} - V_{th}}\right)^2
\]

Example: 5 unit element current sources

Desirable to have $g_m$ small
Two sources of systematic error:
- Finite current source output resistance
- Voltage drop due to finite ground bus resistance

Example: INL of 3-Bit unit element DAC

- If switching of current sources arranged sequentially (1-2-3-4-5-6-7)
  → \( \text{INL} = +0.25 \text{LSB} \)
- If switching of current sources symmetrical (4-3-5-2-6-1-7)
  → \( \text{INL} = +0.09, -0.058 \text{LSB} \) → \( \text{INL} \) reduced by a factor of 2.6

Current-Switched DACs in CMOS
Example: INL of 3-Bit unit element DAC

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Current-Switched DACs in CMOS
Example: DNL of 7 unit element DAC

Input DNL [LSB]

- If switching of current sources arranged sequentially (1-2-3-4-5-6-7)
  \[ DNL_{\text{max}} = +0.15\text{LSB} \]

- If switching of current sources symmetrical (4-3-5-2-6-1-7)
  \[ DNL_{\text{max}} = +0.15\text{LSB} \] \[ DNL_{\text{max}} \text{ unchanged} \]

Example: 7 unit element current source DAC- assume \( g_mR = 1/100 \)

More recent published DAC using symmetrical switching built in 0.35\( \mu \)V/3V analog/1.9V digital, area x10 smaller compared to previous example
A 10-bit 1-GSample/s Nyquist Current-Steering CMOS D/A Converter

Anton Van den Bosch, Student Member, IEEE, Marc A. F. Borreman, Student Member, IEEE, Michel S. J. Steyaert, Senior Member, IEEE, and Willy Sansen, Fellow, IEEE

- Layout of Current sources - each current source made of 4 devices in parallel each located in one of the 4 quadrants
- Thermometer decoder used to convert incoming binary digital control for the 5 MSB bits
- Dummy decoder used on the LSB side to match the latency due to the MSB decoder

- Current source layout
  - MSB current sources layout in the mid sections of the four quad
  - LSB current sources mostly in the periphery
  - Two rows of dummy current sources added @ the periphery to create identical environment for devices in the center versus the ones on the outer sections
A 10-bit 1-GSample/s Nyquist Current-Steering CMOS D/A Converter

Anne Van den Bosch, Student Member, IEEE; Marc A. F. Borremans, Student Member, IEEE; Michel S. J. Steyaert, Senior Member, IEEE; and Willy Sansen, Fellow, IEEE

Note that each current cell has its clocked latch and clock signal laid out to be close to its switch to ensure simultaneous switching of current sources.

Special attention paid to the final latch to have the cross point of the complementary switch control signal such that the two switches are not both turned off during transition.

• Measured DNL/INL with current associated with the current cells as variable.
 Called: Current Copier

Fig. 2. Calibration principle. (a) Calibration. (b) Operation.

16bit DAC (6+10) - MSB DAC uses current copier technique
Current Divider Inaccuracy due to Device Mismatch

M1 & M2 mismatch results in the two output currents not being exactly equal:

\[
I_d = \frac{I_{d1} + I_{d2}}{2}
\]

\[
\frac{dI_d}{I_d} = \frac{I_{d1} - I_{d2}}{I_d}
\]

\[
\frac{dI_d}{I_d} = \frac{2}{V_{GS} - V_{th}} \times \left[ \left( \frac{dW_{L}}{W_{L}} \right) + dV_{th} \right]
\]

Problem: Device mismatch could severely limit DAC accuracy

Use of dynamic element matching (next few pages)

Dynamic Element Matching for High-Accuracy Monolithic D/A Converters

RUDY J. VAN DE PLASSCHE

Fig. 2. (a) New current divider schematic diagram. (b) Time dependence of various currents in the new divider.
Dynamic Element Matching

During Φ₁

\[ I_f^{(1)} = \frac{1}{2} I_o (1 + \Delta I) \]
\[ I_f^{(1)} = \frac{1}{2} I_o (1 - \Delta I) \]

During Φ₂

\[ I_f^{(2)} = \frac{1}{2} I_o (1 - \Delta I) \]
\[ I_f^{(2)} = \frac{1}{2} I_o (1 + \Delta I) \]

Average of \( I_f \):

\[ \langle I_f \rangle = \frac{I_f^{(1)} + I_f^{(2)}}{2} \]
\[ = \frac{I_o (1 - \Delta I) + (1 + \Delta I)}{2} \]
\[ = \frac{I_o}{2} \]

Note:
For optimum current division accuracy → clock frequency is divided by two for each finer division
Problem: Frequency of operation drastically reduced

Fig. 4. (a) Binary weighted current network using different switching frequencies. (b) Time dependence of current flowing in the first and second divider stage.

Note: What if the same clock frequency is used?
Dynamic Element Matching

During $\Phi_1$  
\[
I_1^{(1)} = \frac{1}{2} I_o (1 + \Delta_1) \\
I_1^{(2)} = \frac{1}{2} I_o (1 - \Delta_1)
\]
\[
I_1^{(3)} = \frac{1}{2} I_o (1 + \Delta_2) \\
I_1^{(4)} = \frac{1}{2} I_o (1 - \Delta_2)
\]
\[
\langle I_1 \rangle = \frac{I_1^{(1)} + I_1^{(2)} + I_1^{(3)} + I_1^{(4)}}{4} \\
= \frac{I_o (1 + \Delta_1)(1 + \Delta_2) + (1 - \Delta_1)(1 - \Delta_2)}{2} \\
= \frac{I_o}{4} (1 + \Delta_1 \Delta_2)
\]

During $\Phi_2$  
\[
I_2^{(1)} = \frac{1}{2} I_o (1 + \Delta_1) \\
I_2^{(2)} = \frac{1}{2} I_o (1 - \Delta_1)
\]
\[
I_2^{(3)} = \frac{1}{2} I_o (1 + \Delta_2) \\
I_2^{(4)} = \frac{1}{2} I_o (1 - \Delta_2)
\]
\[
\langle I_2 \rangle = \frac{I_2^{(1)} + I_2^{(2)} + I_2^{(3)} + I_2^{(4)}}{4} \\
= \frac{I_o (1 + \Delta_1)(1 + \Delta_2) + (1 - \Delta_1)(1 - \Delta_2)}{2} \\
= \frac{I_o}{4} (1 + \Delta_1 \Delta_2)
\]

E.g. $\Delta_1 = \Delta_2 = 1\%$  \(\rightarrow\) matching error is $(1\%)^2 = 0.01\%$

---

Dynamic Element Matching for High-Accuracy Monolithic D/A Converters

RUDY J. VAN DE PLASCHER

• Bipolar 12-bit DAC using dynamic element matching built in 1976
• Element matching clock frequency 100kHz
• INL <0.25LSB!
Example: State-of-the-Art current steering DAC

<table>
<thead>
<tr>
<th></th>
<th>Max Sample Frequency</th>
<th>1.4</th>
<th>GSPS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution</td>
<td>14</td>
<td></td>
<td>Bit</td>
</tr>
<tr>
<td>DNL</td>
<td>+/- 0.8</td>
<td></td>
<td>LSB</td>
</tr>
<tr>
<td>INL</td>
<td>+/- 2.1</td>
<td></td>
<td>LSB</td>
</tr>
<tr>
<td>SFDR @ 1.0 GSPS</td>
<td>&gt; 60</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>IMD @ 1.0 GSPS</td>
<td>&gt; 64</td>
<td></td>
<td>dBC</td>
</tr>
<tr>
<td>NSD @ f_{out} = 400MHz</td>
<td>-155</td>
<td></td>
<td>dBm/Hz</td>
</tr>
<tr>
<td>Power (Core) @ 1.4GSPS</td>
<td>200</td>
<td></td>
<td>mW</td>
</tr>
<tr>
<td>Power (Total) @ 1.4GSPS</td>
<td>400</td>
<td></td>
<td>mW</td>
</tr>
<tr>
<td>Area (Core)</td>
<td>0.8</td>
<td></td>
<td>mm²</td>
</tr>
<tr>
<td>Area (Chip)</td>
<td>6.25</td>
<td></td>
<td>mm²</td>
</tr>
</tbody>
</table>
DAC In the Big Picture

- Learned to build DACs
  - Convert the incoming digital signal to analog
- DAC output → staircase form
- Some applications require filtering (smoothing) of DAC output → reconstruction filter

DAC Reconstruction Filter

- Need for and requirements depend on application
- Tasks:
  - Correct for sinc droop
  - Remove “aliases” (stair-case approximation)
Reconstruction Filter Options

- Reconstruction filter options:
  - Continuous-time filter only
  - CT + SC filter
- SC filter possible only in combination with oversampling (signal bandwidth $B << f_s/2$)
- Digital filter
  - Band limits the input signal → prevent aliasing
  - Could also provide high-frequency pre-emphasis to compensate in-band $\sin x/x$ amplitude droop associated with the inherent DAC S/H function

DAC Reconstruction Filter

Example: Voice-Band CODEC Receive Path


Note: $f_{\text{sig max}} = 3.4\text{kHz}$

$f_{\text{DAC}} = 8\text{kHz}$

$\sin (\pi f_{\text{sig max}} x T_s)/ (\pi f_{\text{sig max}} x T_s)$

$= -2.75 \text{ dB droop due to DAC } \sin x/x \text{ shape}$
Summary
D/A Converter

• D/A architecture
  – Unit element – complexity proportional to $2^B$, excellent DNL
  – Binary weighted- complexity proportional to B- poor DNL
  – Segmented- unit element MSB($B_1$)+ binary weighted LSB($B_2$)
    → Complexity proportional ($2^{B_1-1} + B_2$) -DNL compromise between the two

• Static performance
  – Component matching

• Dynamic performance
  – Time constants, Glitches

• DAC improvement techniques
  – Symmetrical switching rather than sequential switching
  – Current source self calibration
  – Dynamic element matching

• Depending on the application, reconstruction filter may be needed

What Next?

• ADC Converters:
  – Need to build circuits that "sample"
  – Need to build circuits for amplitude quantization

Analog Input
    | Anti-Aliasing Filter
    | Sampling +Quantization
    | "Bits to Staircase"
    | Reconstruction Filter
    | Analog Output

    Analog Preprocessing
    | A/D Conversion
    | DSP
    | D/A Conversion
    | Analog Post processing

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Analog-to-Digital Converters

• Two categories:
  – Nyquist rate ADCs $\Rightarrow f_{\text{sig max}} \sim 0.5f_{\text{sampling}}$
    • Maximum achievable signal bandwidth higher compared to oversampled type
    • Resolution limited to max. 12-14bits
  – Oversampled ADCs $\Rightarrow f_{\text{sig max}} \ll 0.5f_{\text{sampling}}$
    • Maximum achievable signal bandwidth significantly lower compared to nyquist
    • Maximum achievable resolution high (18 to 20bits!)

MOS Sampling Circuits
Ideal Sampling

• In an ideal world, zero resistance sampling switches would close for the briefest instant to sample a continuous voltage $v_{IN}$ onto the capacitor $C$.

  $\rightarrow$ Output Dirac-like pulses with amplitude equal to $v_{IN}$ at the time of sampling.

• In practice not realizable!

Ideal Track & Hold Sampling

• $V_{out}$ tracks input for $\frac{1}{2}$ clock cycle when switch is closed.
• Acquires exact value of $V_{in}$ at the instant the switch opens.
• "Track and Hold" (T/H) (often called Sample & Hold!)
Ideal T/H Sampling

Continuous Time

T/H signal (Sampled-Data Signal)

Clock

Discrete-Time Signal

Practical Sampling Issues

- Switch induced noise due to M1 finite channel resistance
- Clock jitter
- Finite $R_{sw} \rightarrow$ limited bandwidth $\rightarrow$ finite acquisition time
- $R_{sw} = f(V_{in}) \rightarrow$ distortion
- Switch charge injection & clock feedthrough
Sampling Circuit kT/C Noise

- Switch resistance & sampling capacitor form a low-pass filter
- Noise associated with the switch resistance results in Total noise variance= kT/C @ the output (see noise analysis in Lecture 1)
- In high resolution ADCs kT/C noise at times dominates overall minimum signal handling capability (power dissipation considerations).

Sampling Network kT/C Noise

For ADCs sampling capacitor size is usually chosen based on having thermal noise smaller or equal or at times larger compared to quantization noise:
Assumption: Nyquist rate ADC

For a Nyquist rate ADC: Total quantization noise power = \( \frac{\Delta^2}{12} \)

Choose C such that thermal noise level is less (or equal) than Q noise

\[
\frac{k_B T}{C} \leq \frac{\Delta^2}{12}
\]

\[
\rightarrow \quad C \geq 12k_B T \left( \frac{2^B - 1}{V_{FS}} \right)^2
\]

\[
\rightarrow \quad C \geq 12k_B T \times \frac{2^{2B}}{V_{FS}^2}
\]
**Sampling Network $kT/C$ Noise**

$$C \geq 12kBT \frac{2^B}{V_{FS}^2}$$

| Required $C_{\text{min}}$ as a Function of ADC Resolution |
|---------------------------------|-----------------|-----------------|
| B     | $C_{\text{min}}$ ($V_{FS} = 1V$) | $C_{\text{min}}$ ($V_{FS} = 0.5V$) |
| 8     | 0.003 pF                  | 0.012 pF                  |
| 12    | 0.8 pF                    | 2.4 pF                    |
| 14    | 13 pF                     | 52 pF                     |
| 16    | 206 pF                    | 824 pF                    |
| 20    | 52,800 pF                 | 211,200 pF                 |

The large area required for $C$ limit highest achievable resolution for Nyquist rate ADCs.

Oversampling results in reduction of required value for $C$ (will be covered in oversampled converter lectures).

**Clock Jitter**

- So far: clock signal controls sampling instants – which we assumed to be precisely equi-distant in time (period $T$)

- Real clock generator $\rightarrow$ some level of variability

- Variability in $T$ causes errors
  - "Aperture Uncertainty" or "Aperture Jitter"

- What is the effect of clock jitter on ADC performance?
Clock Jitter

- Sampling jitter adds an error voltage proportional to the product of \((t_J - t_0)\) and the derivative of the input signal at the sampling instant.

- Does jitter matter when sampling dc signals \((x'(t_0) = 0)\)?

\[ e = x'(t_0)(t_J - t_0) \]

The error voltage is

\[ e = x'(t_0)(t_J - t_0) \]
Effect of Clock Jitter on Sampling of a Sinusoidal Signal

Sinusoidal input

Amplitude: \( A \)
Frequency: \( f_s \)
Jitter: \( A \sin(2\pi f_s t) \)

Worst case

\[ A = \frac{A_{FS}}{2}, \quad f_s = \frac{f_s}{2} \]

\[ \Delta \ll \frac{A_{FS}}{2^b + 1} \]

\[ dt \ll \frac{1}{2^b \pi f_s} \]

\[
\begin{array}{|c|c|c|}
\hline
\text{# of Bits} & f_s & dt \ll \\
\hline
12 & 1 MHz & 78 \text{ ps} \\
16 & 20 MHz & 0.24 \text{ ps} \\
10 & 1000 MHz & 0.3 \text{ ps} \\
\hline
\end{array}
\]

Law of Jitter

- The worst case looks pretty stringent … what about the “average”?
- Let’s calculate the mean squared jitter error (variance)
- If we’re sampling a sinusoidal signal
  \[ x(t) = A \sin(2\pi f_s t), \]
  then
  \[ x'(t) = 2\pi f_s A \cos(2\pi f_s t) \]
  \[ E[|x'(t)|^2] = 2\pi^2 f_s^2 A^2 \]
- Assume the jitter has variance \( E[(t_j - t_0)^2] = \tau^2 \)
Law of Jitter

- If $x'(t)$ and the jitter are independent
  \[ E[(x'(t)(t_j-t_0))^2] = E[x'(t)]^2 E[(t_j-t_0)^2] \]

- Hence, the jitter error power is
  \[ E[e^2] = 2\pi^2 f_x^2 A^2 \tau^2 \]

- If the jitter is uncorrelated from sample to sample, this “jitter noise” is white
Example: ADC Spectral Tests

- SFDR
- SDR
- SNR


More on Jitter

- In cases where clock signal is provided from off-chip ➔ have to choose a source with low enough jitter
- On-chip precautions to keep the clock jitter less than single-digit pico-second:
  - Separate supplies as much as possible
  - Separate analog and digital clocks
  - Short inverter chains between clock source and destination
- Few, if any, other analog-to-digital conversion non-idealities have the same symptoms as sampling jitter:
  - RMS noise proportional to input signal frequency
  - RMS noise proportional to input signal amplitude

 ➔ In cases where clock jitter limits the dynamic range, it’s easy to tell, but may be difficult to fix...
Sampling Acquisition Bandwidth

- The resistance $R$ of switch $S_1$ turns the sampling network into a lowpass filter with finite time constant:
  \[ \tau = RC \]

- Assuming $V_{in}$ is constant during the sampling period and $C$ is initially discharged

- Need to allow enough time for the output to settle to less than 1 ADC LSB \( \Delta \) determines minimum duration for \( \phi_1 \) or maximum clock frequency

\[ v_{out}(t) = v_{in}(1 - e^{-t/\tau}) \]

---

Sampling: Effect of Switch On-Resistance

\[ V_{in}^n - V_{out}^n \ll \Delta \text{ since } V_{out} = V_{in}(1 - e^{-t/\tau}) \]

\[ \rightarrow V_{in} e^{-T_s/\tau} \ll \Delta \text{ or } \tau \ll \frac{T_s}{2} \ln\left(\frac{V_{in}}{\Delta}\right) \]

Worst Case: $V_{in} = V_{SS}$

\[ \tau \ll \frac{T_s}{2} \frac{1}{\ln(2^B - 1)} = 0.72 \times T_s \]

\[ R \ll \frac{1}{2f_sC \ln(2^B - 1)} \approx 0.72 \times \frac{1}{Bf_sC} \]

Example:

- $B = 14$, $C = 13pF$, $f_s = 100MHz$
- $T_s/\tau >> 19.4$, or $10 \tau << T_s/2 \rightarrow R << 40 \Omega$
Switch On-Resistance

Switch \( \rightarrow \) MOS operating in triode mode:

\[
I_{D(\text{triode})} = \mu C_{m} \frac{W}{L} \left( V_{GS} - \frac{V_{DD}}{2} \right) V_{DS}, \quad \frac{1}{R_{ON}} = \frac{dI_{D(\text{triode})}}{dV_{DS}} \bigg|_{V_{DS}=0}
\]

\[
R_{ON} = \frac{1}{\mu C_{m} \frac{W}{L}(V_{GS} - V_{th})} = \frac{1}{\mu C_{m} \frac{W}{L}(V_{DD} - V_{th})}
\]

Let us call \( R \) at \( V_{in}=0 \) \( R_o \) then

\[
R_{ON} = \frac{R_o}{1 - \frac{V_{in}}{V_{DD} - V_{th}}}
\]

Sampling Distortion

Simulated 10-Bit ADC &

\[
\frac{T}{2} = 5 \tau \\
V_{DD} - V_{th} = 2V \\
V_{FS} = 1V
\]

Sampling Switch modeled:

\[
V_{out} = \left( V_{in} \cdot \frac{1 - e^{-\frac{T}{2\tau}}}{V_{in} - V_{th}} \right)
\]

\( \rightarrow \) Results in

\[
HD2 = -41 \text{dBFS} \& \\
HD3 = -51.4 \text{dBFS}
\]
Sampling Distortion

Doubling sampling time (or $\frac{1}{2}$ time constant)
Results in:

HD2 improved from -41dBFS to -70dBFS ~30dB
HD3 improved from -51.4dBFS to -76.3dBFS ~25dB

Allowing enough time for the sampling network settling
Reduces distortion due to switch R non-linear behavior to a tolerable level

Effect of Supply Voltage

- 10bit ADC & $T_s/2 = 5\tau$
  $V_{DD} - V_{th} = 2V$  $V_{FS} = 1V$

- Effect of higher supply voltage on sampling distortion
  - HD3 decrease by $(V_{DD}/V_{DD2})^2$
  - HD2 decrease by $(V_{DD}/V_{DD2})$

10bit ADC & $T_s/2 = 10\tau$
$V_{DD} - V_{th} = 2V$  $V_{FS} = 1V$

$V_{DD} - V_{th} = 4V$  $V_{FS} = 1V$
Sampling Distortion

- SFDR → sensitive to sampling distortion - improve linearity by:
  - Larger $V_{DD}/V_{FS}$
  - Higher sampling bandwidth
- Solutions:
  - Overdesign → Larger switches issue:
    - Increased switch charge injection
    - Increased nonlinear $S$ & $D$ junction cap.
  - Maximize $V_{DD}/V_{FS}$
    - Decreased dynamic range if $V_{DD}$ const.
  - Complementary switch
  - Constant & max. $V_{GS} \neq f(V_{in})$

Practical Sampling

Summary So Far!

- $kT/C$ noise
  $$C \geq 12k_BT \frac{2B}{V_{FS}^2}$$
- Finite $R_{sw}$ → limited bandwidth
  $$R \ll \frac{0.72}{Bf_C}$$
- $g_{sw} = f(V_{in})$ → distortion
  $$g_{ON} = g_o \left(1 - \frac{V_{in}}{V_{DD} - V_{th}}\right)$$
  for
  $$g_o = \mu C_{ox} \frac{W}{L}(V_{DD} - V_{th})$$
Sampling: Use of Complementary Switches

- Complementary n & p switch advantages:
  - Increase in the overall conductance
  - Linearize the switch conductance for the range \( |V_{th}^n| < V_{in} < V_{dd} - |V_{th}^p| \)

Complementary Switch Issues

Supply Voltage Evolution

- Supply voltage has scaled down with technology scaling
- Threshold voltages do not scale accordingly

Complementary Switch
Effect of Supply Voltage Scaling

As supply voltage scales down input voltage range for constant $g_{o}$ shrinks, Complementary switch not effective when $V_{DD}$ becomes comparable to $2xV_{th}$.

Boosted & Constant $V_{GS}$ Sampling

Gate voltage $V_{GS} =$ low
- Device off
- Beware of signal feedthrough due to parasitic capacitors

Increase gate overdrive voltage as much as possible + keep $V_{GS}$ constant
- Switch overdrive voltage independent of signal level
- Error due to finite $R_{ON}$ linear (to 1st order)
- Lower $R_{on}$ → lower time constant
Constant $V_{GS}$ Sampling

- **Boosted clock**
- **Input signal** (= voltage @ the switch input terminal)

**Constant $V_{GS}$ Sampling Circuit**

- **VP1**: 100ns
- **M1-M12**: All device sizes: 10μ/0.35μ
- **C1-C3**: All capacitor size: 1pF (except for Chold)
- **VS1**: 1.5V 1MHz
- **Sampling switch & C**

**Note:** Each critical switch requires a separate clock booster
Clock Voltage Doubler

a) Start-up

- $V_{DD}=0 \rightarrow 3V$
- M1 off
- $0 \rightarrow 3V$
- C1
- P
- VP1 = clock

- $0 \rightarrow 3V$

- Acquire charge

b) Next clock phase

- $V_{DD}=3V$
- M1 Triode
- $3V \rightarrow 0$
- (3V - $V_{th}^{M2}$) ➔ (6V - $V_{th}^{M2}$)
- C1
- C2
- P
- VP1

- $3V \rightarrow 0$

- Acquire charge

- Both C1 & C2 ➔ charged to VDD after one clock cycle

- Note that bottom plate of C1 & C2 is either 0 or VDD while top plates are at VDD or 2VDD

c) Next clock phase

- $V_{DD}=3V$
- M1 off
- $3V \rightarrow 6V$
- M2 Triode
- (6V - $V_{th}^{M2}$) ➔ (3V - $V_{th}^{M2}$) ➔ ~ 3V
- C1
- C2
- P
- VP1

- $0 \rightarrow 3V$
**Clock Voltage Doubler**

- Clock period: 100ns
- R1 & R2 = 1 GΩ
- Dummy resistors added for simulation only

**Constant V\textsubscript{\text{GS}} Sampler: \Phi Low**

- Sampling switch M11 is OFF
- C3 charged to ~VDD

- VDD = 3V
- ~2 VDD (boosted clock)
Constant $V_{GS}$ Sampler: $\Phi$ High

- C3 previously charged to VDD
- M8 & M9 are on: C3 across G-S of M11
- M11 on with constant $V_{GS} = VDD$

Constant $V_{GS}$ Sampling

Input Switch $V_{Gate}$

Chold Signal

Input Signal
Boosted Clock Sampling
Complete Circuit

- $V_{DS}$ constant only for $V_{in} < 0$
- Nonlinearity due to $V_{th}$ dependence of $M11$ on body-source voltage

Remaining issues:

M7 & M13 for reliability