EE247
Lecture 15

- Administrative issues
  - Midterm exam postponed to **Tues. Oct. 28th**
    - o You can *only* bring one 8x11 paper with your own written notes (please do not photocopy)
    - o No books, class or any other kind of handouts/notes, calculators, computers, PDA, cell phones....
    - o Midterm includes material covered to end of lecture 14

EE247
Lecture 15

- D/A converters
  - Static performance of D/As (continued)
    - Systematic & random errors
  - Practical aspects of current-switched DACs
  - Segmented current-switched DACs
  - DAC dynamic non-idealities
  - DAC design considerations
  - Self calibration techniques
    - Current copiers
    - Dynamic element matching
  - DAC reconstruction filter

Summary Last Lecture

D/A converter architectures:

- Resistor string DAC
- Serial charge redistribution DAC
- Parallel charge scaling DAC
- Combination of resistor string (MSB) & binary weighted charge scaling (LSB)
- Current source DAC
  - Unit element
  - Binary weighted

- Static performance
  - Component matching-systematic & random errors
    - Component random variations → Gaussian pdf
    - INL for both unit-element DAC: $\sigma_{INL} = \sigma_{\varepsilon} \, x2^{B/2-1}$
    - DNL for unit-element: $\sigma_{DNL} = \sigma_{\varepsilon}$

DAC INL

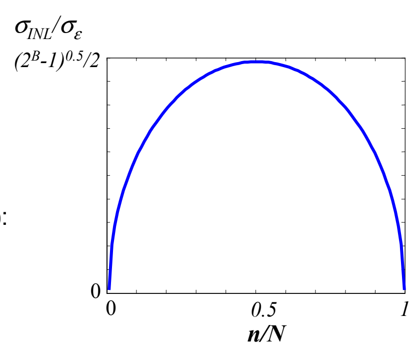
$$\sigma_E^{\,2} = n\left(1 - \frac{n}{N}\right) \times \sigma_\varepsilon^{\,2}$$

$$To\ find\ max.\ variance: \quad \frac{d\sigma_E^{\,2}}{dn} = 0$$

$$\rightarrow n = N/2 \rightarrow \sigma_E^{\,2} = \frac{N}{4} \times \sigma_\varepsilon^{\,2}$$

- Error is maximum at mid-scale ($N/2$):

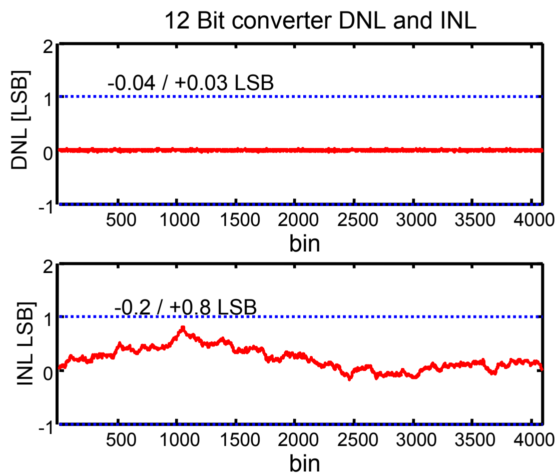
$$\boxed{\sigma_{INL} = \frac{1}{2}\sqrt{2^B - 1}\,\sigma_\varepsilon \quad with \quad N = 2^B - 1}$$



- INL depends on both DAC resolution & element matching σ_ε
- While $\sigma_{DNL} = \sigma_\varepsilon$ is to first order independent of DAC resolution and is only a function of element matching

Ref: Kuboki et al, TCAS, 6/1982

Simulation Example



σ_ε = 1%
B = 12
Random # generator used in MatLab

Computed INL:
σ_{INL}^{max} = 0.32 LSB (midscale)

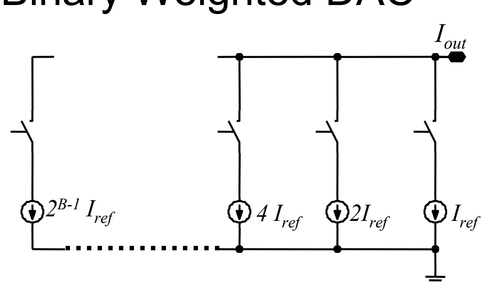
Why is the results not as expected per our derivation?

INL & DNL for Binary Weighted DAC

- INL same as for unit element DAC
- DNL depends on transition
  - Example:

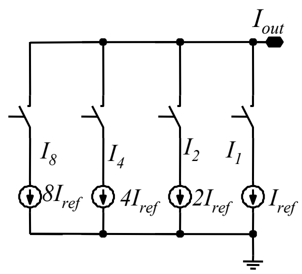
    0 to 1 → $\sigma_{DNL}^2 = \sigma_{(dI/I)}^{\ 2}$

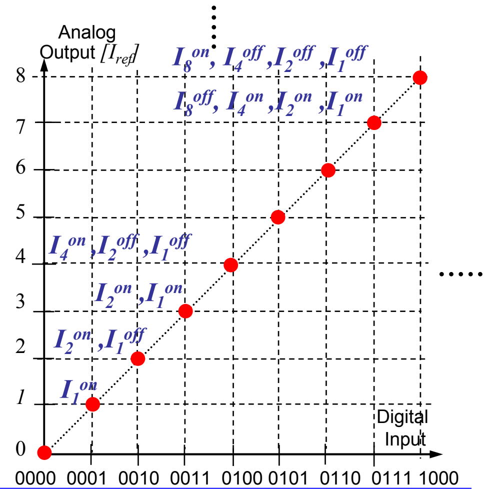
    1 to 2 → $\sigma_{DNL}^2 = 3\sigma_{(dI/I)}^{\ 2}$



- Consider MSB transition: 0111 … → 1000 …

DAC DNL
Example: 4bit DAC



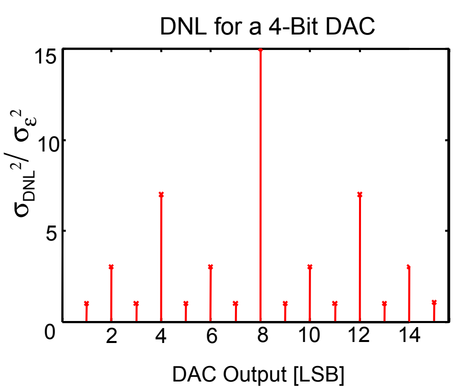


- DNL depends on transition
  - Example:

    0 to 1 → $\sigma_{DNL}^2 = \sigma_{(dIref/Iref)}^2$

    1 to 2 → $\sigma_{DNL}^2 = 3\sigma_{(dIref/Iref)}^2$

Binary Weighted DAC DNL



- Worst-case transition occurs at mid-scale:

$$\sigma_{DNL}^2 = \underbrace{\left(2^{B-1}-1\right)\sigma_\varepsilon^2}_{0111\ldots} + \underbrace{\left(2^{B-1}\right)\sigma_\varepsilon^2}_{1000\ldots}$$

$$\cong 2^B \sigma_\varepsilon^2$$

$$\sigma_{DNL_{max}} = 2^{B/2}\sigma_\varepsilon$$

$$\sigma_{INL_{max}} \cong \frac{1}{2}\sqrt{2^B - 1}\,\sigma_\varepsilon \cong \frac{1}{2}\sigma_{DNL_{max}}$$

- Example:

  B = 12, σ_ε = 1%

  → σ_{DNL} = 0.64 LSB

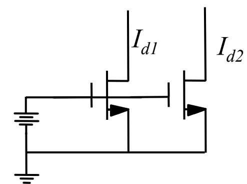
  → σ_{INL} = 0.32 LSB

MOS Current Source Variations Due to Device Matching Effects

$$I_d = \frac{I_{d1} + I_{d2}}{2}$$

$$\frac{dI_d}{I_d} = \frac{I_{d1} - I_{d2}}{I_d}$$

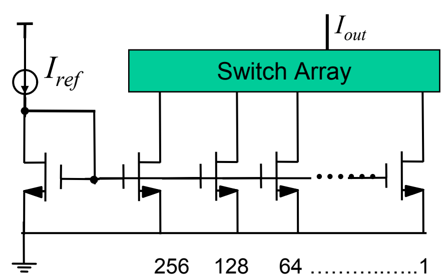
$$\frac{dI_d}{I_d} = \frac{d\,W/L}{W/L} + \frac{2 \times d\,V_{th}}{V_{GS} - V_{th}}$$



- Current matching depends on:
  - Device W/L ratio matching
    → Larger device area less mismatch effect
  - Current mismatch due to threshold voltage variations:
    → Larger gate-overdrive less threshold voltage mismatch effect

Current-Switched DACs in CMOS

$$\frac{dI_d}{I_d} = \frac{d\,W/L}{W/L} + \frac{2d\,V_{th}}{V_{GS} - V_{th}}$$



Example: 8bit Binary Weighted

- Advantages:
  Can be very fast
  Reasonable area for resolution < 9-10bits

- Disadvantages:
  Accuracy depends on device W/L & V_{th} matching

Unit Element versus Binary Weighted DAC

Unit Element DAC

$$\sigma_{DNL} = \sigma_{\varepsilon}$$

$$\sigma_{INL} \cong 2^{B/2 - 1} \sigma_{\varepsilon}$$

Binary Weighted DAC

$$\sigma_{DNL} \cong 2^{B/2} \sigma_{\varepsilon} = 2\sigma_{INL}$$

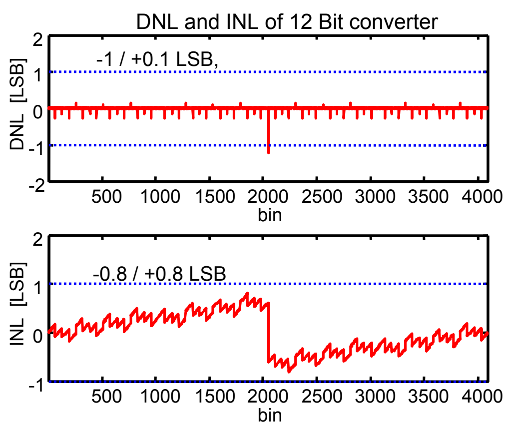
$$\sigma_{INL} \cong 2^{B/2 - 1} \sigma_{\varepsilon}$$

Number of switched elements:

$$S = 2^B \qquad\qquad S = B$$

Key point: Significant difference in performance and complexity!

"Another" Random Run …

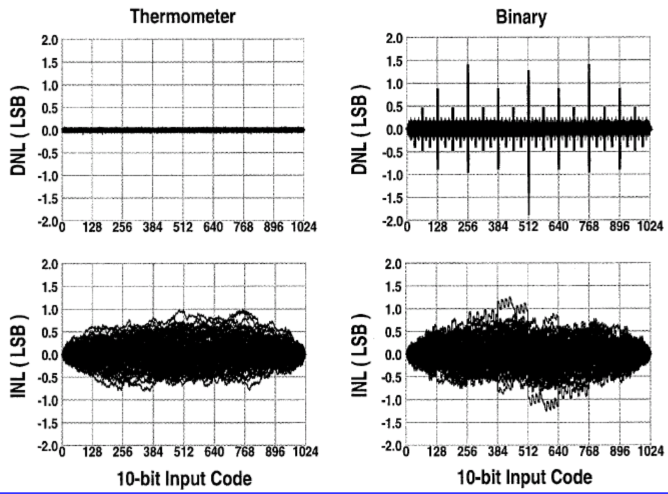


Now (by chance) worst DNL is mid-scale.

Close to statistical result!

10Bit DAC DNL/INL Comparison Plots: 100 Simulation Runs Overlaid

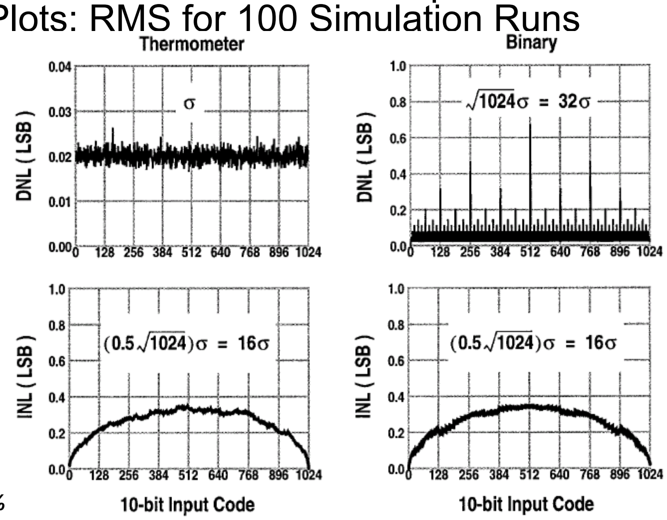
Ref: C. Lin and K. Bult, "A 10-b, 500-MSample/s CMOS DAC in 0.6 mm2," *IEEE Journal of Solid-State Circuits,* vol. 33, pp. 1948 - 1958, December 1998.



Note: σ_ε**=2%**

10Bit DAC DNL/INL Comparison Plots: RMS for 100 Simulation Runs

Ref: C. Lin and K. Bult, "A 10-b, 500-MSample/s CMOS DAC in 0.6 mm2," *IEEE Journal of Solid-State Circuits,* vol. 33, pp. 1948 - 1958, December 1998.



Note: σ_ε**=2%**

DAC INL/DNL Summary

- DAC choice of architecture has significant impact on DNL
- INL is independent of DAC architecture and requires element matching commensurate with overall DAC precision
- Results assume uncorrelated random element variations
- Systematic errors and correlations are usually also important and may affect final DAC performance

Ref: Kuboki, S.; Kato, K.; Miyakawa, N.; Matsubara, K. Nonlinearity analysis of resistor string A/D converters. IEEE Transactions on Circuits and Systems, vol.CAS-29, (no.6), June 1982. p.383-9.

Unit Element versus Binary Weighted DAC Example: B=10

Unit Element DAC

$$\sigma_{DNL} = \sigma_{\varepsilon}$$

$$\sigma_{INL} \cong 2^{B/2-1}\sigma_{\varepsilon} = 16\sigma_{\varepsilon}$$

Binary Weighted DAC

$$\sigma_{DNL} \cong 2^{B/2}\sigma_{\varepsilon} = 32\sigma_{\varepsilon}$$

$$\sigma_{INL} \cong 2^{B/2-1}\sigma_{\varepsilon} = 16\sigma_{\varepsilon}$$

Number of switched elements:

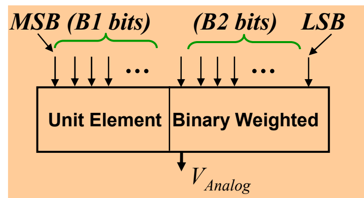
Unit Element DAC: $$S = 2^B = 1024$$

Binary Weighted DAC: $$S = B = 10$$

Significant difference in performance and complexity!

Segmented DAC
Combination of Unit-Element & Binary-Weighted

- Objective:
  Compromise between unit-element and binary-weighted DAC



$B_{Total} = B_1 + B_2$

- Approach:
  B_1 MSB bits → unit elements
  B_2 LSB bits → binary weighted

- INL: unaffected same as either architecture
- DNL: Worst case occurs when LSB DAC turns off and one more MSB DAC element turns on → Same as binary weighted DAC with (B_2+1) # of bits
- Number of switched elements: $(2^{B1}-1) + B_2$

Comparison

Example:

$B = 12, \quad B_1 = 5, \quad B_2 = 7$

$\underbrace{B_1 = 6,}_{\text{MSB}} \quad \underbrace{B_2 = 6}_{\text{LSB}}$

$$\sigma_{DNL} \cong 2^{(B_2+1)/2}\sigma_\varepsilon = 2\sigma_{INL}$$

$$\sigma_{INL} \cong 2^{B/2-1}\sigma_\varepsilon$$

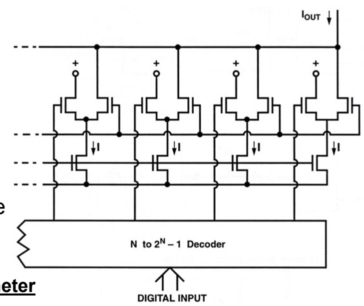
$$S = 2^{B1} - 1 + B_2$$

Assuming: $\sigma_\varepsilon = 1\%$

DAC Architecture (B1+B2)	$\sigma_{INL[LSB]}$	$\sigma_{DNL[LSB]}$	# of switched elements
Unit element (12+0)	0.32	0.01	4095
Segmented (6+6)	0.32	0.113	63+6=69
Segmented (5+7)	0.32	0.16	31+7=38
Binary weighted(0+12)	0.32	0.64	12

Practical Aspects Current-Switched DACs

- Unit element DACs ensure monotonicity by turning on equal-weighted current sources in succession
- Typically current switching performed by differential pairs
- For each diff pair, only one of the devices are on→ switch device mismatch not an issue
- Issue: While binary weighted DAC can use the incoming binary digital word directly, unit element requires a decoder

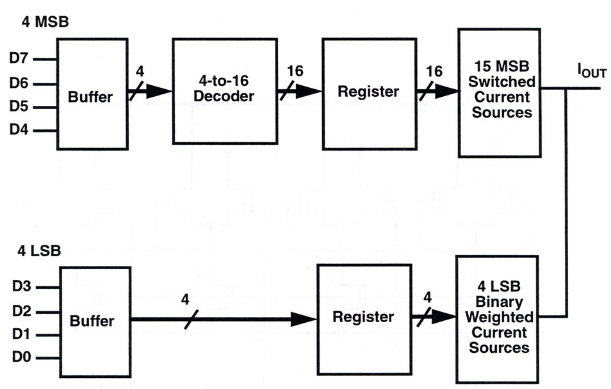


→ N to (2^N-1) decoder

Binary	Thermometer
000	0000000
001	0000001
010	0000011
011	0000111
100	0001111
101	0011111
110	0111111
111	1111111

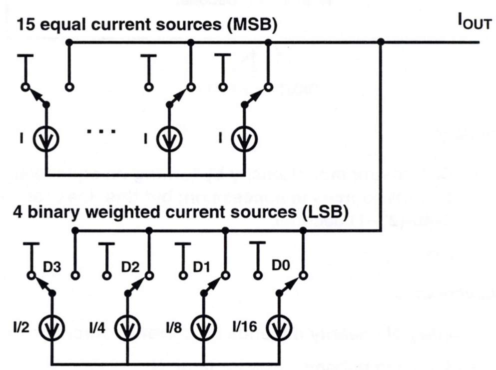
Segmented Current-Switched DAC Example: 8bit→4MSB+4LSB

- 4-bit MSB Unit element DAC + 4-bit binary weighted DAC
- Note: 4-bit MSB DAC requires extra 4-to-16 bit decoder
- Digital code for both DACs stored in a register



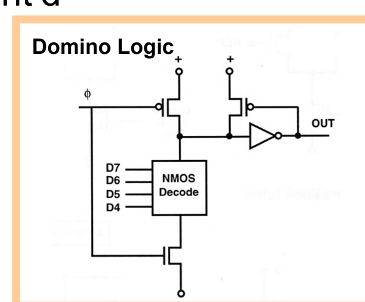
Segmented Current-Switched DAC Cont'd

- 4-bit MSB Unit element DAC + 4-bit binary weighted DAC
- Note: 4-bit MSB DAC requires extra 4-to-16 bit decoder
- Digital code for both DACs stored in a register

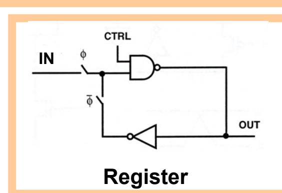


Segmented Current-Switched DAC Cont'd

- MSB Decoder
  - →Domino logic
  - →Example: D4,5,6,7=1 OUT=1



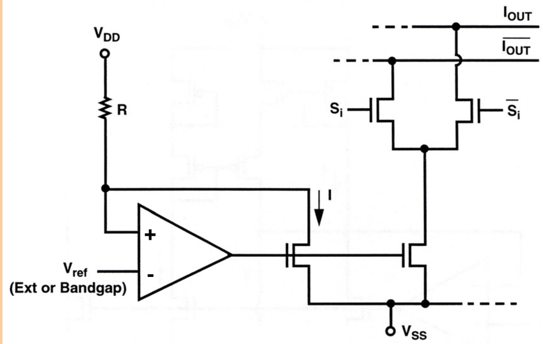
- Register
  - → Latched NAND gate:
  - → CTRL=1 OUT=INB



Segmented Current-Switched DAC Reference Current Considerations

- I_{ref} is referenced to V_{DD}

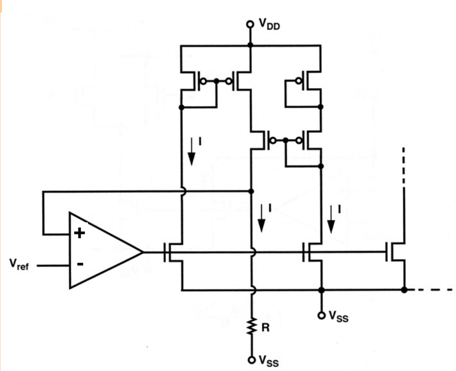
  → Problem: Reference current varies with supply voltage



$$I_{ref}=(V_{DD}-V_{ref})\,/\,R$$

Segmented Current-Switched DAC Reference Current Considerations

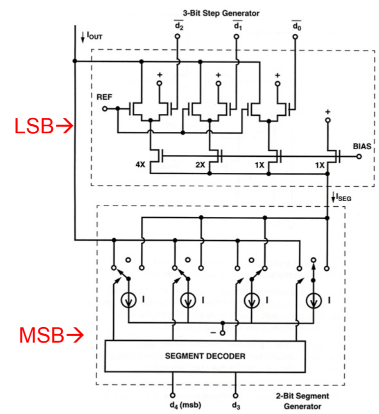
- I_{ref} is referenced to V_{ss}→GND



$$I_{ref}=(V_{ref}-V_{ss})\,/\,R$$

Segmented Current-Switched DAC Considerations

- Example:
  - 2bit MSB Unit element DAC & 3bit binary weighted DAC
- To ensure monotonicity at the MSB→ LSB transition: First OFF MSB current source is routed to LSB current generator

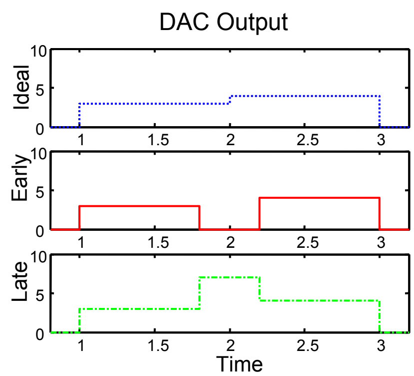


DAC Dynamic Non-Idealities

- Finite settling time
  - Linear settling issues: (e.g. RC time constants)
  - Slew limited settling
- Spurious signal coupling
  - Coupling of clock/control signals to the output via switches
- Timing error related glitches
  - Control signal timing skew

Dynamic DAC Error: Timing Glitch

- Consider binary weighted DAC transition 011 → 100
- DAC output depends on timing
- Plot shows situation where the control signals for LSB & MSB
  - LSB/MSBs on time
  - LSB early, MSB late
  - LSB late, MSB early



Glitch Energy

- Glitch energy (worst case) proportional to: $dt \times 2^{B-1}$
- dt → error in timing & 2^{B-1} associated with half of the switches changing state
- LSB energy proportional to: $T=1/f_s$
- Need $dt \times 2^{B-1} << T$ or $dt << 2^{-B+1}\, T$
- Examples:

f_s [MHz]	B	dt [ps]
1	12	<< 488
20	16	<< 1.5
1000	10	<< 2

→ Timing accuracy for data converters much more critical compared to digital circuitry

DAC Dynamic Errors

- To suppress effect of non-idealities:
  - Retiming of current source control signals
    - Each current source has its own clocked latch incorporated in the current cell
    - Minimization of latch clock skew by careful layout ensuring simultaneous change of bits
  - To minimize control and clock feed through to the output via G-D & G-S of the switches
    - Use of low-swing digital circuitry

DAC Implementation Examples

- Untrimmed segmented
  - T. Miki et al, "An 80-MHz 8-bit CMOS D/A Converter," JSSC December 1986, pp. 983
  - A. Van den Bosch et al, "A 1-GSample/s Nyquist Current-Steering CMOS D/A Converter," JSSC March 2001, pp. 315
- Current copiers:
  - D. W. J. Groeneveld et al, "A Self-Calibration Technique for Monolithic High-Resolution D/A Converters," JSSC December 1989, pp. 1517
- Dynamic element matching:
  - R. J. van de Plassche, "Dynamic Element Matching for High-Accuracy Monolithic D/A Converters," JSSC December 1976, pp. 795

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An 80-MHz 8-bit CMOS D/A Converter

TAKAHIRO MIKI, YASUYUKI NAKAMURA, MASAO NAKAYA, SOTOJU ASAI, YOICHI AKASAKA, AND YASUTAKA HORIBA

8x8 array

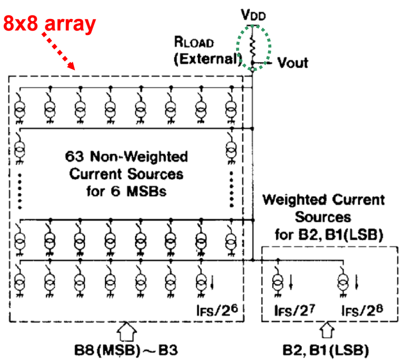


Fig. 1. Basic architecture of the DAC.

2μ tech., 5Vsupply
6+2 segmented

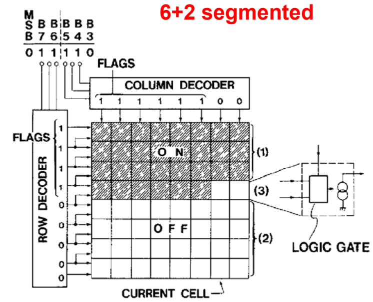
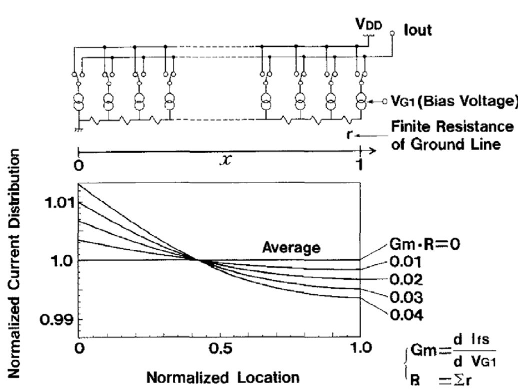


Fig. 2. Two-step decoding.

Two sources of systematic error:
- **Finite current source output resistance**
- **Voltage drop due to finite ground bus resistance**



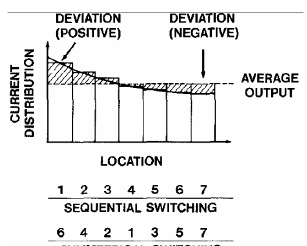
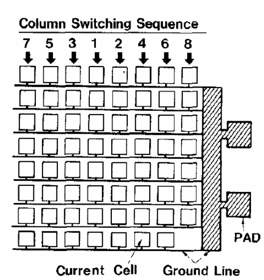


Fig. 9. Symmetrical switching.



Current-Switched DACs in CMOS

Assumptions:
RxI small compared to transistor gate-overdrive
To simplify analysis: Initially, all device currents assumed to be equal to *I*

$$V_{GS_{M2}} = V_{GS_{M1}} - 4RI$$

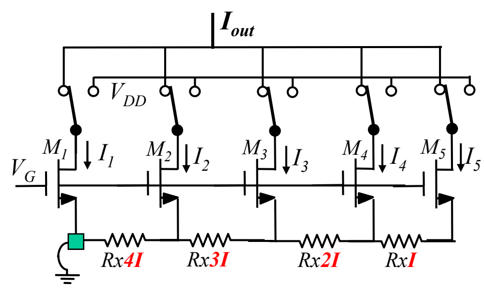
$$V_{GS_{M3}} = V_{GS_{M1}} - 7RI$$

$$V_{GS_{M4}} = V_{GS_{M1}} - 9RI$$

$$V_{GS_{M5}} = V_{GS_{M1}} - 10RI$$

$$I_2 = k\left(V_{GS_{M2}} - V_{th}\right)^2$$

$$I_2 = I_1\left(1 - \frac{4RI}{V_{GS_{M1}} - V_{th}}\right)^2$$



Example: 5 unit element current sources

Current-Switched DACs in CMOS

$$I_2 = k\left(V_{GS_{M2}} - V_{th}\right)^2 = I_1\left(1 - \frac{4RI}{V_{GS_{M1}} - V_{th}}\right)^2$$

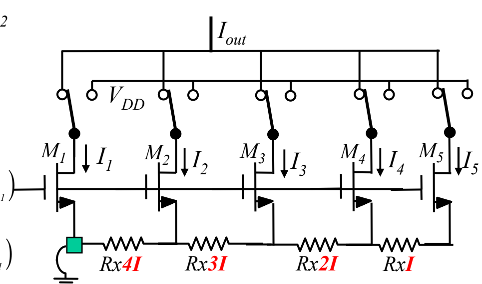
$$g_{m_{M1}} = \frac{2I_1}{V_{GS_{M1}} - V_{th}}$$

$$\rightarrow I_2 = I_1\left(1 - \frac{4Rg_{m_{M1}}}{2}\right)^2 \approx I_1\left(1 - 4Rg_{m_{M1}}\right)$$

$$\rightarrow I_3 = I_1\left(1 - \frac{7Rg_{m_{M1}}}{2}\right)^2 \approx I_1\left(1 - 7Rg_{m_{M1}}\right)$$

$$\rightarrow I_4 = I_1\left(1 - \frac{9Rg_{m_{M1}}}{2}\right)^2 \approx I_1\left(1 - 9Rg_{m_{M1}}\right)$$

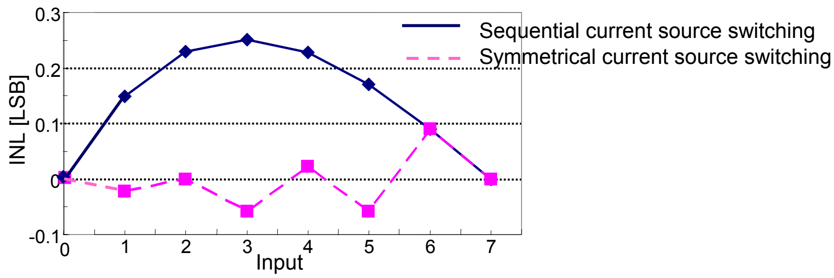
$$\rightarrow I_5 = I_1\left(1 - \frac{10Rg_{m_{M1}}}{2}\right)^2 \approx I_1\left(1 - 10Rg_{m_{M1}}\right)$$



Example: 5 unit element current sources

→ Desirable to have g_m small

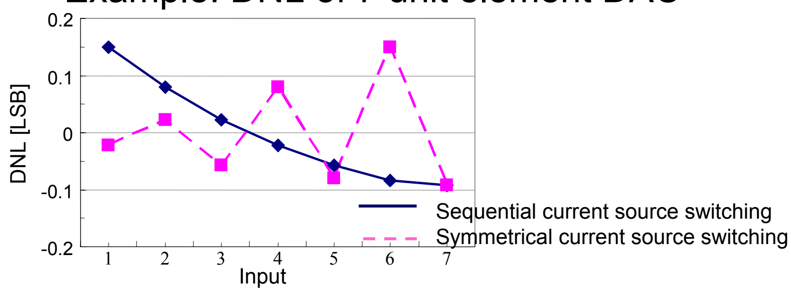
Current-Switched DACs in CMOS
Example: INL of 3-Bit unit element DAC



Example: 7 unit element current source DAC- assume $g_m R=1/100$

- If switching of current sources arranged sequentially (1-2-3-4-5-6-7)
  → $INL= +0.25LSB$
- If switching of current sources symmetrical (4-3-5-2-6-1-7)
  → $INL = +0.09, -0.058LSB$ → INL reduced by a factor of 2.6

Current-Switched DACs in CMOS
Example: DNL of 7 unit element DAC



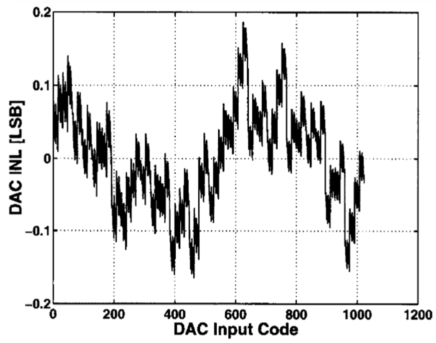
Example: 7 unit element current source DAC- assume $g_m R=1/100$

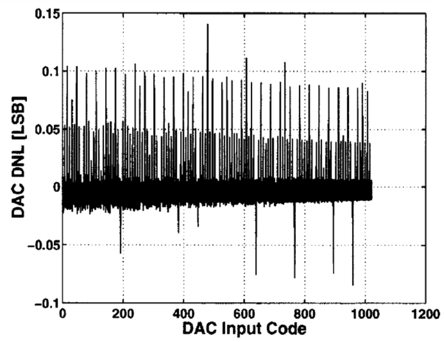
- If switching of current sources arranged sequentially (1-2-3-4-5-6-7)
  → $DNL_{max}= + 0.15LSB$
- If switching of current sources symmetrical (4-3-5-2-6-1-7)
  → $DNL_{max} = + 0.15LSB$
  → DNL unchanged

A 10-bit 1-GSample/s Nyquist Current-Steering CMOS D/A Converter

(5+5)

Anne Van den Bosch, *Student Member, IEEE*, Marc A. F. Borremans, *Student Member, IEEE*, Michel S. J. Steyaert, *Senior Member, IEEE*, and Willy Sansen, *Fellow, IEEE*



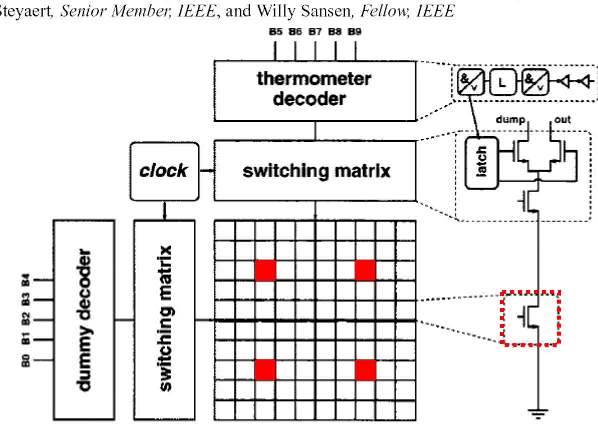


More recent published DAC using symmetrical switching built in 0.35μ/3V analog/1.9V digital, area x10 smaller compared to previous example

A 10-bit 1-GSample/s Nyquist Current-Steering CMOS D/A Converter

Anne Van den Bosch, *Student Member, IEEE*, Marc A. F. Borremans, *Student Member, IEEE*, Michel S. J. Steyaert, *Senior Member, IEEE*, and Willy Sansen, *Fellow, IEEE*

- Layout of Current sources -each current source made of 4 devices in parallel each located in one of the 4 quadrants
- Thermometer decoder used to convert incoming binary digital control for the 5 MSB bits
- Dummy decoder used on the LSB side to match the latency due to the MSB decoder

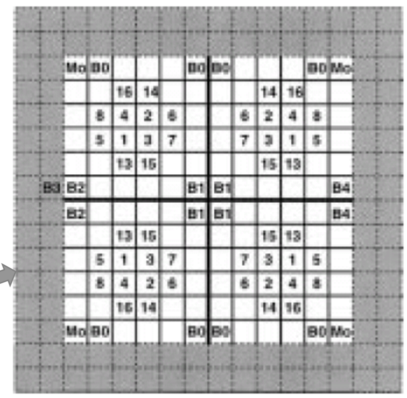


IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 36, NO. 3, MARCH 2001 315

A 10-bit 1-GSample/s Nyquist Current-Steering CMOS D/A Converter

Anne Van den Bosch, *Student Member, IEEE*, Marc A. F. Borremans, *Student Member, IEEE*, Michel S. J. Steyaert, *Senior Member, IEEE*, and Willy Sansen, *Fellow, IEEE*

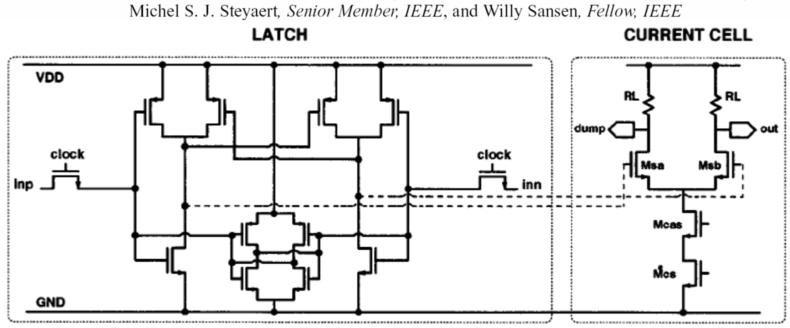
- Current source layout
  - MSB current sources layout in the mid sections of the four quad
  - LSB current sources on the periphery
  - Two rows of dummy current sources added @ the periphery to create identical environment for devices in the center versus the ones on the outer sections



IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 36, NO. 3, MARCH 2001 315

A 10-bit 1-GSample/s Nyquist Current-Steering CMOS D/A Converter

Anne Van den Bosch, *Student Member, IEEE*, Marc A. F. Borremans, *Student Member, IEEE*, Michel S. J. Steyaert, *Senior Member, IEEE*, and Willy Sansen, *Fellow, IEEE*



- Note that each current cell has its clocked latch and clock signal laid out to be close to its switch to ensure simultaneous switching of current sources
- Special attention paid to the final latch to have the cross point of the complementary switch control signal such that the two switches are not both turned off during transition

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A 10-bit 1-GSample/s Nyquist Current-Steering CMOS D/A Converter

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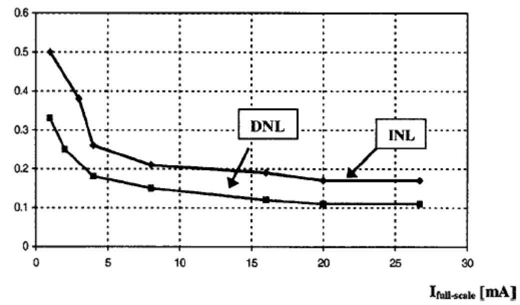


- Measured DNL/INL with current associated with the current cells as variable

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 24, NO. 6, DECEMBER 1989 1517

A Self-Calibration Technique for Monolithic High-Resolution D/A Converters

D. WOUTER J. GROENEVELD, HANS J. SCHOUWENAARS, SENIOR MEMBER, IEEE, HENK A. H. TERMEER, AND CORNELIS A. A. BASTIAANSEN

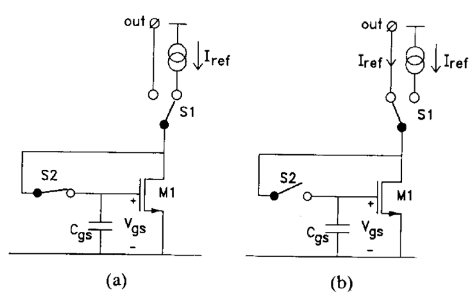
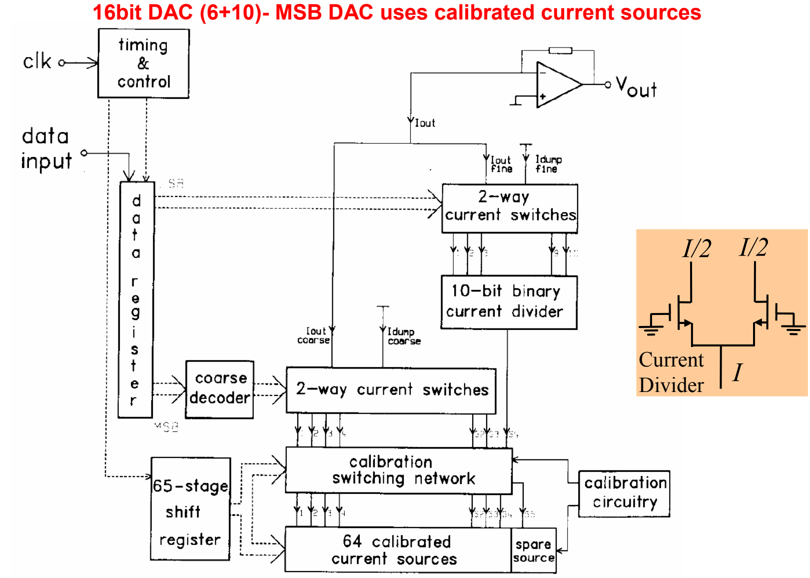
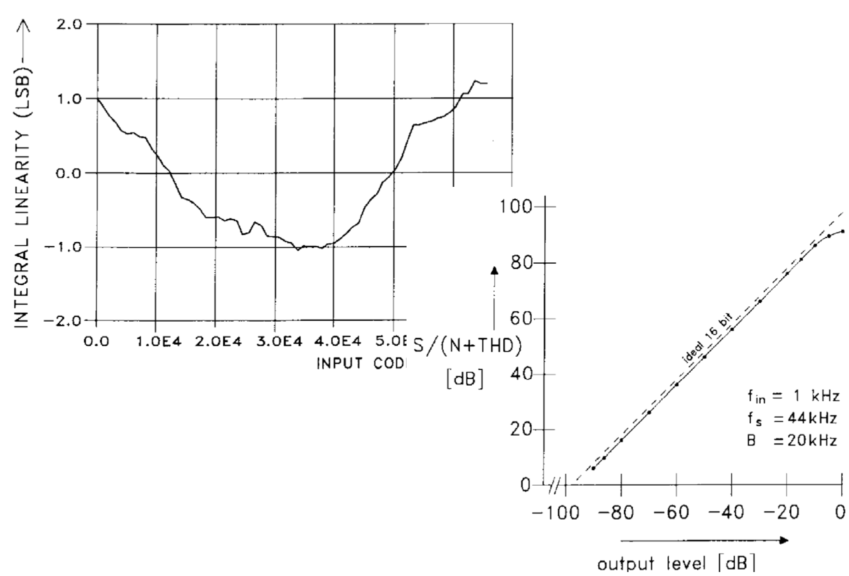


Fig. 2. Calibration principle. (a) Calibration. (b) Operation.

16bit DAC (6+10)- MSB DAC uses calibrated current sources



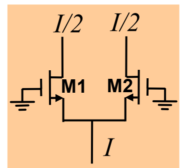


Current Divider Accuracy

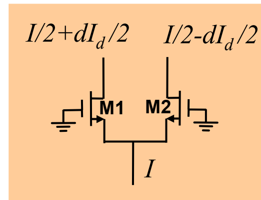
$$I_d = \frac{I_{d1} + I_{d2}}{2}$$

$$\frac{dI_d}{I_d} = \frac{I_{d1} - I_{d2}}{I_d}$$

$$\frac{dI_d}{I_d} = \frac{2}{V_{GS} - V_{th}} \times \left[\left(\frac{d\,W/L}{W/L} \right) + dV_{th} \right]$$



Ideal Current Divider



Real Current Divider
M1& M2 mismatched

→Problem: Device mismatch could severely limit DAC accuracy

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. SC-11, NO. 6, DECEMBER 1976 795

Dynamic Element Matching for High-Accuracy Monolithic D/A Converters

RUDY J. VAN DE PLASSCHE

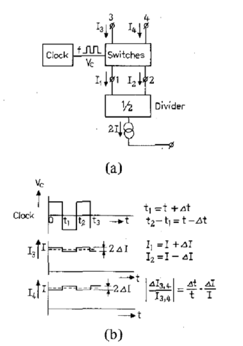


Fig. 2. (a) New current divider schematic diagram. (b) Time dependence of various currents in the new divider.

Dynamic Element Matching

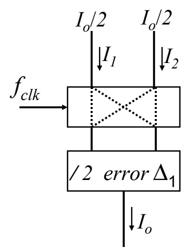
During Φ_1

$$I_1^{(1)} = \frac{1}{2} I_o (1+\Delta_1)$$
$$I_2^{(1)} = \frac{1}{2} I_o (1-\Delta_1)$$

During Φ_2

$$I_1^{(2)} = \frac{1}{2} I_o (1-\Delta_1)$$
$$I_2^{(2)} = \frac{1}{2} I_o (1+\Delta_1)$$

$$\langle I_2 \rangle = \frac{I_2^{(1)} + I_2^{(2)}}{2}$$
$$= \frac{I_o}{2} \frac{(1-\Delta_1)+(1+\Delta_1)}{2}$$
$$\approx \frac{I_o}{2}$$



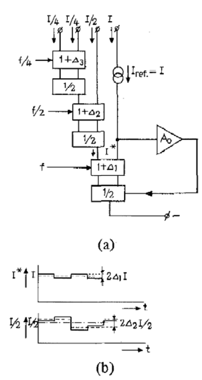
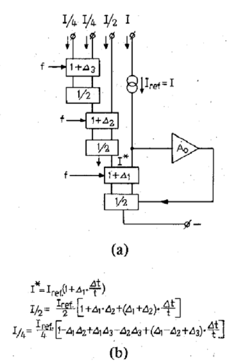


Fig. 4. (a) Binary weighted current network using different switching frequencies. (b) Time dependence of currents flowing in the first and second divider stage.



(a) Binary weighted current network with equal switching frequency. (b) Error analysis results.

Dynamic Element Matching

During Φ_1

$$I_1^{(1)} = \tfrac{1}{2} I_o (1+\Delta_1)$$
$$I_2^{(1)} = \tfrac{1}{2} I_o (1-\Delta_1)$$

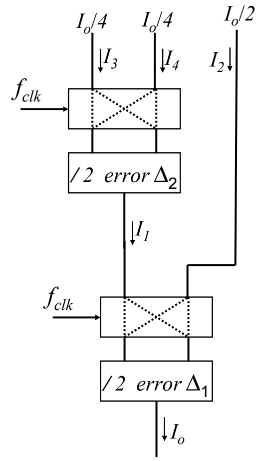
$$I_3^{(1)} = \tfrac{1}{2} I_1^{(1)} (1+\Delta_2)$$
$$= \tfrac{1}{4} I_o (1+\Delta_1)(1+\Delta_2)$$

During Φ_2

$$I_1^{(2)} = \tfrac{1}{2} I_o (1-\Delta_1)$$
$$I_2^{(2)} = \tfrac{1}{2} I_o (1+\Delta_1)$$

$$I_3^{(2)} = \tfrac{1}{2} I_1^{(2)} (1-\Delta_2)$$
$$= \tfrac{1}{4} I_o (1-\Delta_1)(1-\Delta_2)$$

$$\langle I_3 \rangle = \frac{I_3^{(1)} + I_3^{(2)}}{2}$$
$$= \frac{I_o}{4} \frac{(1+\Delta_1)(1+\Delta_2) + (1-\Delta_1)(1-\Delta_2)}{2}$$
$$= \frac{I_o}{4}(1+\Delta_1\Delta_2)$$



E.g. $\Delta_1 = \Delta_2 = 1\%$ → matching error is $(1\%)^2 = 0.01\%$

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. SC-11, NO. 6, DECEMBER 1976 795

Dynamic Element Matching for High-Accuracy Monolithic D/A Converters

RUDY J. VAN DE PLASSCHE

- Bipolar 12-bit DAC using dynamic element matching built in 1976
- Element matching clock frequency 100kHz
- INL <0.25LSB!

12-BIT D/A TEST CHIP

D/A NETWORK DATA	
Resolution :	12 bit
Accuracy :	≤1/4 L.S.B. or $5 \cdot 10^{-5}$ (linearity)
Output current :	2 mA
Temp. Coeff. of output current :	5 ppm/°C
Voltage Coeff. of output current :	1 ppm/V
Chip size :	2.5 x 2.5 mm
Max. clock freq. for dynamic matching :	100 kHz
Power supply :	-15V

ISSCC 2004 / SESSION 20 / DIGITAL-TO-ANALOG CONVERTERS / 20.1

20.1 A 3V CMOS 400mW 14b 1.4GS/s DAC for Multi-Carrier Applications

Bernd Schafferer and Richard Adams

Example: State-of-the-Art current steering DAC

6bit unit-element
8bit binary

Max Sample Frequency	1.4	GSPS
Resolution	14	Bit
DNL	+/- 0.8	LSB
INL	+/- 2.1	LSB
SFDR @ 1.0 GSPS	> 60	dB
IMD @ 1.0 GSPS	> 64	dBc
NSD @ f_{out} = 400MHz	-155	dBm/Hz
Power (Core) @1.4GSPS	200	mW
Power(Total) @ 1.4GSPS	400	mW
Area (Core)	0.8	mm^2
Area (Chip)	6.25	mm^2

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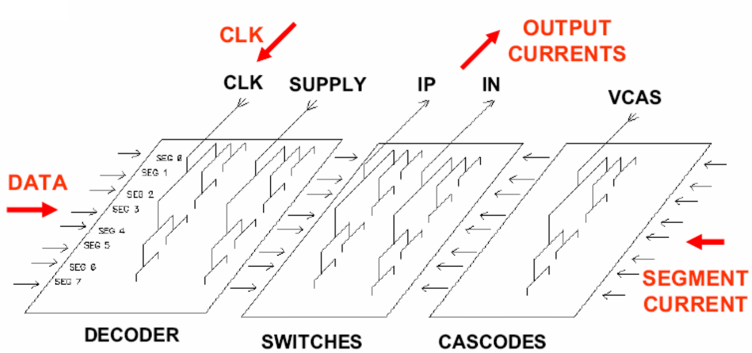
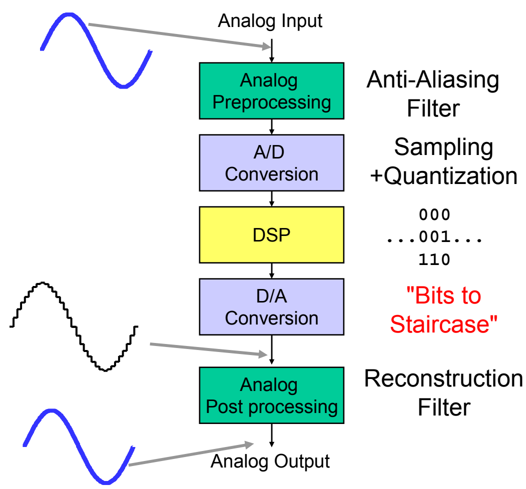
20.1 A 3V CMOS 400mW 14b 1.4GS/s DAC for Multi-Carrier Applications

Layout Tree Structures



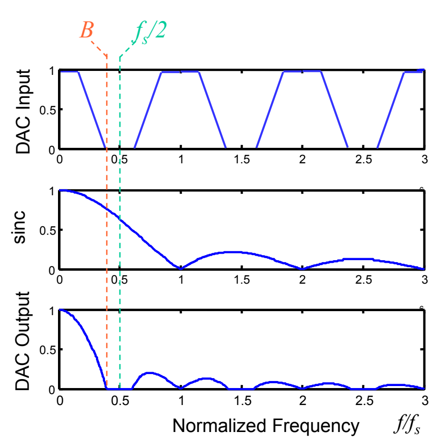
DAC In the Big Picture

- Learned to build DACs
  - Convert the incoming digital signal to analog
- DAC output → staircase form
- Some applications require filtering (smoothing) of DAC output
  → reconstruction filter

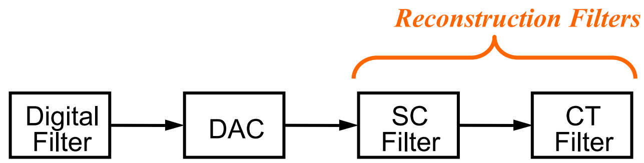


DAC Reconstruction Filter

- Need for and requirements depend on application
- Tasks:
  - Correct for sinc droop
  - Remove "aliases" (stair-case approximation)

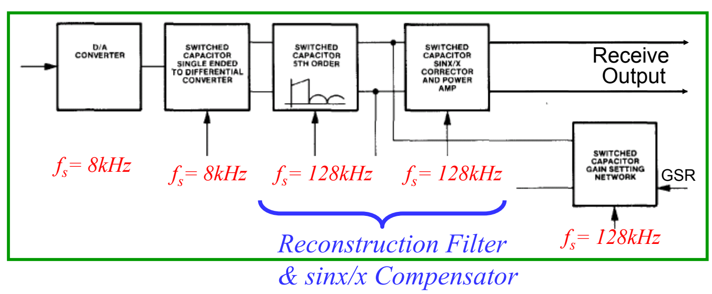


Reconstruction Filter Options



- Digital and SC filter possible only in combination with oversampling (signal bandwidth B << $f_s/2$)
- Digital filter
  - Band limits the input signal → prevent aliasing
  - Could also provide high-frequency pre-emphasis to compensate in-band sinc amplitude droop associated with the inherent DAC S/H function

DAC Reconstruction Filter Example: Voice-Band CODEC Receive Path



Note: $f_{sig}^{max} = 3.4kHz$

$f_s^{DAC} = 8kHz$

$\rightarrow sin(\pi f_{sig}^{max} x\ T_s)/(\pi f_{sig}^{max} x T_s)$

$= -2.75$ *dB droop due to DAC sinc shape*

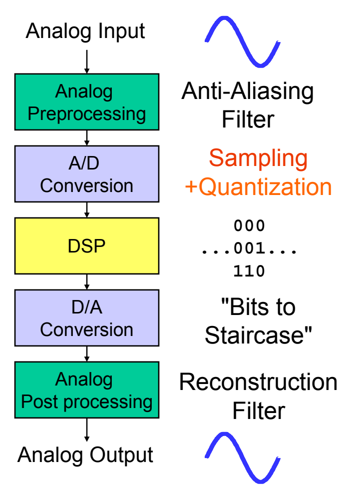
Ref: D. Senderowicz et. al, "A Family of Differential NMOS Analog Circuits for PCM Codec Filter Chip," *IEEE Journal of Solid-State Circuits,* Vol.-SC-17, No. 6, pp.1014-1023, Dec. 1982.

Summary
D/A Converter

- D/A architecture
  - Unit element – complexity proportional to 2^B- excellent DNL
  - Binary weighted- complexity proportional to B- poor DNL
  - Segmented- unit element MSB(B_1)+ binary weighted LSB(B_2)
    → Complexity proportional $((2^{B1}-1) + B_2)$ -DNL compromise between the two
- Static performance
  - Component matching
- Dynamic performance
  - Time constants, Glitches
- DAC improvement techniques
  - Symmetrical switching rather than sequential switching
  - Current source self calibration
  - Dynamic element matching
- Depending on the application, reconstruction filter may be needed

What Next?

- ADC Converters:
  - Need to build circuits that "sample“
  - Need to build circuits for amplitude quantization



Analog-to-Digital Converters

- Two categories:
  - Nyquist rate ADCs → $f_{sig}^{max} \sim 0.5xf_{sampling}$
    - Maximum achievable signal bandwidth higher compared to oversampled type
    - Resolution limited to max. 12-14bits
  - Oversampled ADCs → $f_{sig}^{max} << 0.5xf_{sampling}$
    - Maximum achievable signal bandwidth significantly lower compared to nyquist
    - Maximum achievable resolution high (18 to 20bits!)