EE247
Lecture 10
Supplemental Material for S.C. Filters

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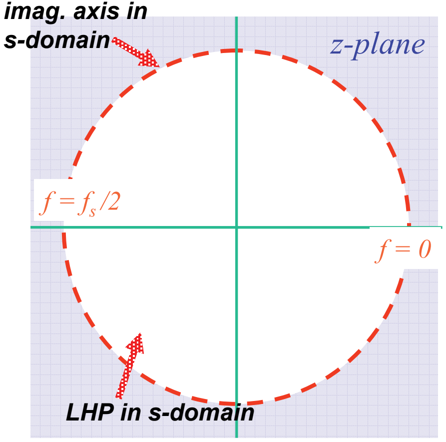
z-Domain Frequency Response

- The jω axis maps onto the unit-circle
- LHP singularities in s-plane map into inside of unit-circle in z-domain
- RHP singularities in s-plane map into outside of unit-circle in z-domain
- Particular values:
  - $f = 0 \rightarrow z = 1$
  - $f = f_s/2 \rightarrow z = -1$

$$z = e^{s.Ts}$$

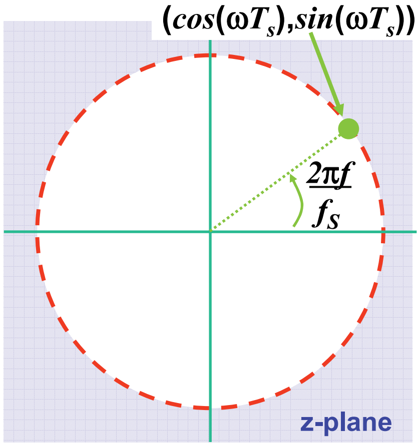


z-Domain Frequency Response

- The frequency response is obtained by evaluating H(z) on the unit circle at:

  $z = e^{j\omega T} = cos(\omega T_s) + j\,sin(\omega T_s)$

- Once z=-1 (f_s/2) is reached, the frequency response repeats, as expected
- The angle to the pole is equal to 360° (or 2π radians) times the ratio of the pole frequency to the sampling frequency



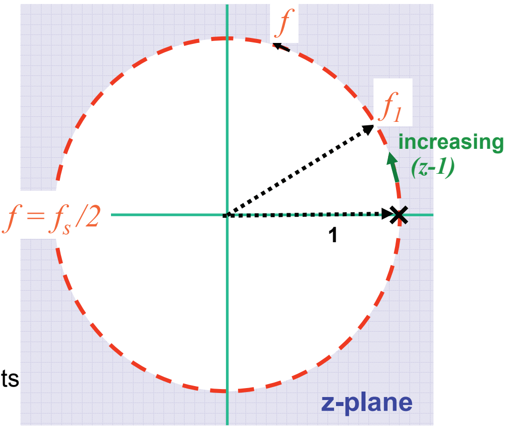
DDI Integrator
Pole-Zero Map in z-Plane

z -1=0 → z = 1
on unit circle

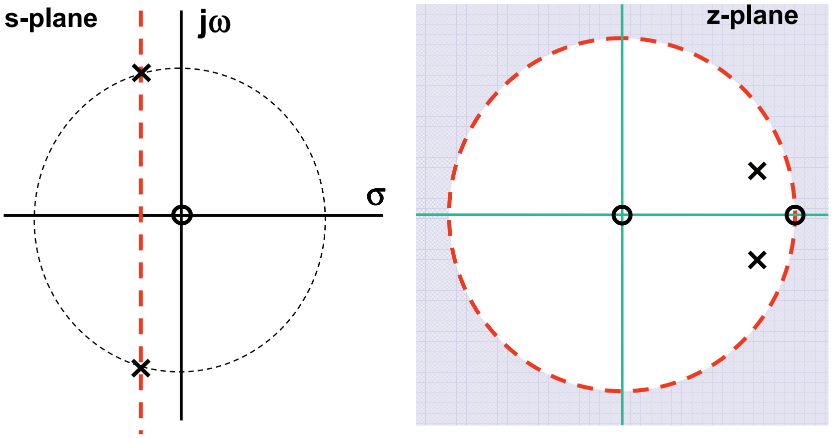
Pole from f → 0
in s-plane mapped to z =+1

As frequency increases z domain point moves on unit circle (CCW)

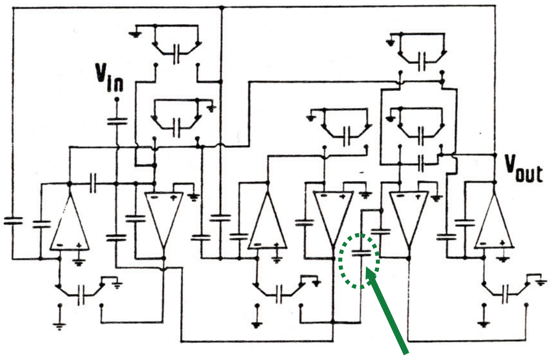
Once frequency gets to:
z=-1 (f=f_s/2)
→ frequency response repeats



Example: 2^{nd} Order LDI Bandpass Filter s-Plane versus z-Plane



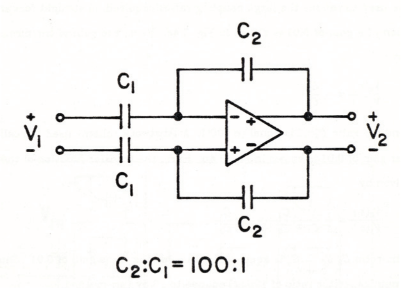
Sixth-Order Elliptic LDI Bandpass Filter

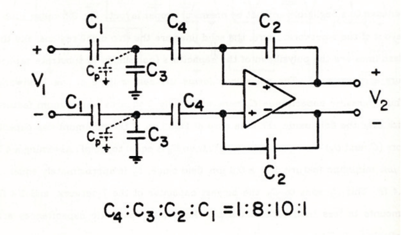


Transmission Zero

Ref: Tat C. Choi, "High-Frequency CMOS Switched-Capacitor Filters," U. C. Berkeley, Department of Electrical Engineering, Ph.D. Thesis, May 1983 (ERL Memorandum No. UCB/ERL M83/31).

Use of T-Network





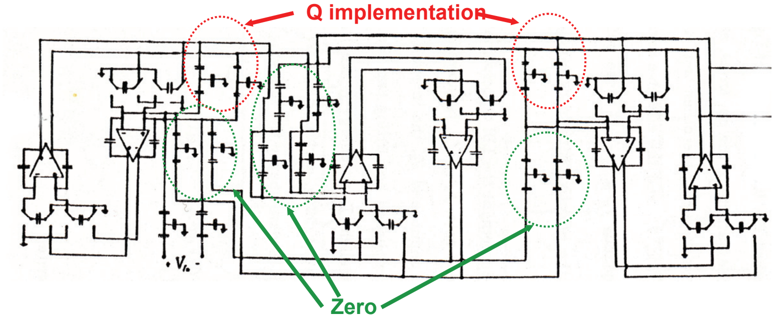
$$\frac{V_2}{V_1} = -\frac{C_1}{C_2}$$

$$\frac{V_2}{V_1} = -\frac{C_1}{C_2} \times \frac{C_4}{C_1 + C_3 + C_4}$$

High Q filter → large cap. ratio for Q & transmission zero implementation
To reduce large ratios required → T-networks utilized

Ref: Tat C. Choi, "High-Frequency CMOS Switched-Capacitor Filters," U. C. Berkeley, Department of Electrical Engineering, Ph.D. Thesis, May 1983 (ERL Memorandum No. UCB/ERL M83/31).

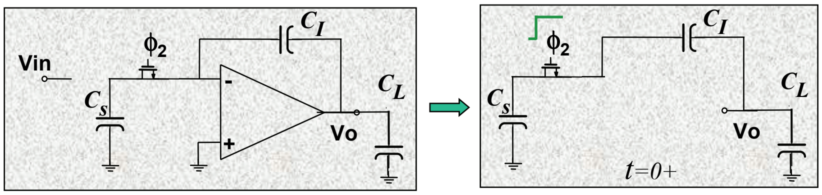
Sixth Order Elliptic Bandpass Filter Utilizing T-Network



- **T-networks utilized** for:
  - **Q implemention**
  - **Transmission zero implementation**

Ref: Tat C. Choi, "High-Frequency CMOS Switched-Capacitor Filters," U. C. Berkeley, Department of Electrical Engineering, Ph.D. Thesis, May 1983 (ERL Memorandum No. UCB/ERL M83/31).

More Realistic Switched-Capacitor Circuit Slew Scenario



At the instant C_s connects to input of opamp (t=0+)

→ Opamp not yet active at t=0+ due to finite opamp bandwidth → delay

→ Feedforward path from input to output generates a voltage spike at the output with polarity opposite to final Vo step- spike magnitude function of C_I, C_L, C_s

→ Spike increases slewing period

→ Eventually, opamp becomes active - starts slewing followed by subsequent settling

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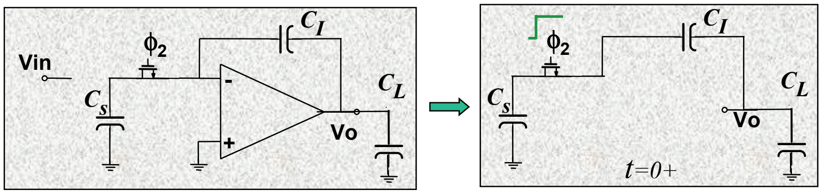
Switched-Capacitor Circuit
Opamp not Active @ t=0+



$$\textit{Charge sharing}: C_s V_{Cs}^{t0-} = V_{Cs}^{t0+}\left(C_s + C_{eq}\right) \quad \textit{where } C_{eq} = \frac{C_I C_L}{C_I + C_L}$$

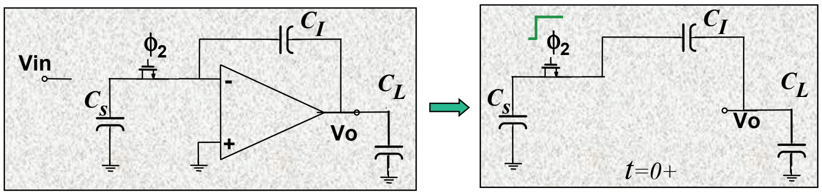
$$\Delta V_{out}^{t0+} = V_{Cs}^{t0+} \frac{C_I}{C_I + C_L} = V_{Cs}^{t0-} \frac{C_s}{C_s + C_{eq}} \times \frac{C_I}{C_I + C_L}$$

$$\textit{Assuming } C_L << C_s << C_I \rightarrow C_{eq} \approx C_L \rightarrow C_s V_{Cs}^{t0-} \approx V_{Cs}^{t0+}\left(C_s + C_L\right) \rightarrow V_{Cs}^{t0-} \approx V_{Cs}^{t0+}$$

$$\rightarrow \Delta V_{out}^{t0+} \approx V_{Cs}^{t0-} \frac{C_s}{C_s + C_L} \times \frac{C_I}{C_I + C_L} \approx V_{Cs}^{t0-}$$

$$\textit{Note that } \Delta V_{out}^{final} \approx -\frac{C_s}{C_I} V_{Cs}^{t0+} \approx -\frac{C_s}{C_I} V_{Cs}^{t0-}$$

More Realistic Switched-Capacitor Circuit Slew Scenario



Notice that if C_L is large → some of the charge stored on Cs is lost prior to opamp becoming effective → operation looses accuracy

$$Charge\ sharing:\ C_s V_{Cs}^{t0-} = V_{Cs}^{t0+}\left(C_s + C_{eq}\right)\quad where\ C_{eq} = \frac{C_I C_L}{C_I + C_L}$$

$$V_{Cs}^{t0+} = V_{Cs}^{t0-}\frac{C_s}{C_s + C_{eq}} = V_{Cs}^{t0-}\frac{C_s}{C_s + \frac{C_I C_L}{C_I + C_L}}$$

→ Partly responsible for S.C. filters only good for low-frequency applications

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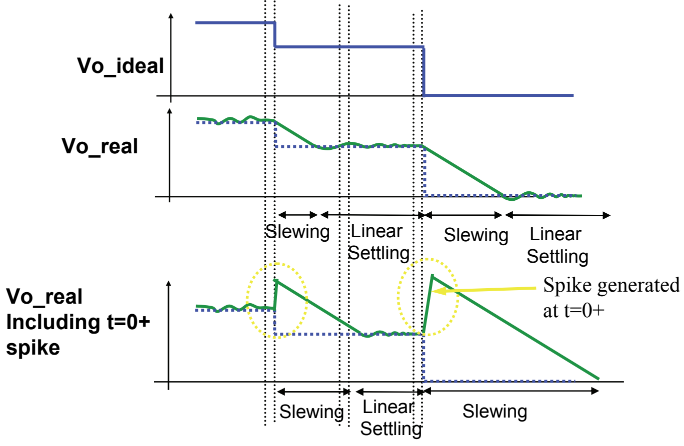
More Realistic S.C. Slew Scenario



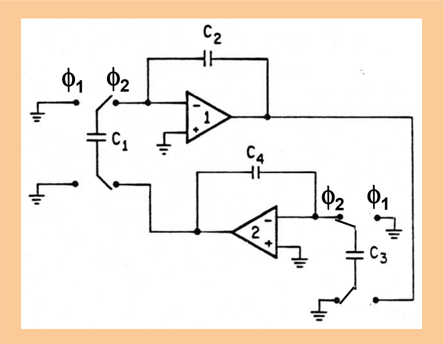
Ref: R. Castello, “Low Voltage, Low Power Switched-Capacitor Signal Processing Techniques," U. C. Berkeley, Department of Electrical Engineering, Ph.D. Thesis, Aug. ‘84 (ERL Memorandum No. UCB/ERL M84/67).

Extending the Maximum Achievable Critical Frequency of Switched-Capacitor Filters

Consider a switched-capacitor resonator:

Regular sampling:
Each opamp is busy settling only during one of the two clock phases

→ Idle during the other clock phase

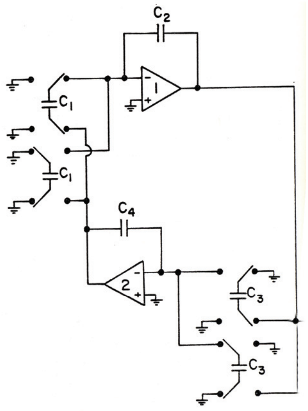


Note: During ϕ_1 both opamps are idle

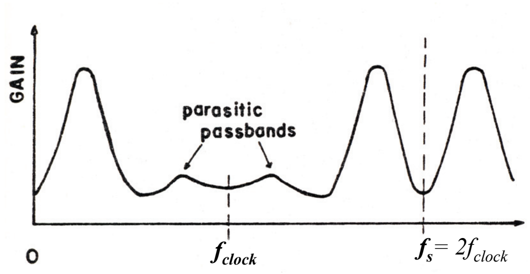
Switched-Capacitor Resonator Using Double-Sampling

Double-sampling:

- 2nd set of switches & sampling caps added to all integrators
- While one set of switches/caps sampling the other set transfers charge into the intg. cap
- Opamps busy during both clock phases
- **Effective sampling freq. twice the clock freq. while opamp bandwidth requirement remains the same**



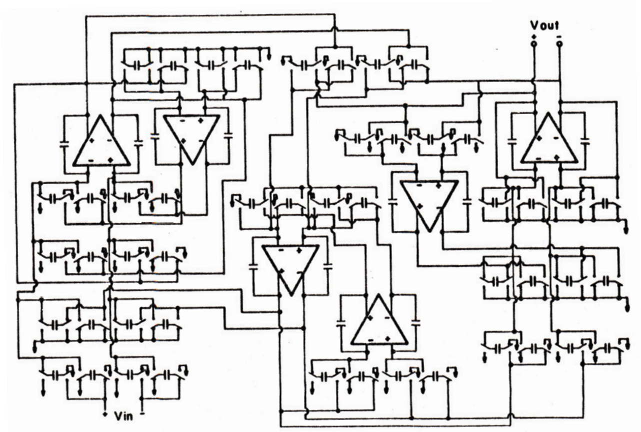
Double-Sampling Issues



Issues to be aware of:
- Jitter in the clock
- Unequal clock phases
-Mismatch in sampling caps.
→ parasitic passbands

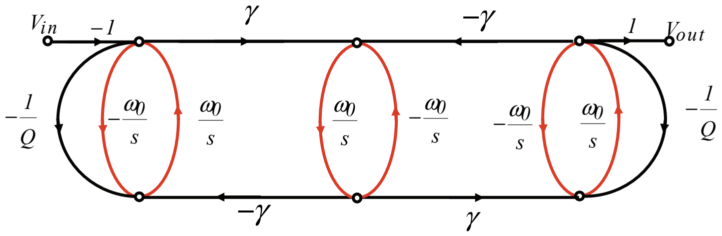
Ref: Tat C. Choi, "High-Frequency CMOS Switched-Capacitor Filters," U. C. Berkeley, Department of Electrical Engineering, Ph.D. Thesis, May 1983 (ERL Memorandum No. UCB/ERL M83/31).

Double-Sampled Fully Differential S.C. 6th Order All-Pole Bandpass Filter

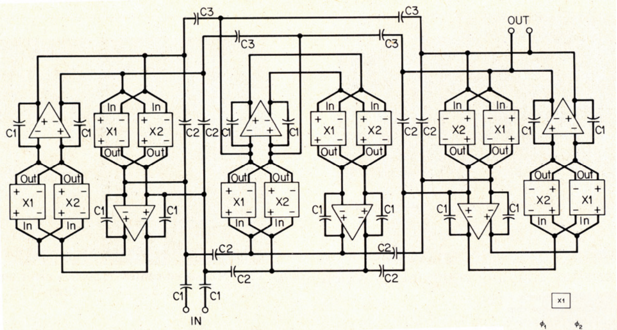


Ref: Tat C. Choi, "High-Frequency CMOS Switched-Capacitor Filters," U. C. Berkeley, Department of Electrical Engineering, Ph.D. Thesis, May 1983 (ERL Memorandum No. UCB/ERL M83/31).

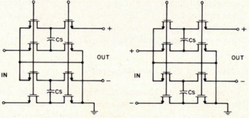
Sixth Order Bandpass Filter Signal Flowgraph



Double-Sampled Fully Differential 6th Order S.C. All-Pole Bandpass Filter



- Cont. time termination (Q) implementation
- Folded-Cascode opamp with $f_u = 100MHz$ used
- Center freq. $3.1MHz$ (Measured error $>1\%$), filter $Q=55$
- Clock freq. $12.83MHz$ → effective oversampling ratio 8.27
- Measured dynamic range $46dB$ ($IM3=1\%$)



Ref: B.S. Song, P.R. Gray "Switched-Capacitor High-Q Bandpass Filters for IF Applications," *IEEE Journal of Solid State Circuits,* Vol. 21, No. 6, pp. 924-933, Dec. 1986.