EE247
Lecture 10

• Switched-capacitor filters (continued)
  – Switched-capacitor integrators
    • DDI & LDI integrators
      – Effect of parasitic capacitance
      – Bottom-plate integrator topology
  – Switched-capacitor resonators
  – Bandpass filters
  – Lowpass filters
  – Switched-capacitor filter design considerations
    • Termination implementation
    • Transmission zero implementation
    • Limitations imposed by non-idealities

Switched-Capacitor Integrator

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Switched-Capacitor Integrator
Output Sampled on $\phi_1$

\[ Q_s[(n-1)Ts] = C_s V_i[(n-1)Ts] \]

\[ Q_I[(n-1)Ts] = Q_I[(n-3/2)Ts] \]

\[ Q_s[(n-1/2)Ts] = 0 \]

\[ Q_I[(n-1/2)Ts] = Q_I[(n-1)Ts] + Q_s[(n-1)Ts] \]

\[ Q_s[nTs] = C_s V_i[nTs] \]

\[ Q_I[nTs] = Q_I[(n-1)Ts] + Q_s[(n-1)Ts] \]

Since $V_{out} = -Q_s/C_s$ & $V_i = Q_s/C_s$:

\[ C_s V_{out}(nTs) = C_s V_{out}[(n-1)Ts] - C_s V_i[(n-1)Ts] \]
Switched-Capacitor Integrator
Output Sampled on $\phi_1$

\[ C_I \ V_o(nT_s) = C_I \ V_o((n-1)T_s) - C_s \ V_{in}((n-1)T_s) \]
\[ V_o(nT_s) = V_o((n-1)T_s) - C_s \ V_{in}((n-1)T_s) \]
\[ V_o(Z) = Z^{-1}V_o(Z) - Z^{-1}C_s \ V_{in}(Z) \]
\[ \frac{V_o(Z)}{V_{in}} = -\frac{C_s}{C_I} \times \frac{Z^{-1}}{1-Z^{-1}} \]

DDI (Direct-Transform Discrete Integrator)

Switched-Capacitor Direct-Transform Discrete Integrator

\[ \frac{V_o(z)}{V_{in}} = -\frac{C_s}{C_I} \times \frac{z^{-1}}{1-z^{-1}} \]
\[ = -\frac{C_s}{C_I} \times \frac{1}{z-1} \]
### DDI Switched-Capacitor Integrator

\[
\frac{V_o(z)}{V_{in}} = -\frac{C_s}{C_f} \times \frac{z^{-1} - \frac{1}{1 + z^{-1}}}{1 - z^{-1}} = -\frac{C_s}{C_f} \times \frac{z^{-1} - \frac{1}{1 + z^{-1}}}{1 - z^{-1}}
\]

since: \( \sin(\alpha) = \frac{e^{j\alpha} - e^{-j\alpha}}{2j} \)

\[
= -\frac{C_s}{C_f} \times \frac{1 - \frac{1}{2\sin(\alpha/2)}}{2\sin(\alpha/2)} \times e^{-j\alpha/2}
\]

### Example: Mag. & phase error for:

1. \( f/f_s = 1/12 \) → Mag. error = 1% or 0.1dB
   - Phase error = 15 degree
   - \( Q_{in} = -3.8 \)

2. \( f/f_s = 1/32 \) → Mag. error = 0.16% or 0.014dB
   - Phase error = 5.6 degree
   - \( Q_{in} = -10.2 \)

DDI Integrator:
- magnitude error no problem
- phase error major problem
5th Order Low-Pass Switched Capacitor Filter
Built with DDI Integrators

Example:
5th Order Elliptic Filter
Singularities pushed towards RHP due to integrator excess phase

Switched Capacitor Filter
Build with DDI Integrator

Continuous-Time Prototype
Switched-Capacitor Integrator
Output Sampled on $\phi_2$

Sample output $\frac{1}{2}$ clock cycle earlier
$\rightarrow$ Sample output on $\phi_2$

$\Phi_1 \rightarrow Q_s[(n-1)T_s] = C_s V_i[(n-1)T_s], \quad Q_i[(n-1)T_s] = Q_i[(n-3/2)T_s]$

$\Phi_2 \rightarrow Q_s[(n-1/2)T_s] = 0, \quad Q_i[(n-1/2)T_s] = Q_i[(n-3/2)T_s] + Q_s[(n-1)T_s]$

$\Phi_1 \rightarrow Q_s[nT_s] = C_s V_i[nT_s], \quad Q_i[nT_s] = Q_i[(n-1)T_s] + Q_s[(n-1)T_s]$

$\Phi_2 \rightarrow Q_s[(n+1/2)T_s] = 0, \quad Q_i[(n+1/2)T_s] = Q_i[(n+1/2)T_s] + Q_s[nT_s]$
\[ Q_I[(n+1/2)T_s] = Q_I[(n-1/2)T_s] + Q_s[nT_s] \]
\[ V_{o2} = -\frac{Q_I}{C_I} & V_I = \frac{Q_s}{C_s} \]

Using the z operator rules:
\[ C_I V_{o2}z^{1/2} = C_I V_{o2}z^{-1/2} - C_s V_i \]

**Switched-Capacitor Integrator**

**LDI Switched-Capacitor Integrator**

LDI (Lossless Discrete Integrator) \( \rightarrow \)
same as DDI but output is sampled \( \frac{1}{2} \) clock cycle earlier

\[ \frac{V_{o2}(z)}{V_{in}} = -\frac{C_s}{C_I} \times \frac{z^{-1/2}}{1-z^{-1}} \]

\[ = -\frac{C_s}{C_I} \times \frac{\frac{1}{2} e^{j\omega T / 2}}{1 - e^{j\omega T / 2}} \]

\[ = \frac{C_s}{C_I} \times \frac{1}{2 \sin(j\omega T / 2)} \]

For signals at frequencies \(<<\) sampling freq.

\( \Rightarrow \) Magnitude error negligible

No Phase Error!
Switched-Capacitor Filter
Built with LDI Integrators

\[ |H(j\omega)| \]

Zeros Preserved

\[ f_s/2 \quad f_s \quad 2f_s \quad f \]

Switched-Capacitor Integrator
Parasitic Capacitor Sensitivity

Effect of parasitic capacitors:
1. \( C_{p1} \) - driven by opamp o.k.
2. \( C_{p2} \) - at opamp virtual gnd o.k.
3. \( C_{p3} \) – Charges to \( V_{in} \) & discharges into \( C_i \)

\[ \text{Problem parasitic capacitor sensitivity} \]
Parasitic Insensitive
Bottom-Plate Switched-Capacitor Integrator

Sensitive parasitic cap. \( C_{p1} \) → rearrange circuit so that \( C_{p1} \) does not charge/discharge

\[ \phi_1 = 1 \rightarrow C_{p1} \text{ grounded} \]

\[ \phi_2 = 1 \rightarrow C_{p1} \text{ at virtual ground} \]

Solution: Bottom plate capacitor integrator

Note:
Different delay from \( Vi^+ \) & \( Vi^- \) to either output
\( \rightarrow \) Special attention needed for input/output connections to ensure LDI realization

Output/Input

<table>
<thead>
<tr>
<th>( Vi^+ ) on ( \phi_1 )</th>
<th>( Vi^- ) on ( \phi_2 )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \frac{C_s}{C_f} \frac{z^{-1}}{1-z^{-1}} )</td>
<td>( \frac{C_s}{C_f} \frac{z^{-1/2}}{1-z^{-1/2}} )</td>
</tr>
<tr>
<td>( \frac{C_s}{C_f} \frac{z^{-1}}{1-z^{-1}} )</td>
<td>( -\frac{C_s}{C_f} \frac{1}{1-z^{-1}} )</td>
</tr>
</tbody>
</table>
Bottom Plate Switched-Capacitor Integrator
z-Transform Model

\[ z^{-1/2} \]

\[ z^{-1/2} \]

Input/Output z-transform

Vi+

Cs

Vi-

\( \phi_1 \)

\( \phi_2 \)

Vo1

Vo2

LDI

Delay around integrator loop is \( (z^{-1/2} \cdot z^{1/2} = 1) \) \( \Rightarrow \) LDI function
Switched-Capacitor LDI Resonator

\[ \omega_1 = \frac{1}{R_{eq} C_2} f_s \frac{C_1}{C_2} \]
\[ \omega_2 = \frac{1}{R_{eq} C_4} f_s \frac{C_3}{C_4} \]

Fully Differential Switched-Capacitor Resonator

• Note: Two sets of S.C. bottom plate networks for each differential integrator
Switched-Capacitor LDI Bandpass Filter
Utilizing Continuous-Time Termination

\[ a_0 = f_s \times \frac{C_3}{C_4} = f_s \times \frac{C_1}{C_2} \]
\[ Q = \frac{C_2}{C_4} \]

\[ f_0 = \frac{1}{2\pi} f_s \times \frac{C_1}{C_2} \]
\[ \Delta f = \frac{f_0}{Q} = \frac{1}{2\pi} f_s \times \frac{C_1 C_Q}{C_2 C_4} \]

Both accurately determined by cap ratios & clock frequency
Fifth Order All-Pole LDI Low-Pass Ladder Filter
Complex Conjugate Terminations

Termination Resistor

Complex conjugate terminations (alternate phase switching)

Sixth-Order Elliptic LDI Bandpass Filter

Effect of Opamp Nonidealities on Switched Capacitor Filter Behaviour

• Opamp finite gain

• Opamp finite bandwidth

• Finite slew rate of the opamp

• Non-linearity associated with opamp output/input characteristics

Effect of Opamp Non-Idealities
Finite DC Gain

\[ H(s) = -f_s \frac{C_s}{C_I} \frac{I}{s + f_s \frac{C_s}{C_I} \frac{L}{a}} \]

\[ H(s) = -\frac{a_0}{s + a_0 \frac{s}{a}} \]

\[ \Rightarrow Q_{intg} = a \]

- Finite DC gain same effect in S.C. filters as for C.T. filters
- If DC gain not high enough → lowing of overall Q & droop in passband

Effect of Opamp Non-Idealities
Finite Opamp Bandwidth

Assumption-
Opamp → does not slew (will be revisited)
Opamp has only one pole only → exponential settling

Effect of Opamp Non-Idealities

Finite Opamp Bandwidth

\[ H_{\text{actual}}(Z) = H_{\text{ideal}}(Z) \left[ 1 - e^{-k + \frac{1}{2} \pi} \frac{C_l}{C_l + C_s} Z^{-1} \right] \]

where \( k = \pi \times \frac{f_t}{C_1 f_s} \)

\( f_t \rightarrow \text{Opamp unity-gain-frequency} \), \( f_s \rightarrow \text{Clock frequency} \)


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Effect of Opamp Finite Bandwidth on Filter Magnitude Response

Magnitude deviation due to finite opamp unity-gain-frequency

Example: 2nd order bandpass with Q=25

Effect of Opamp Finite Bandwidth on Filter Magnitude Response

For 1dB magnitude response deviation:

1. $f_c/f_s=1/12$
   $f_c/f_t~0.04$
   $f_t>25f_c$

2. $f_c/f_s=1/32$
   $f_c/f_t~0.022$
   $f_t>45f_c$

3. Cont.-Time
   $f_c/f_t=1/700$
   $f_t>700f_c$

Example:


Effect of Opamp Finite Bandwidth on Filter Critical Frequency

Critical frequency deviation due to finite opamp unity-gain-frequency

Example: 2nd order filter

Effect of Opamp Finite Bandwidth on Filter Critical Frequency

Example:
For maximum critical frequency shift of <1%
1. $f_c/f_s=1/32$
   $f_c/f_t=0.028$
   $\Rightarrow f_t > 36f_c$
2. $f_c/f_s=1/12$
   $f_c/f_t=0.046$
   $\Rightarrow f_t > 22f_c$
3. Active RC
   $f_c/f_t=0.008$
   $\Rightarrow f_t > 125f_c$


Opamp Bandwidth Requirements for Switched-Capacitor Filters Compared to Continuous-Time Filters

- Finite opamp bandwidth causes phase lag at the unity-gain frequency of the integrator for both type filters
  $\Rightarrow$ Results in negative intg. Q & thus increases overall Q and gain at results in peaking in the passband in the frequency range of interest
- For given filter requirements, opamp bandwidth requirements much less stringent for S.C. filters compared to cont. time filters
  $\Rightarrow$ Lower power dissipation for S.C. filters (at low freq.s only due to other effects)
- Finite opamp bandwidth causes down shifting of critical frequencies in both type filters
  - Since cont. time filters are usually tuned $\Rightarrow$ tuning accounts for frequency deviation
  - S.C. filters are untuned and thus frequency shift could cause problems specially for narrow-band filters
Sources of Distortion in Switched-Capacitor Filters

- Opamp output/input transfer function non-linearity- similar to cont. time filters
- Capacitor non-linearity, similar to cont. time filters
- Distortion induced by finite slew rate of the opamp
- Distortion incurred by finite setting time of the opamp
- Distortion due to switch clock feed-through and charge injection

What is Slewing?

Assumption:
Integrator opamp is a simple class A transconductance type differential pair with fixed tail current, $I_{ss}=\text{const.}$
What is Slewing?

|\[|V_{Cs}| > V_{max}\] | Output current constant \[I_o = \frac{I_{ss}}{2}\] or \[-\frac{I_{ss}}{2}\] 
|\[\Rightarrow\] | Constant current charging/discharging \[C_f\]; \[V_o\] ramps down/up | Slewing

After \[V_{Cs}\] is discharged enough to have:
|\[|V_{Cs}| < V_{max}\] | \[I_o = \frac{gm}{C_f} V_{Cs}\] | Exponential or over-shoot settling

Distortion Induced by Opamp Finite Slew Rate

Multiple pole settling

One pole settling
Ideal Switched-Capacitor Output Waveform

$\phi_1, \phi_2$

$\phi_2$, High $\rightarrow$ Charge transferred from $C_s$ to $C_I$

Slew Limited Switched-Capacitor Integrator

Output Slewing & Settling
Distortion Induced by Finite Slew Rate of the Opamp


Distortion Induced by Opamp Finite Slew Rate

- Error due to exponential settling changes linearly with signal amplitude
- Error due to slew-limited settling changes non-linearly with signal amplitude (doubling signal amplitude X4 error)

→ For high-linearity need to have either high slew rate or non-slewing opamp

\[ H_D = \frac{V_o}{S_0 T_s} \frac{8 (\sin \frac{a_0 T_s}{2})^2}{\pi k (k^2 - 4)} \]

\[ H_D = \frac{V_o}{S_0 T_s} \frac{8 (\sin \frac{a_0 T_s}{2})^2}{f_0 << f_s \rightarrow HD_3 = \frac{8 \pi V_o T_s f_s^2}{75 S_0 f_s}} \]

Example:
Slew Related Harmonic Distortion

\[ HD_3 = \frac{V_o}{S_r T_s} \left( \frac{\sin \left( \frac{a_0 T_s}{2} \right)}{15\pi} \right) \]

\[ HD_3 = \frac{8\pi V_o f_o^2}{15S_r f_s} \]

Switched-capacitor filter with 4kHz bandwidth, \( f_s = 128kHz, S_r = 1V/\mu \text{sec}, V_o = 3V \)


Distortion Induced by Finite Slew Rate of the Opamp

- Note that for a high order switched capacitor filter \( \rightarrow \) only the last stage slewing will affect the output linearity (as long as the previous stages settle to the required accuracy)
  - Can reduce slew limited linearity by using an amplifier with a higher slew rate \textit{only} for the last stage
  - Can reduce slew limited linearity by using class A/B amplifiers
    - Even though the output/input characteristics is non-linear as long as the DC open-loop gain is high, the significantly higher slew rate compared to class A amplifiers helps improve slew rate induced distortion

- In cases where the output is sampled by another sampled data circuit (e.g. an ADC or a S/H) \( \rightarrow \) no issue with the slewing of the output as long as the output settles to the required accuracy & is sampled at the right time
Sources of Noise in Switched-Capacitor Filters

- Opamp Noise
  - Thermal noise
  - \( 1/f \) (flicker) noise
- Thermal noise associated with the switching process \((kT/C)\)
  - Same as continuous-time filters
- Precaution regarding aliasing of noise required

Switched-Capacitor Filter Application
Example: Voice-Band Codec (Coder-Decoder) Chip

CODEC Transmit Path
Lowpass Filter Frequency Response

Note: \( f_s = 128\text{kHz} \)

CODEC Transmit Path
Highpass Filter

Note: \( f_s = 8\text{kHz} \)
Low Q bandpass ($Q < 1$) filter shape → Implemented with lowpass followed by highpass

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**CODEC Transmit Path**

**Clocking & Anti-Aliasing Scheme**

First filter (1\textsuperscript{st} order RC type) performs anti-aliasing for the next S.C. biquad

The 1\textsuperscript{st} & 2\textsuperscript{nd} stage filters form 3\textsuperscript{rd} order elliptic LPF with corner frequency @ 32kHz → Anti-aliasing for the next lowpass filter

The stages prior to the high-pass perform anti-aliasing for high-pass

Notice gradual lowering of clock frequency → Ease of anti-aliasing
SC Filter Summary

- Pole and zero frequencies proportional to:
  - Sampling frequency $f_s$
  - Capacitor ratios
  - High accuracy and stability in response
  - Long time constants realizable without requiring large value $R$
- Compatible with transconductance amplifiers
  - Reduced circuit complexity, power dissipation
- Amplifier bandwidth requirements less stringent compared to CT filters (low frequencies only)

**Issue:** Sampled-data filters require anti-aliasing prefiltering

Switched-Capacitor Filters versus Continuous-Time Filter Limitations

Considering overall effects of:
- Opamp finite slew rate
- Opamp finite unity-gain-bandwidth
- Opamp settling issues
- Clock feedthru
- Switch+ sampling cap. finite time-constant

$\rightarrow$ Limited switched-capacitor filter performance frequency range
### Summary

**Filter Performance versus Filter Topology**

<table>
<thead>
<tr>
<th>Filter Type</th>
<th>Max. Usable Bandwidth</th>
<th>SNDR</th>
<th>Freq. tolerance w/o tuning</th>
<th>Freq. tolerance + tuning</th>
</tr>
</thead>
<tbody>
<tr>
<td>Opamp-RC</td>
<td>~10MHz</td>
<td>60-90dB</td>
<td>+-30-50%</td>
<td>1-5%</td>
</tr>
<tr>
<td>Opamp-MOSFET-C</td>
<td>~5MHz</td>
<td>40-60dB</td>
<td>+-30-50%</td>
<td>1-5%</td>
</tr>
<tr>
<td>Opamp-MOSFET-RC</td>
<td>~5MHz</td>
<td>50-90dB</td>
<td>+-30-50%</td>
<td>1-5%</td>
</tr>
<tr>
<td>Gm-C</td>
<td>~100MHz</td>
<td>40-70dB</td>
<td>+-40-60%</td>
<td>1-5%</td>
</tr>
<tr>
<td>Switched Capacitor</td>
<td>~10MHz</td>
<td>40-90dB</td>
<td>&lt;&lt;1%</td>
<td></td>
</tr>
</tbody>
</table>