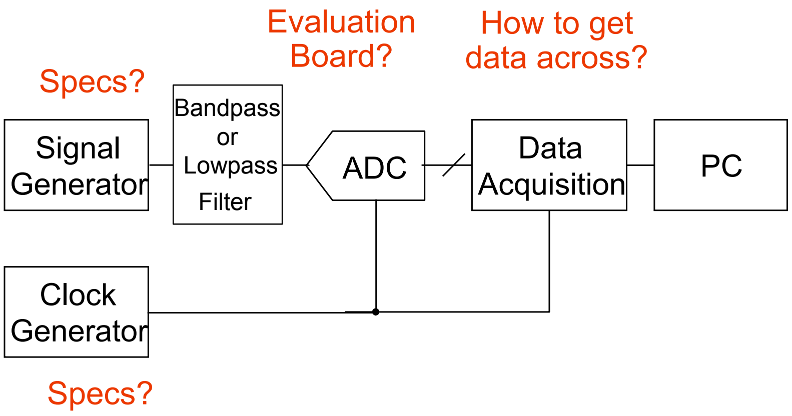
EE247
Lecture 15

- Data Converters
  - Practical aspects of converter testing
    - Evaluation board considerations
  - D/A converter design
    - Architectures
    - Performance
      - Static
      - Dynamic

Summary Last Lecture

- Data Converters
  - Spectral testing
    - Integer number of cylces for test signal → f_{sig} has to be locked to f_s
    - Windowing
  - Practical aspects of converter testing
    - Signal source
    - Clock generator

ADC Test Setup



Evaluation Board?

How to get data across?

Specs?

Signal Generator

Bandpass or Lowpass Filter

ADC

Data Acquisition

PC

Clock Generator

Specs?

Evaluation Board

- Planning begins with converter pin-out
  - Example of poor pin-out→ clock pin right next to a digital output...
- Not "Black Magic", but weeks of design time and studying
- Key aspects
  - Supply/ground routing, bypass capacitors
  - Coupling between signals
- Good idea to look at ADC vendor datasheets for example layouts/schematics/application notes

Vendor Eval Board Layout

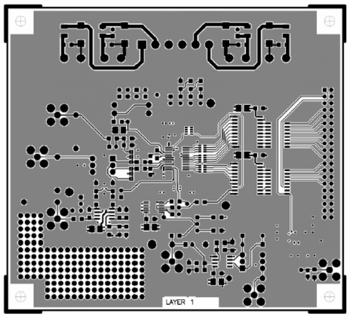


Figure 21. TSSOP Evaluation Board Layout, Primary Side

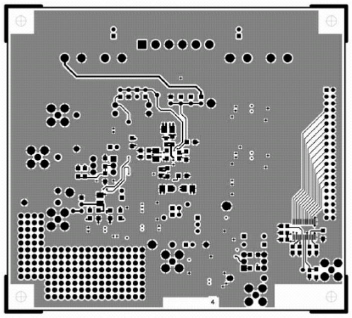


Figure 22. TSSOP Evaluation Board Layout, Secondary Side

[Analog Devices AD9235 Data Sheet]

One thing to remember...

- A converter does not just have one "input" pin but:
  - Clock
  - Power Supply, Ground
  - Reference Voltage
- For good practices on how to avoid issues see e.g.:
  - Analog Devices Application Note 345**:** "Grounding for Low-and-High-Frequency Circuits"
  - Maxim Application Note 729**:** "Dynamic Testing of High-Speed ADCs, Part 2"

How to Get the Bits Off Chip?

- "Full swing" CMOS signaling works well for f_{CLK}<100MHz- For higher frequencies:
  – Uncontrolled characteristic impedance
  – High swing→ higher level of spurious coupling to other signals
  – Low power efficiency
- But we want to build faster ADCs...
- Alternative to CMOS: LVDS – Low Voltage Differential Signaling
- LVDS vs. CMOS:
  – Higher speed, more power efficient at high speed
  – Two pins/bit!

LVDS Outputs

- Output in the form of current

- Transmission lines layouted out to have 50OHM char. Imp.

- Termination resistor off-chip
  → More accurate matching to transmission line impedance

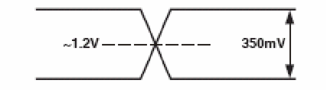
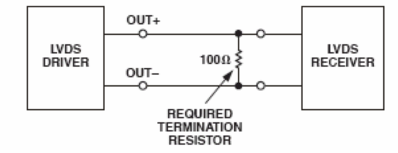


Figure 1. LVDS Output Levels



Ref: Analog Devices Application Note 586: "LVDS Data Outputs for High Speed ADCs"

LVDS Outputs

- Since signal is differential→ spurious coupling to/from other nodes tend to cancel
- Constant current drawn from supply → less glitches on the line
- Less power hungry at: f >100MHz

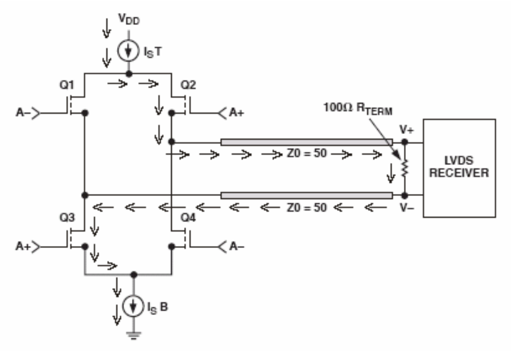
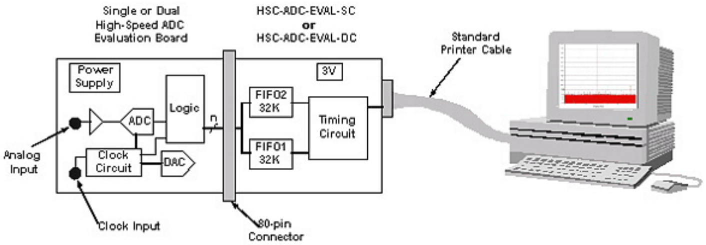


Figure 4. LVDS Output Current

Ref: Analog Devices Application Note 586**:** "LVDS Data Outputs for High Speed ADCs"

Data Acquisition

- Several options:
  - – Logic analyzer with PC interface
  - – FIFO board, interface to PC DAQ card
  - – Vendor kit, simple interface to printer port:

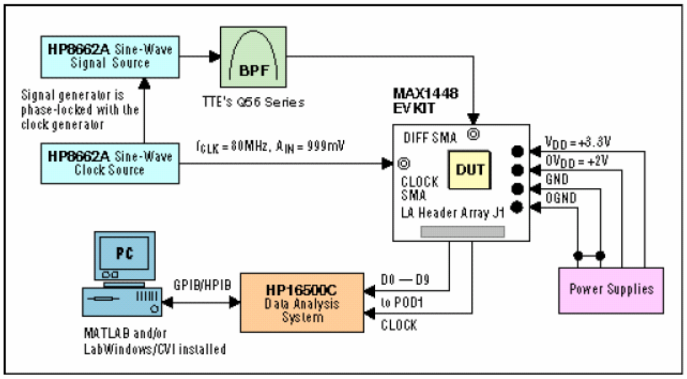


[Analog Devices, High-Speed ADC FIFO Evaluation Kit]

Post-Processing

- LabView (DAQ Software Toolbox)
- Matlab
- Some vendors provide example source code
- E.g. Maxim Application Note 1819**:** "Selecting the Optimum Test Tones and Test Equipment for Successful High-Speed ADC Sine Wave Testing"

Example: Complete ADC Test Setup


HP8662A Sine-Wave Signal Source
BPF
TTE's Q56 Series
Signal generator is phase-locked with the clock generator
HP8662A Sine-Wave Clock Source
f_{CLK} = 80MHz, A_{IN} = 999mV
MAX1448 EV KIT
DIFF SMA
CLOCK SMA
DUT
LA Header Array J1
V_{DD} = +3.3V
OV_{DD} = +2V
GND
OGND
Power Supplies
PC
GPIB/HPIB
HP16500C Data Analysis System
D0 — D9
to POD1
CLOCK
MATLAB and/or LabWindows/CVI installed

[Maxim Application Note 729**:** "Dynamic Testing of High-Speed ADCs, Part 2]

Debugging

- State-of-the-art converters almost always yield surprises in silicon
  - If models anticipate everything, the application probably isn't state-of-the-art
- Analog designers and mixed-signal architects at times invent new circuits while measuring in the lab
- How do we debug converters?
  - Start with a simple time domain test. Does the captured digital waveform look like a sine wave?
  - Begin your DFT/INL signature analysis by scaling down sampling frequencies and signal input frequencies together
  - If you can't explain performance with essentially infinite settling times, don't add dynamic errors to the mix

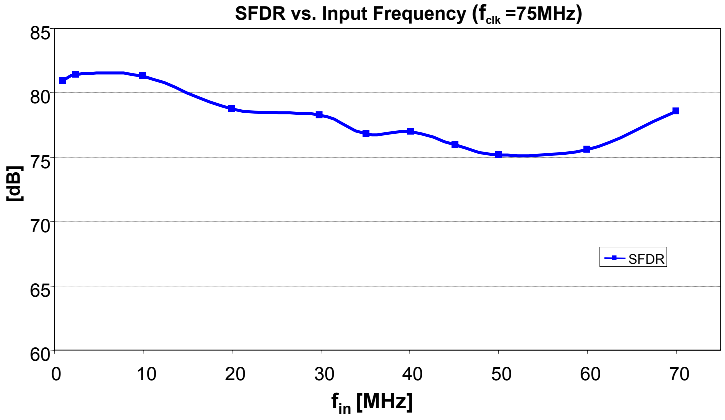
Debugging

- Typical problems come from non-idealities never built into your "model"
  - E.g. half-circuit models for fully-differential circuits inherently can't explain some types of differential-symmetry errors
- You can't afford to rediscover old non-idealities in new silicon
  - Talking to veterans early in the modeling phase can be important

Debugging

- Design teams usually track down and fix single-cause problems quickly
- Problems due to circuit interactions are much more difficult to debug, try to avoid by good design/layout
- Interaction examples:
  - Digital activity-dependent clock jitter
    - S/(N+D) degradation only happens when large amplitude, high frequency analog inputs coincide with the offending digital activity
  - Distortion cancellation
    - Nonlinear phenomena don’t obey superposition

Debugging



- Cancellation of Nonlinearities?

Debugging

- Never assume all of your data is good
  - One bad data set can “rule out” the correct explanation, leading you astray forever
- "Compare measurements to themselves“
- But, noise is a random variable, and the noise power in 1000 time samples will vary from DFT to DFT
- How big an effect is this?

Debugging

- Can show that:
  - Variation of noise in 1000 samples yields a standard deviation in SNR of 0.2dB
  - This means that 68.3% of all DFTs will produce SNRs within 0.2dB of the average
  - 99.7% of 1000 point DFTs yield SNRs within ±0.6dB of the average
- If you’re seeing ADC noise variation of greater than ±0.6dB in the lab, some sort of interference is usually the culprit

Testing & Debugging

- Always try to use two independent measurement methods to verify important results
  - Correlate INL & SFDR, DNL & SNR
- Comparing time domain and frequency domain views of the same measurement is good practice
  - e.g. DNL & SNR

Debugging and testing of state-of-the-art circuitry
→ Non-trivial
→ Need to plan ahead

D/A Converters

- D/A architecture examples
  - Unit element (thermometer)
  - Binary weighted
- Static performance
  - Limited by component matching
  - Architectures
    - Unit element
    - Binary weighted
    - Segmented
  - Dynamic element matching
- Dynamic performance
  - Limited by timing errors causing glitches

D/A Converters

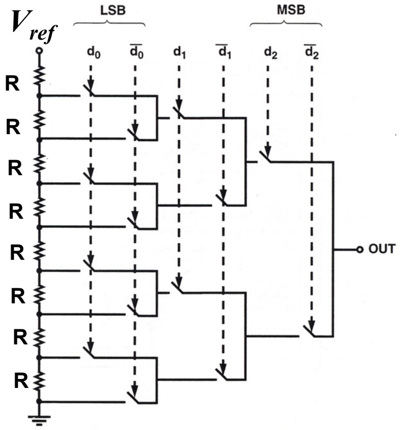
- Comprises voltage or charge or current based elements
- Examples for above three categories:
  - Resistor string → voltage
  - Charge redistribution → charge
  - Current source type → current

Resistor String DAC

Voltage based:

2^B resistors in series
All resistors equal

→ **Generates 2^B equally spaced voltages ready to be chosen based on the digital input word**



R-String DAC Example

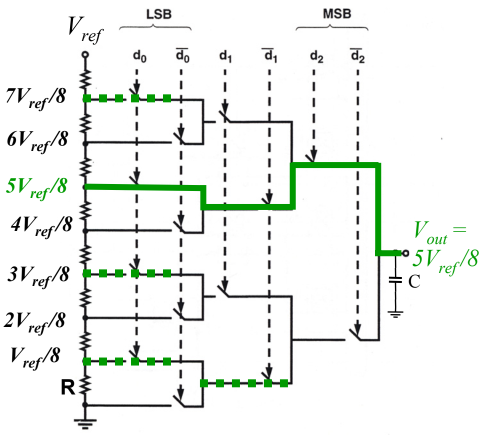
Example:

- Input code ***101***

  → $V_{out} = 5V_{ref}/8$

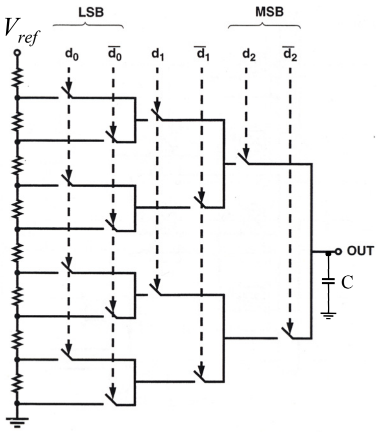
- Assuming switch resistance << ***R:***

$$\tau_{settling} = (3R||5R) \times C$$
$$= 0.23 \times 8RC$$



R-String DAC

- Advantages:
  - Takes full advantage of availability of almost perfect switches in MOS technologies
  - Simple, fast for <8-10bits
  - Inherently monotonic
  - Compatible with purely digital technologies
- Disadvantages:
  - 2^B resistors & ~2×2^B switches for B bits → High element count & large area for B >10bits
  - High settling time for B > 10: $\tau_{max} \sim 0.25 \times 2^B RC$



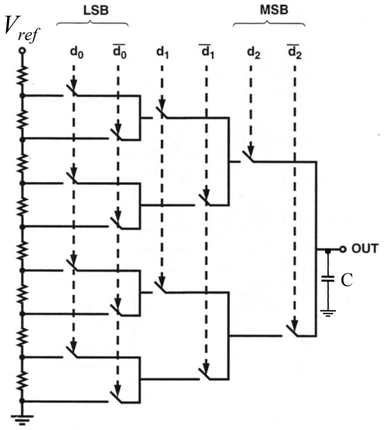
Ref:

M. Pelgrom, “A 10-b 50-MHz CMOS D/A Converter with 75-W Buffer,” JSSC, Dec. 1990, pp. 1347

R-String DAC

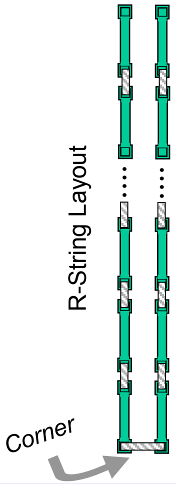
- Resistor size
  - Since maximum output settling time:

    $\tau_{max} \sim 0.25 \times 2^B RC$
  - Choice of resistor size directly affects DAC maximum operating speed
  - Power dissipation function of $V_{ref}^2 / (Rx2^B)$
    - → Tradeoff between speed and power dissipation
- Resistor type:
  - Choice of resistive material important
  - Diffusion type R → high temp. co. & voltage co.
    - Results in poor INL/DNL
  - Better choice is poly resistor beware of poly R 1/f noise
  - At times thin film or metal R used



R-String DAC
Layout Considerations

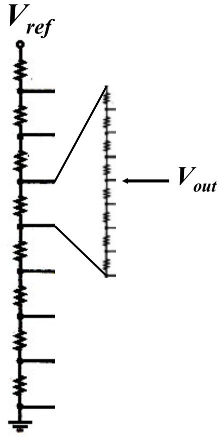
- Number of resistor segments → 2^B
  - E.g. 10-bit R-string DAC →1024 resistors
- Low INL/DNL dictates good R matching
- Layout quite a challenge
  - Good matching dictates all R segments either vertical or horizontal - not both
  - Need to fold the string
    - Difficult to match corner segments to rest
    - Could result in large INL/DNL



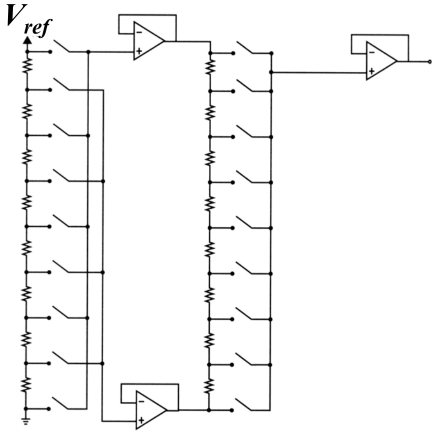
R-String DAC
Including Interpolation

Resistor string DAC
+ Resistor string interpolator increases resolution w/o drastic increase in complexity
e.g. 6bit DAC→ (3bit +3bit→ $2x2^3=2^4$ # of Rs) instead of direct 6bit→2^6

Considerations:
- ❑Main R-string loaded by the interpolation string
- ❑Large R values → less loading but lower speed
- ❑Can use buffers



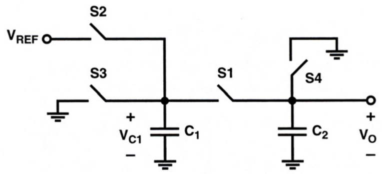
R-String DAC
Including Interpolation

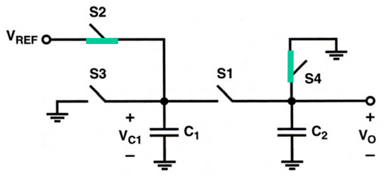


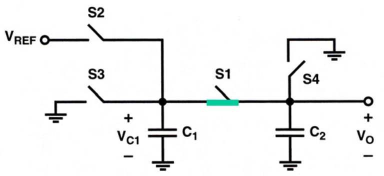
Use buffers, to prevent loading of the main ladder
Issues:
- → Buffer offset
- → Speed

Serial Charge Redistribution DAC Simplified Operation

Nominally C_1=C_2



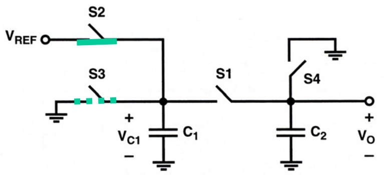


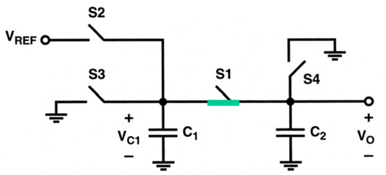


- Operation sequence:
  - Initialize: Discharge C2 & charge C1 to V_{REF} → S2& S4 closed
  - Charge share: close S1→ V_{C2}=V_{C1}=V_{REF}/2

Serial Charge Redistribution DAC Simplified Operation (Cont'd)

Nominally C_1=C_2



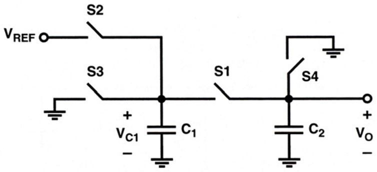


- Operation sequence:
  - Next cycle
    - If S3 closed V_{C1}=0 then when S1 closes V_{C1} = V_{C2} = V_{REF}/4
    - If S2 closed V_{C1}=V_{REF} then when S1 closes V_{C1} =V_{C2} =V_{REF}/2+V_{REF}/4

Serial Charge Redistribution DAC

- Nominally $C_1=C_2$
- Operation sequence:
  - Discharge C1 & C2→ S3& S4 closed
  - For each bit in succession beginning with LSB, b_1:
    - S1 open- if b_i=1 C1 precharge to V_{REF} if b_i=0 discharged to GND
    - S2 & S3 & S4 open- S1 closed- Charge sharing C1 & C2

      → ½ of precharge on C1 +½ of charge previously stored on C2→ C2



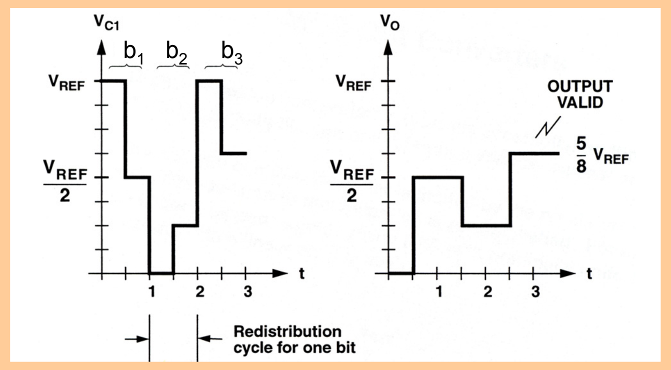
$$V_o(1) = \frac{b_N}{2}V_{REF}$$

$$V_o(2) = \frac{1}{2}\left(b_{N-1} + \frac{b_N}{2}\right)V_{REF}$$

$$\vdots$$

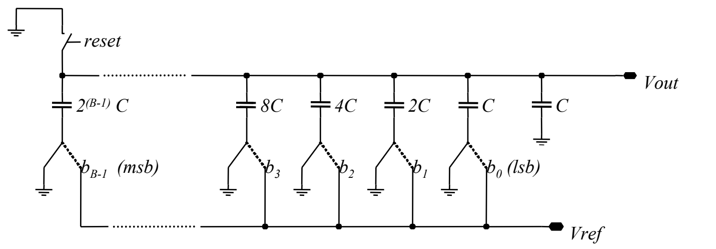
$$V_o(N) = \left(\sum_{i=1}^{N}\frac{b_i}{2^i}\right)V_{REF}$$

Serial Charge Redistribution DAC
Example: Input Code 101



- Example input code 101→ output (1/8 +0/8 +4/8)V_{REF} =5/8 V_{REF}
- Very small area
- N redistribution cycles for N-bit conversion → quite slow

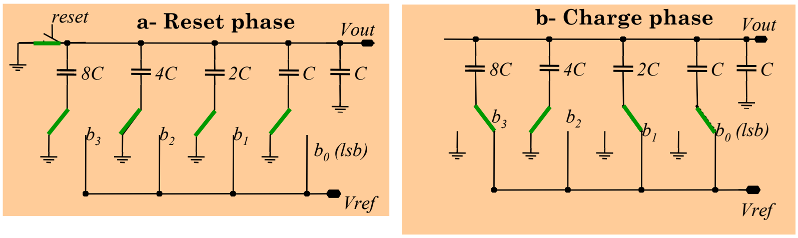
Parallel Charge Scaling DAC



$$V_{out} = \frac{\sum_{i=0}^{B-1} b_i 2^i C}{2^B C} V_{ref}$$

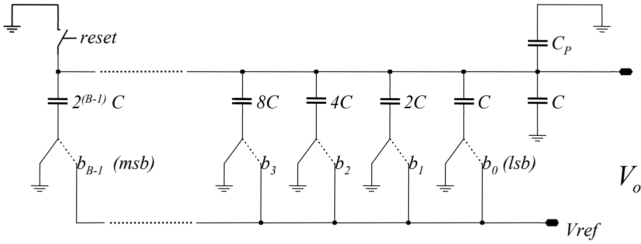
- E.g. "Binary weighted"
- B+1 capacitors & switches (Cs built of unit elements → 2^B cap units)

Charge Scaling DAC
Example: 4Bit DAC- Input Code 1011



$$V_{out} = \frac{2^0 C + 2^1 C + 2^3 C}{2^4 C} V_{ref} = \frac{11}{16} V_{ref}$$

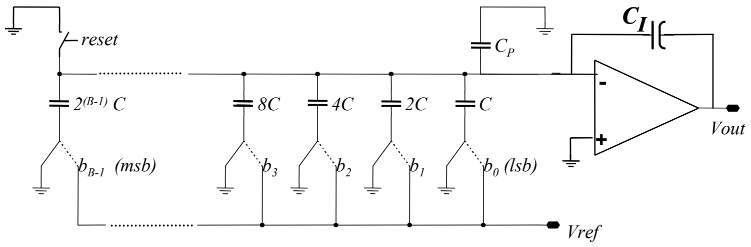
Charge Scaling DAC



$$V_{out} = \frac{\sum_{i=0}^{B-1} b_i 2^i C}{2^B C + C_P} V_{ref}$$

- Sensitive to parasitic capacitor @ output
  - If C_p constant → gain error
  - If C_p voltage dependant → DAC nonlinearity
- Large area of caps for high DAC resolution (10bit DAC ratio 1:512)
- Monotonicity depends on element matching (more later)

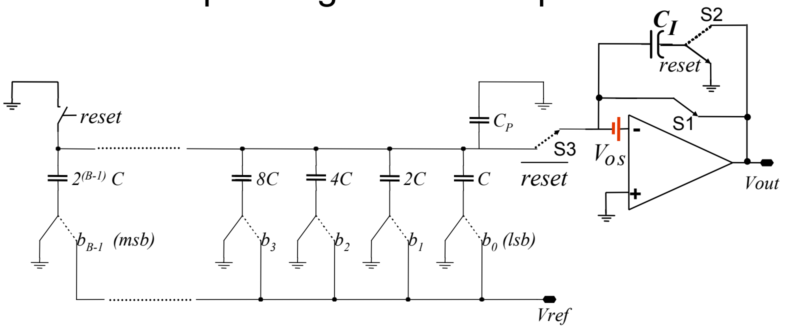
Parasitic Insensitive Charge Scaling DAC



$$V_{out} = \frac{\sum_{i=0}^{B-1} b_i 2^i C}{C_I} V_{ref} \ , \quad C_I = 2^B C \ \rightarrow V_{out} = \frac{\sum_{i=0}^{B-1} b_i 2^i}{2^B} V_{ref}$$

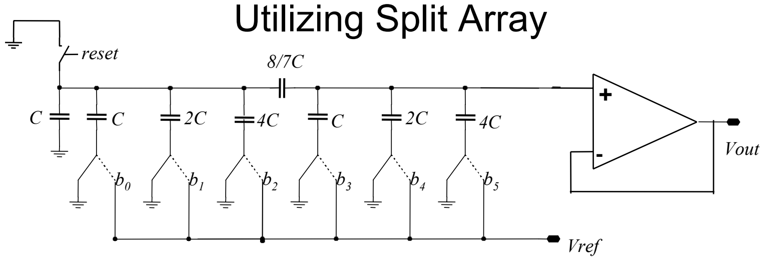
- Opamp helps eliminate the parasitic capacitor effect by producing virtual ground at the sensitive node since C_P has zero volts at start & end
  - Issue: opamp offset & speed

Charge Scaling DAC
Incorporating Offset Compensation



- During reset phase:
  - Opamp disconnected from capacitor array via switch S3
  - Opamp connected in unity-gain configuration (S1)
  - C_I Bottom plate connected to ground (S2)
  - $V_{out} \sim - V_{os}$ → $V_{CI} = -V_{os}$
- This effectively compensates for offset during normal phase

Charge Scaling DAC
Utilizing Split Array



$$C_{series} = \frac{\sum all\, LSB\, array\, C}{\sum all\, MSB\, array\, C}\, C$$

- Split array→ reduce the total area of the capacitors required for high resolution DACs
  - E.g. 10bit regular binary array requires 513 unit Cs while split array (5&5) needs 64 unit Cs
  - Issue: Sensitive to parasitic capacitor

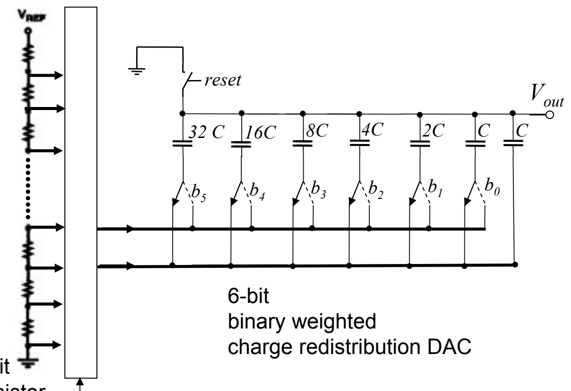
Charge Scaling DAC

- Advantages:
  - Low power dissipation → capacitor array does not dissipate DC power
  - Output is sample and held → no need for S/H
  - INL function of capacitor ratio
  - Possible to trim or calibrate for improved INL
  - Offset cancellation almost for free
- Disadvantages:
  - Process needs to include good capacitive material → not compatible with standard digital process
  - Requires large capacitor ratios
  - Not inherently monotonic (more later)

Segmented DAC

Resistor Ladder (MSB) & Binary Weighted Charge Scaling (LSB)

- Example: 12bit DAC
  - 6-bit MSB DAC→ R- string
  - 6-bit LSB DAC → binary weighted charge scaling
- Complexity much lower compared to full R-string
  - Full R string→ 4096 resistors
  - Segmented → 64 R + 7 Cs (64 unit caps)

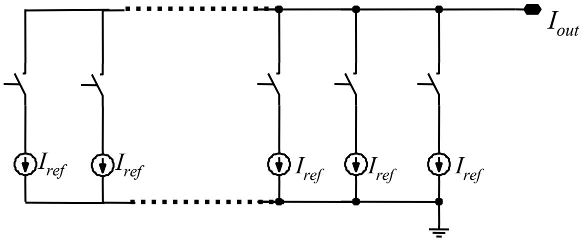


6bit resistor ladder

Switch Network

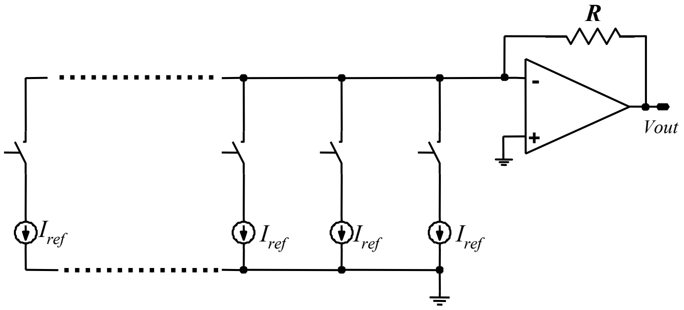
6-bit binary weighted charge redistribution DAC

Current Source DAC
Unit Element



- "Unit elements " or thermometer
- 2^B-1 current sources & switches
- Suited for both MOS and BJT technologies
- Monotonicity does not depend on element matching
- Output resistance of current source → gain error
  - Cascode type current sources higher output resistance → less gain error

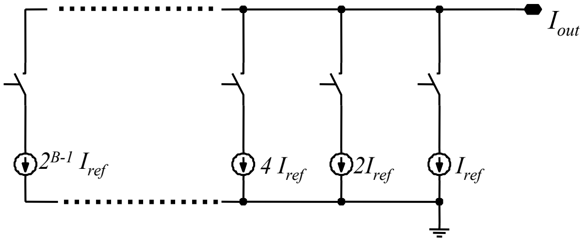
Current Source DAC
Unit Element



- Output resistance of current source → gain error problem

  → Use transresistance amplifier- output of current sources held @ virtual ground – error due to current source output resistance eliminated

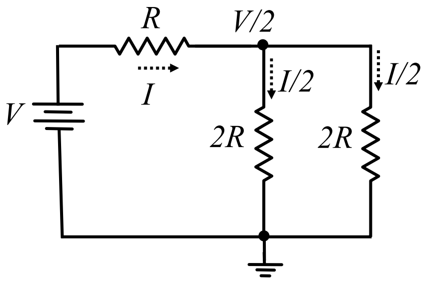
Current Source DAC
Binary Weighted



- "Binary weighted"
- B current sources & switches (2^B-1 unit elements)
- Monotonicity depends on element matching (more later)

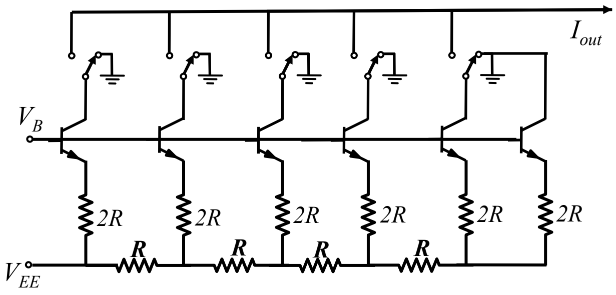
R-2R Ladder Type DAC

- 1-bit R-2R DAC
  - Simple R network divides both voltage & current by 2
    → 1-bit DAC



Increase # of bits by replicating circuit

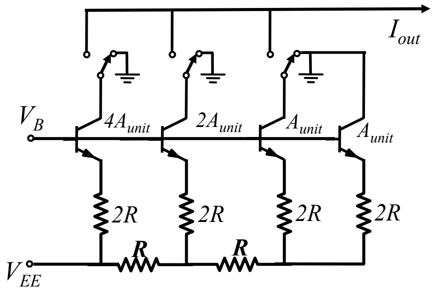
R-2R Ladder DAC



Emitter-follower added to convert to high-impedance current sources
→ Series switch resistance does not impair performance

R-2R Ladder DAC How Does it Work?

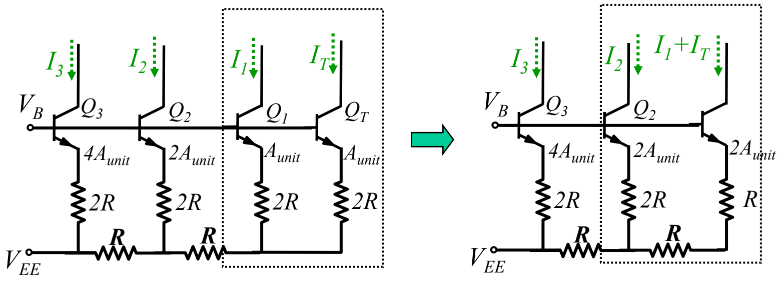
Consider a simple 3bit R-2R DAC:



R-2R Ladder DAC
How Does it Work?

Simple 3bit DAC:

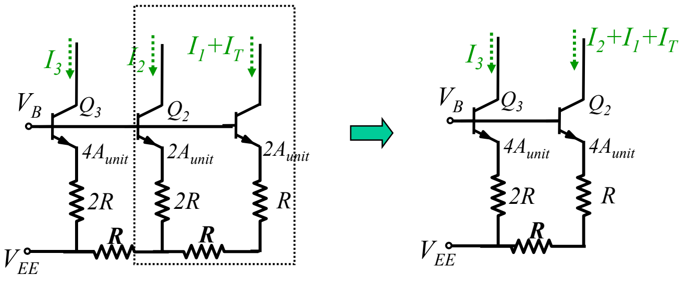
1- Consolidate first two stages:



R-2R Ladder DAC
How Does it Work?

Simple 3bit DAC-

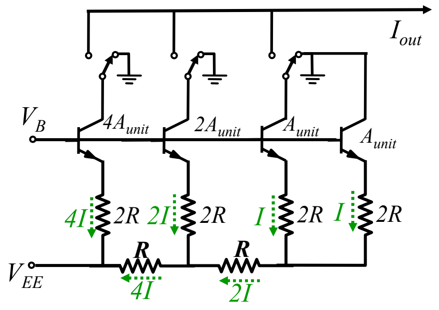
2- Consolidate next two stages:



$$I_3 = I_2 + I_1 + I_T \rightarrow I_3 = \frac{I_{Total}}{2}, I_2 = \frac{I_{Total}}{4}, I_1 = \frac{I_{Total}}{8}$$

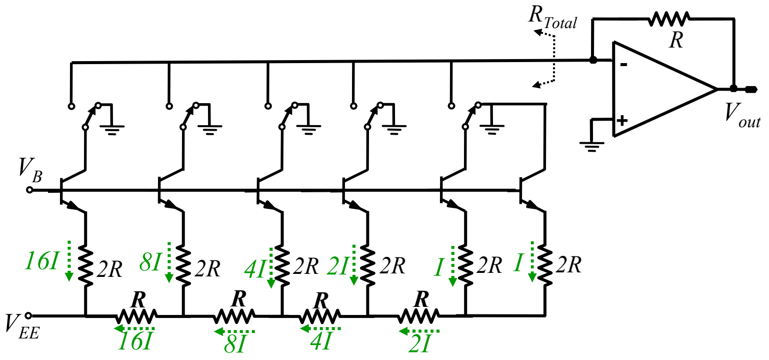
R-2R Ladder DAC
How Does it Work?

Consider a simple 3bit R-2R DAC:



Ref: B. Razavi, "*Data Conversion System Design",* IEEE Press, 1995, page 84-87

R-2R Ladder DAC



Transresistance amplifier added to:

- Convert current to voltage
- Generate virtual ground @ current summing node so that output impedance of current sources do not cause error
- Issue: error due to opamp offset

R-2R Ladder DAC
Opamp Offset Issue

$$V_{os}^{out} = V_{os}^{in}\left(1+\frac{R}{R_{Total}}\right)$$

$If\ R_{Total} = large,$

$\rightarrow V_{os}^{out} = V_{os}^{in}$

$If\ R_{Total} = not\ large$

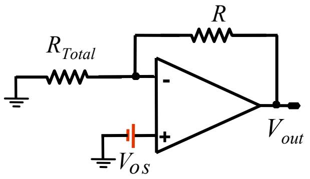
$\rightarrow V_{os}^{out} = V_{os}^{in}\left(1+\frac{R}{R_{Total}}\right)$

$Problem:$

$Since\ R_{Total}\ is\ code\ dependant$

$\rightarrow V_{os}^{out}\ would\ be\ code\ dependant$

$\rightarrow High\ INL$

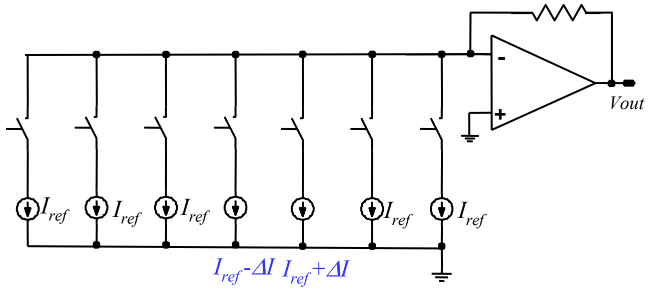


Offset Model

R-2R Ladder
Structure Shown in Page 50

- Advantages:
  - Resistor ratios only x2
- Disadvantages:
  - Total device emitter area → $A_E x 2^B$
    → Not practical for high resolution DACs
  - INL/DNL error due to amplifier offset

Current Source DAC
DNL/INL Due to Element Mismatch



- Simple unit-element example:
  - 3-bit DAC
  - Assume only two of the current sources mismatched (# 4 & #5)

Current Source DAC
DNL/INL Due to Element Mismatch

$$DNL[m]=\frac{segment[m]-V[LSB]}{V[LSB]}$$

$$DNL[4]=\frac{segment[4]-V[LSB]}{V[LSB]}$$

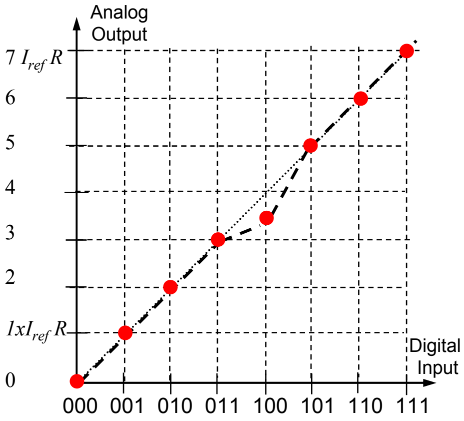
$$=\frac{(I-\Delta I)R-IR}{IR}$$

$$\boxed{DNL[4]=-\Delta I/I\,[LSB]}$$

$$DNL[5]=\frac{(I+\Delta I)R-IR}{IR}$$

$$\boxed{DNL[5]=\Delta I/I[LSB]}$$

$$\boxed{\rightarrow INL_{max}=-\Delta I/I\,[LSB]}$$



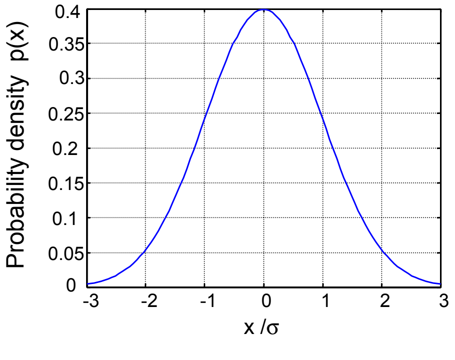
Static DAC Errors -INL / DNL

Static DAC errors mainly due to component mismatch

- Systematic errors
  - Contact resistance
  - Edge effects in capacitor arrays
  - Process gradients
  - Finite current source output resistance
- Random errors
  - Lithography etc…
  - Often Gaussian distribution (central limit theorem)

*Ref: C. Conroy et al, “Statistical Design Techniques for D/A Converters,” JSSC Aug. 1989, pp. 1118-28.

Gaussian Distribution



$$p(x)=\frac{1}{\sqrt{2\pi}\sigma}e^{-\frac{(x-\mu)^2}{2\sigma^2}}$$

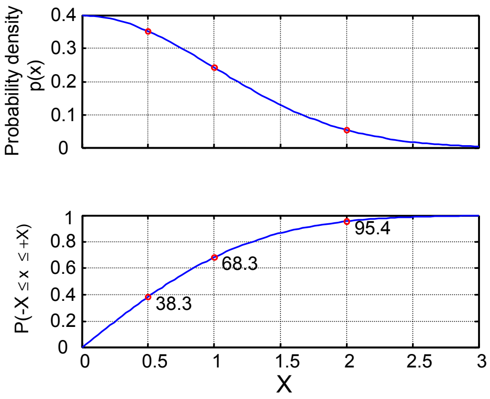
$$where\ standard\ deviation:\sigma=\sqrt{E(X^2)-\mu^2}$$

Yield

$$P\left(-X \le x \le +X\right) =$$

$$= \frac{1}{\sqrt{2\pi}} \int_{-X}^{+X} e^{-\frac{x^2}{2}} dx$$

$$= erf\left(\frac{X}{\sqrt{2}}\right)$$



Yield

X/σ	P(-X ≤ x ≤ X) [%]	X/σ	P(-X ≤ x ≤ X) [%]
0.2000	15.8519	2.2000	97.2193
0.4000	31.0843	2.4000	98.3605
0.6000	45.1494	2.6000	99.0678
0.8000	57.6289	2.8000	99.4890
1.0000	68.2689	3.0000	99.7300
1.2000	76.9861	3.2000	99.8626
1.4000	83.8487	3.4000	99.9326
1.6000	89.0401	3.6000	99.9682
1.8000	92.8139	3.8000	99.9855
2.0000	95.4500	4.0000	99.9937

Example

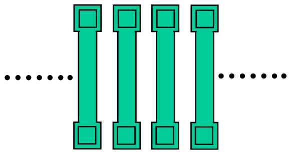
- Measurements show that the offset voltage of a batch of operational amplifiers follows a Gaussian distribution with σ = 2mV and μ = 0.

- Fraction of opamps with $|V_{os}|$ < 6mV:
  - $X/\sigma = 3$ → 99.73 % yield (we'd still test before shipping!)

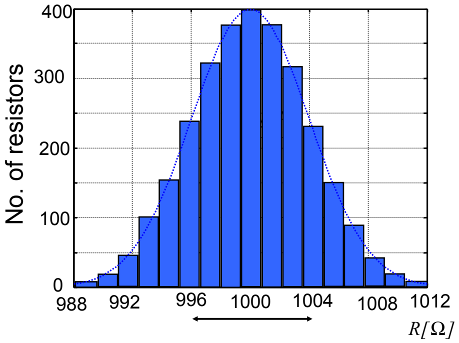
- Fraction of opamps with $|V_{os}|$ < 400μV:
  - $X/\sigma = 0.2$ → 15.85 % yield

Component Mismatch

Example: Resistors layouted out side-by-side



After fabrication large # of devices measured & graphed → typically if sample size large shape is Gaussian

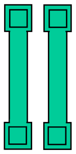


E.g. Let us assume in this example 1000 Rs measured & 68.5% within +-4OHM or +-0.4% of average

→ 1σ for resistors→ 0.4%

Component Mismatch

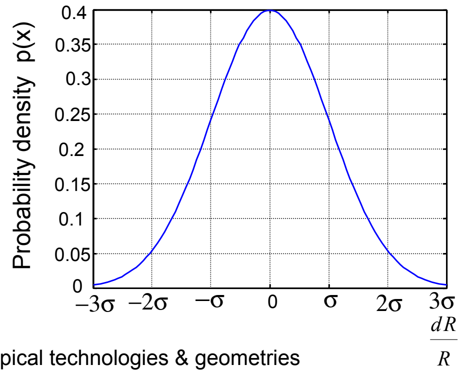
Example: Two resistors layouted out side-by-side



$$R = \frac{R_1 + R_2}{2}$$

$$dR = R_1 - R_2$$

$$\sigma^2_{\frac{dR}{R}} \propto \frac{1}{Area}$$



For typical technologies & geometries

1σ for resistors → 0.02 to 5%

In the case of resistors σ is a function of area

DNL Unit Element DAC

E.g. Resistor string DAC:

$$\Delta = R_{median}\, I_{ref} \quad where \quad R_{median} = \frac{\sum_{o}^{2^B-1} R_i}{2^B}$$

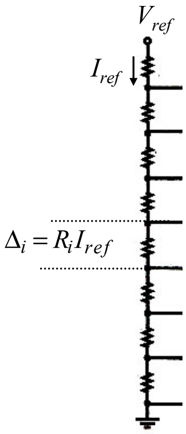
$$\Delta_i = R_i I_{ref}$$

$$DNL_i = \frac{\Delta_{median} - \Delta_i}{\Delta_{median}}$$

$$= \frac{R_i - R_{median}}{R_{median}} = \frac{dR}{R_{median}} \approx \frac{dR}{R_i}$$

$$\sigma_{DNL} = \sigma_{\frac{dR_i}{R_i}}$$

DNL of unit element DAC is independent of resolution!



DNL Unit Element DAC

E.g. Resistor string DAC:

$$\boxed{\sigma_{DNL} = \sigma_{\frac{dR_i}{R_i}}}$$

Example:

If $\sigma_{dR/R}$ = 0.4%, what DNL spec goes into the datasheet so that 99.9% of all converters meet the spec?

To first order → DNL of unit element DAC is independent of resolution!
Note similar results for other unit-element based DACs

Yield

X/σ	P(-X ≤ x ≤ X) [%]	X/σ	P(-X ≤ x ≤ X) [%]
0.2000	15.8519	2.2000	97.2193
0.4000	31.0843	2.4000	98.3605
0.6000	45.1494	2.6000	99.0678
0.8000	57.6289	2.8000	99.4890
1.0000	68.2689	3.0000	99.7300
1.2000	76.9861	3.2000	99.8626
1.4000	83.8487	3.4000	99.9326
1.6000	89.0401	3.6000	99.9682
1.8000	92.8139	3.8000	99.9855
2.0000	95.4500	4.0000	99.9937

DNL Unit Element DAC

E.g. Resistor string DAC:

$$\boxed{\sigma_{DNL} = \sigma_{\frac{dR_i}{R_i}}}$$

Example:

If $\sigma_{dR/R}$ = 0.4%, what DNL spec goes into the datasheet so that 99.9% of all converters meet the spec?

Answer:

From table: for 99.9%

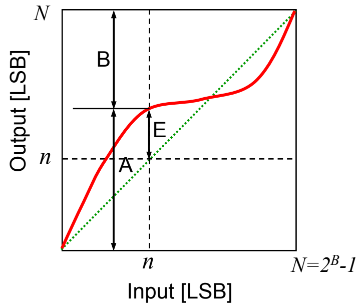
→ X/σ = 3.3

$\sigma_{DNL} = \sigma_{dR/R}$ = 0.4%

3.3 σ_{DNL} = 1.3%

$\boxed{\rightarrow \text{DNL= +/- 0.013 LSB}}$

DAC INL Analysis



	Ideal	Variance
$A=n-E$	n	$n.\sigma_\varepsilon^2$
$B=N-n+E$	$N-n$	$(N-n).\sigma_\varepsilon^2$

$$E = A-n \qquad r = n/N \qquad N=A+B$$

$$= A-r(A+B)$$

$$= A\,(1-r) - B.r$$

→ *Variance of E:*

$$\sigma_E^2 = (1-r)^2 .\sigma_A^2 + r^2 .\sigma_B^2$$

$$= N.r\,.(1-r).\sigma_\varepsilon^2$$

DAC INL

$$\sigma_E^{\,2} = n\left(1-\frac{n}{N}\right)\times\sigma_\varepsilon^{\,2}$$

$$\text{To find max. variance:} \quad \frac{d\sigma_E^{\,2}}{dn} = 0$$

$$\rightarrow n = N/2$$

- Error is maximum at mid-scale (N/2):

$$\boxed{\begin{aligned}\sigma_{INL} &= \frac{1}{2}\sqrt{2^B-1}\;\sigma_\varepsilon \\ &\text{with}\quad N = 2^B-1\end{aligned}}$$

- INL depends on DAC resolution and element matching σ_ε
- While $\sigma_{DNL} = \sigma_\varepsilon$ is to first order independent of DAC resolution and is only a function of element matching

Ref: Kuboki et al, TCAS, 6/1982

Untrimmed DAC INL

$$\sigma_{INL} \cong \frac{1}{2}\sqrt{2^B-1}\;\sigma_\varepsilon$$

$$B \cong 2 + 2\log_2\left[\frac{\sigma_{INL}}{\sigma_\varepsilon}\right]$$

<u>Example:</u>

Assume the following requirement for a DAC:

σ_{INL} = *0.1 LSB*

Then:

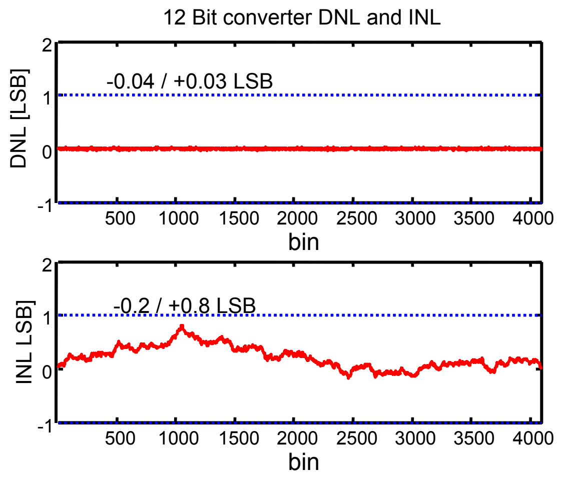
σ_ε = *1%* → *B = 8.6*

σ_ε = *0.5%* → *B = 10.6*

σ_ε = *0.2%* → *B = 13.3*

σ_ε = *0.1%* → *B = 15.3*

Simulation Example

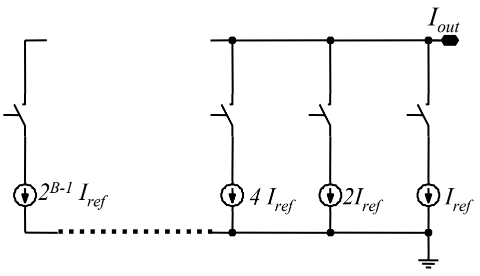


σ_ε = 1%
B = 12
Random # generator used in MatLab

Computed INL:
σ_{INL} = 0.3 LSB (midscale)

INL for Binary Weighted DAC

- INL same as for unit element DAC
- DNL depends on transition
  - Example:
    0 to 1 → $\sigma_{DNL}^2 = \sigma_{(dI/I)}^{\ 2}$
    1 to 2 → $\sigma_{DNL}^2 = 3\sigma_{(dI/I)}^{\ 2}$
- Consider MSB transition: 0111 … → 1000 …

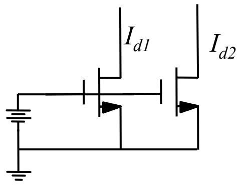


MOS Device Matching Effects

$$I_d = \frac{I_{d1}+I_{d2}}{2}$$

$$\frac{dI_d}{I_d} = \frac{I_{d1}-I_{d2}}{I_d}$$

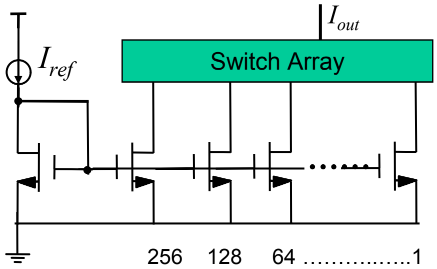
$$\frac{dI_d}{I_d} = \frac{d\,{}^{W}\!/_{L}}{{}^{W}\!/_{L}} + \frac{dV_{th}}{V_{GS}-V_{th}}$$



- Current matching depends on:
  - Device *W/L* ratio matching
    → Larger device area less mismatch effect
  - Threshold voltage matching
    → Larger gate-overdrive less threshold voltage mismatch effect

Current-Switched DACs in CMOS

$$\frac{dI_d}{I_d} = \frac{d\,{}^{W}\!/_{L}}{{}^{W}\!/_{L}} + \frac{dV_{th}}{V_{GS}-V_{th}}$$

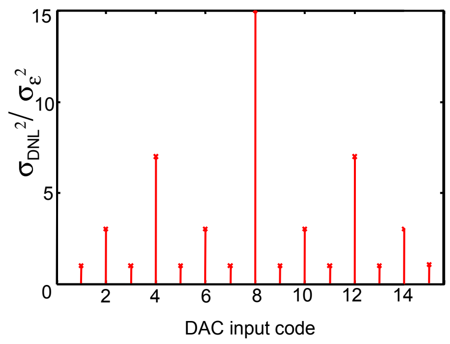


Example: 8bit Binary Weighted

•Advantages:
Can be very fast
Small area for < 9-10bits

•Disadvantages:
Accuracy depends on device *W/L* & V_{th} matching

Binary Weighted DAC DNL



- Worst-case transition occurs at mid-scale:

$$\sigma_{DNL}^2 = \underbrace{\left(2^{B-1}-1\right)\sigma_\varepsilon^2}_{0111\ldots} + \underbrace{\left(2^{B-1}\right)\sigma_\varepsilon^2}_{1000\ldots}$$

$$\cong 2^B \sigma_\varepsilon^2$$

$$\sigma_{DNL_{max}} = 2^{B/2}\sigma_\varepsilon$$

$$\sigma_{INLmax} \cong \frac{1}{2}\sqrt{2^B-1}\ \sigma_\varepsilon \cong \frac{1}{2}\sigma_{DNL_{max}}$$

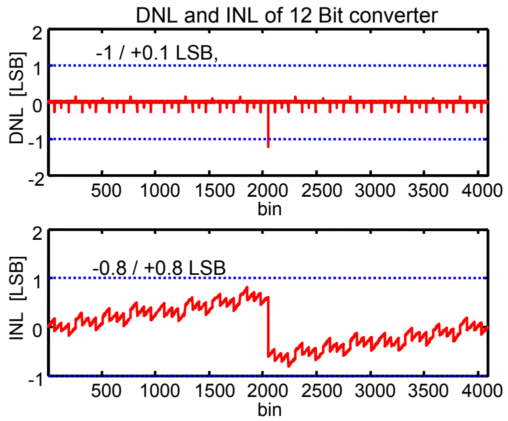
- Example:

B = 12, σ_ε = 1%

→ σ_{DNL} = 0.64 LSB

→ σ_{INL} = 0.32 LSB

“Another” Random Run …



Now (by chance) worst DNL is mid-scale.

Statistical result!

Unit Element versus Binary Weighted DAC

Unit Element DAC	Binary Weighted DAC
$\sigma_{DNL} = \sigma_{\varepsilon}$	$\sigma_{DNL} \cong 2^{B/2}\,\sigma_{\varepsilon} = 2\sigma_{INL}$
$\sigma_{INL} \cong 2^{B/2\,-1}\,\sigma_{\varepsilon}$	$\sigma_{INL} \cong 2^{B/2\,-1}\,\sigma_{\varepsilon}$

Number of switched elements:

$S = 2^{B}$	$S = B$

Key point: Significant difference in performance and complexity!

Unit Element versus Binary Weighted DAC Example: B=10

Unit Element DAC	Binary Weighted DAC
$\sigma_{DNL} = \sigma_{\varepsilon}$	$\sigma_{DNL} \cong 2^{B/2}\sigma_{\varepsilon} = 32\sigma_{\varepsilon}$
$\sigma_{INL} \cong 2^{B/2-1}\sigma_{\varepsilon} = 16\sigma_{\varepsilon}$	$\sigma_{INL} \cong 2^{B/2-1}\sigma_{\varepsilon} = 16\sigma_{\varepsilon}$

Number of switched elements:

$S = 2^{B} = 1024$	$S = B = 10$

Significant difference in performance and complexity!

DAC INL/DNL Summary

- DAC choice of architecture has significant impact on DNL
- INL is independent of DAC architecture and requires element matching commensurate with overall DAC precision
- Results are for uncorrelated random element variations
- Systematic errors and correlations are usually also important

Ref: Kuboki, S.; Kato, K.; Miyakawa, N.; Matsubara, K. Nonlinearity analysis of resistor string A/D converters. IEEE Transactions on Circuits and Systems, vol.CAS-29, (no.6), June 1982. p.383-9.