

EE247

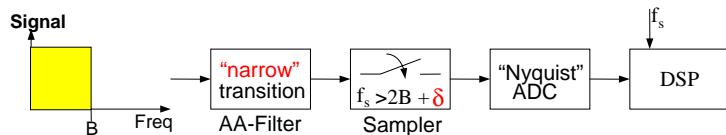
Lecture 24

Oversampled ADCs

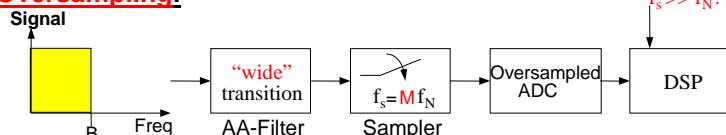
- Why oversampling?
- Pulse-count modulation
- Sigma-delta modulation
 - 1-Bit quantization
 - Quantization error (noise) spectrum
 - SQNR analysis
 - Limit cycle oscillations
- 2nd order $\Sigma\Delta$ modulator
 - Dynamic range
 - Practical implementation
 - Effect of various nonidealities on the $\Sigma\Delta$ performance

The Case for Oversampling

Nyquist sampling:

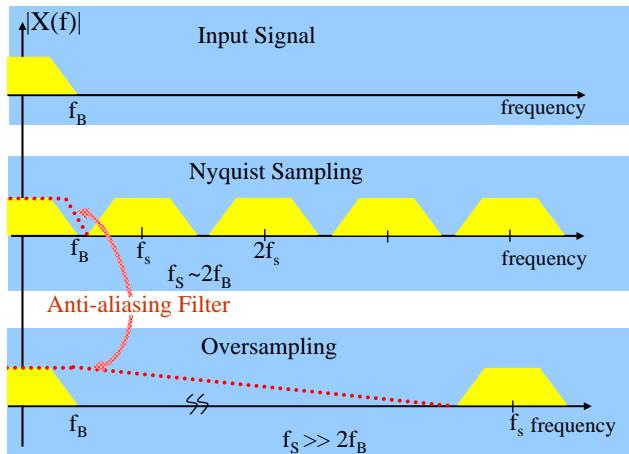


Oversampling:



- Nyquist rate $f_N = 2B$
- Oversampling rate $M = f_s/f_N \gg 1$

Nyquist v.s. Oversampled Converters Antialiasing

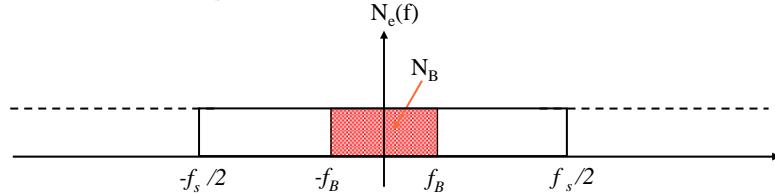


Oversampling Benefits

- No stringent requirements imposed on analog building blocks
- Takes advantage of the availability of low cost, low power digital filtering
- Relaxed transition band requirements for analog anti-aliasing filters
- Reduced baseband quantization noise power
- Allows trading speed for resolution

ADC Converters Baseband Noise

- For a quantizer with step size Δ and sampling rate f_s :
 - Quantization noise power distributed uniformly across Nyquist bandwidth ($f_s/2$)



- Power spectral density:

$$N_e(f) = \frac{\overline{e^2}}{f_s} = \left(\frac{\Delta^2}{12} \right) \frac{I}{f_s}$$

- Noise is aliased into the Nyquist band $-f_s/2$ to $f_s/2$

Oversampled Converters Baseband Noise

$$S_B = \int_{-f_B}^{f_B} N_e(f) df = \int_{-f_B}^{f_B} \left(\frac{\Delta^2}{12} \right) \frac{I}{f_s} df$$

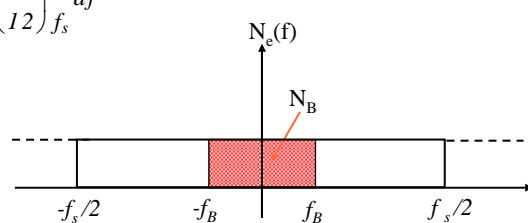
$$= \frac{\Delta^2}{12} \left(\frac{2f_B}{f_s} \right)$$

where for $f_B = f_s/2$

$$S_{B0} = \frac{\Delta^2}{12}$$

$$S_B = S_{B0} \left(\frac{2f_B}{f_s} \right) = \frac{S_{B0}}{M}$$

where $M = \frac{f_s}{2f_B}$ = oversampling ratio



Oversampled Converters Baseband Noise

$$S_B = S_{B0} \left(\frac{2f_B}{f_s} \right) = \frac{S_{B0}}{M}$$

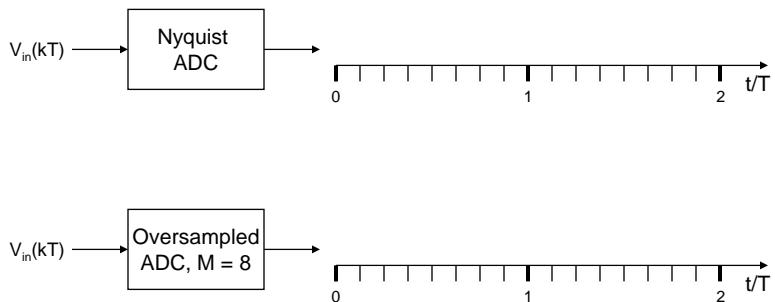
where $M = \frac{f_s}{2f_B}$ = oversampling ratio

2X increase in M
→ 3dB reduction in S_B
→ ½ bit increase in resolution/octave oversampling

To increase the improvement in resolution:

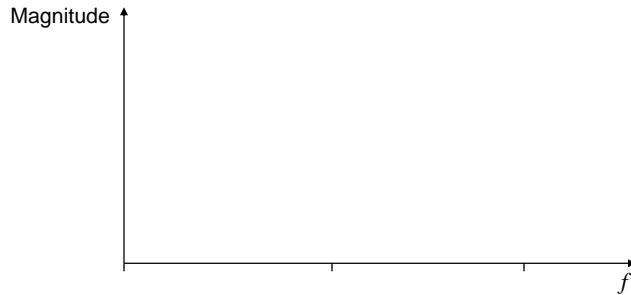
- Embed quantizer in a feedback loop
 - Predictive (delta modulation)
 - Noise shaping (sigma delta modulation)

Pulse-Count Modulation



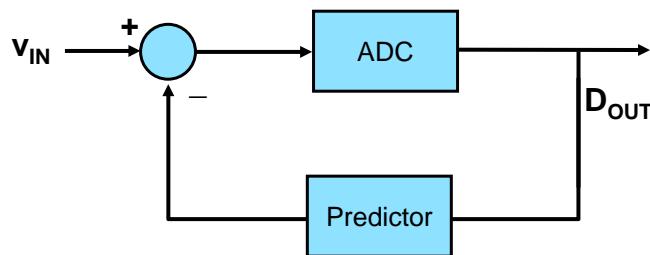
Mean of pulse-count signal approximates analog input!

Pulse-Count Spectrum



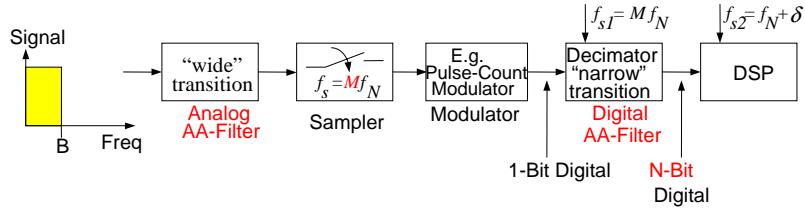
- Signal: low frequencies, $f < B \ll f_s$
- Quantization error: high frequency, $B \dots f_s / 2$
- Separate with low-pass filter!

Oversampled ADC Predictive Coding



- Quantize the difference signal rather than the signal itself
- Smaller input to ADC → Buy dynamic range
- Only works if combined with oversampling
- 1-Bit digital output
- Digital filter computes “average” → N-Bit output

Oversampled ADC



Decimator:

- Digital (low-pass) filter
- Removes quantization error for $f > B$
- Provides most anti-alias filtering
- Narrow transition band, high-order
- 1-Bit input, N-Bit output (essentially computes "average")

Modulator

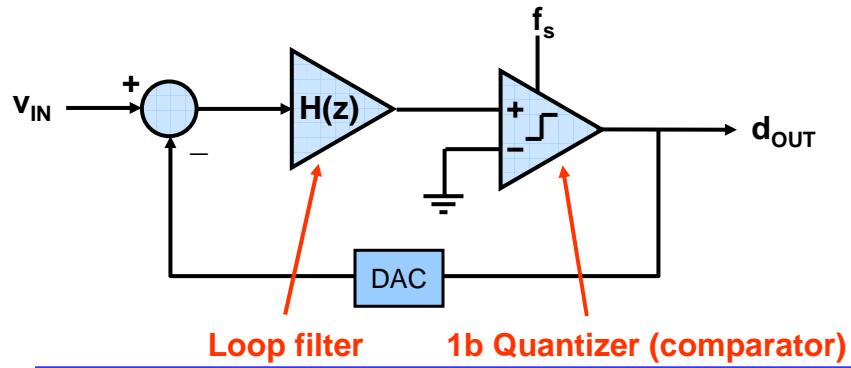
• Objectives:

- Convert analog input to 1-Bit pulse density stream
- Move quantization error to high frequencies $f >> B$
- Operates at high frequency $f_s >> f_N$
 - $M = 8 \dots 256$ (typical) 1024
 - Since modulator operated at high frequencies \rightarrow need to keep circuitry "simple"

$\rightarrow \Sigma\Delta = \Delta\Sigma$ Modulator

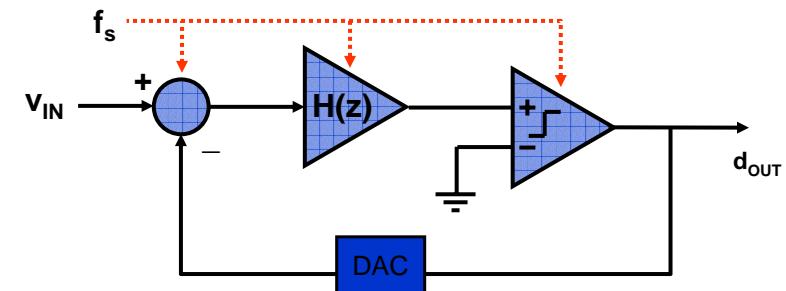
Sigma-Delta Modulators

Analog 1-Bit $\Sigma\Delta$ modulators convert a continuous time analog input v_{IN} into a 1-Bit sequence d_{OUT}

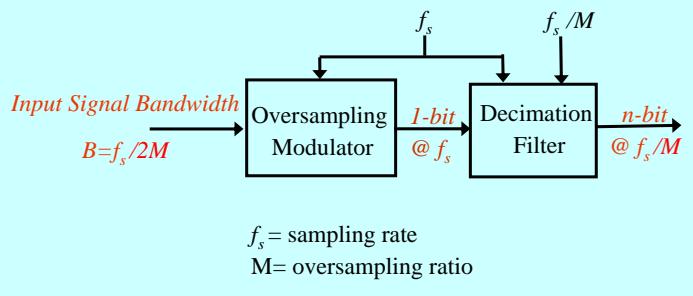


Sigma-Delta Modulators

- The loop filter H can be either switched-capacitor or continuous time
- Switched-capacitor filters are “easier” to implement + frequency characteristics scale with clock rate
- Continuous time filters provide anti-aliasing protection
- Loop filter can also be realized with passive LC’s at very high frequencies



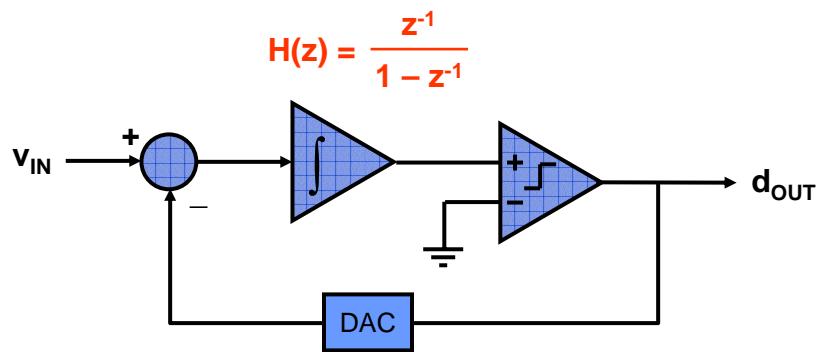
Oversampling A/D Conversion



- Analog front-end → oversampled noise-shaping modulator
 - Converts original signal to a 1-bit digital output at the high rate of $(2MXB)$
- Digital back-end → digital filter
 - Removes out-of-band quantization noise
 - Provides anti-aliasing to allow re-sampling @ lower sampling rate

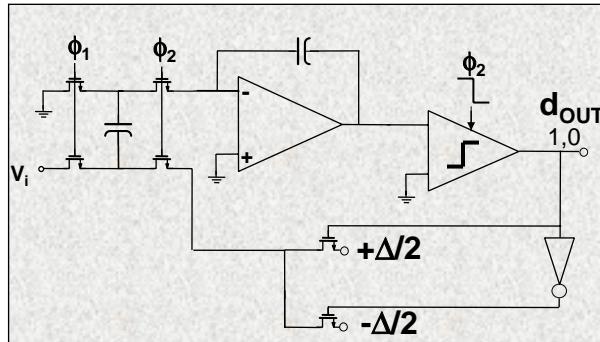
1st Order $\Sigma\Delta$ Modulator

In a 1st order modulator, simplest loop filter → an integrator

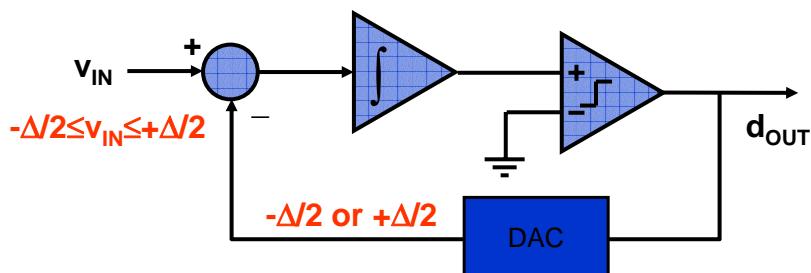


1st Order $\Sigma\Delta$ Modulator

Switched-capacitor implementation

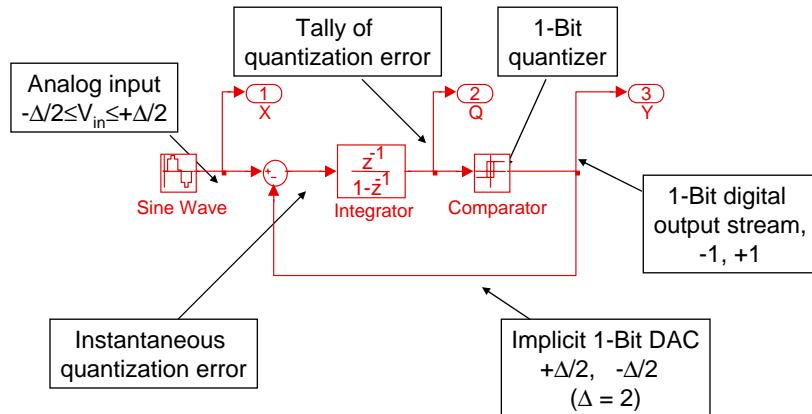


1st Order $\Delta\Sigma$ Modulator



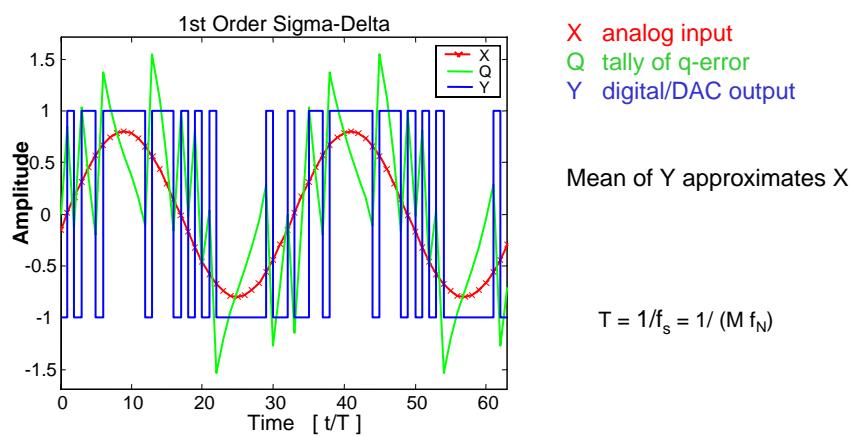
- Properties of the first-order modulator:
 - Analog input range is equal to the DAC reference
 - The average value of d_{OUT} must equal the average value of v_{IN}
 - +1's (or -1's) density in d_{OUT} is an inherently monotonic function of v_{IN}
→ linearity is not dependent on component matching
 - Alternative multi-bit DAC (and ADCs) solutions reduce the quantization error but loose this inherent monotonicity & relaxed matching requirements

1st Order $\Sigma\Delta$ Modulator



- M chosen to be 8 (low) to ease observability

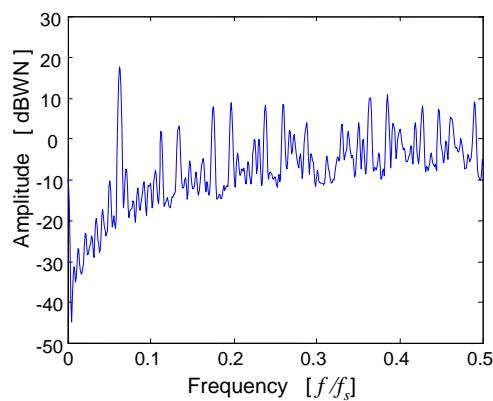
1st Order Modulator Signals



$\Sigma\Delta$ Modulator Characteristics

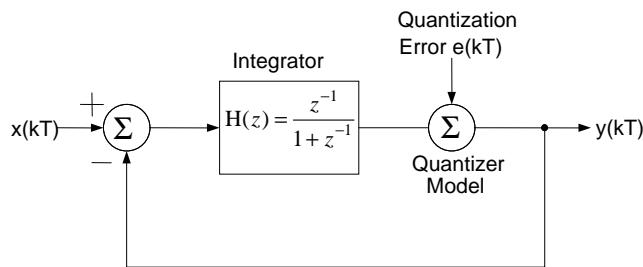
- Quantization noise and thermal noise (KT/C) distributed over $-f_s/2$ to $+f_s/2$
→ Total noise within signal bandwidth reduced by $1/M$
- Very high SQNR achievable (> 20 Bits!)
- Inherently linear for 1-Bit DAC
- To first order, quantization error independent of component matching
- Limited to moderate & low speed

Output Spectrum



- Definitely not white!
- Skewed towards higher frequencies
- Notice the distinct tones
- dBWN (dB White Noise) scale sets the 0dB line at the noise per bin of a random -1, +1 sequence

Quantization Noise Analysis

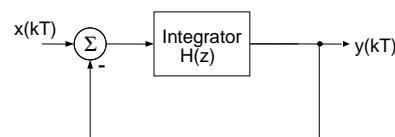


- Sigma-Delta modulators are nonlinear systems with memory → difficult to analyze directly
- Representing the quantizer as an additive noise source linearizes the system

Signal Transfer Function

$$H(z) = \frac{z^{-1}}{1 + z^{-1}}$$

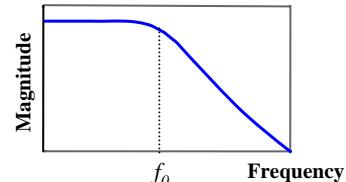
$$H(j\omega) = \frac{\omega_0}{j\omega}$$



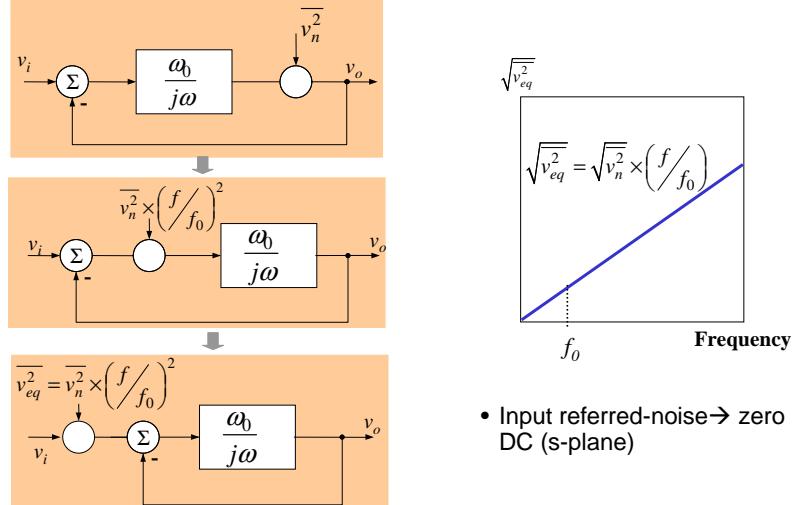
Signal transfer function
→ low pass function:

$$H_{Sig}(j\omega) = \frac{1}{1 + s/\omega_0}$$

$$H_{Sig}(z) = \frac{Y(z)}{X(z)} = \frac{H(z)}{1 + H(z)} = z^{-1} \Rightarrow \text{Delay}$$



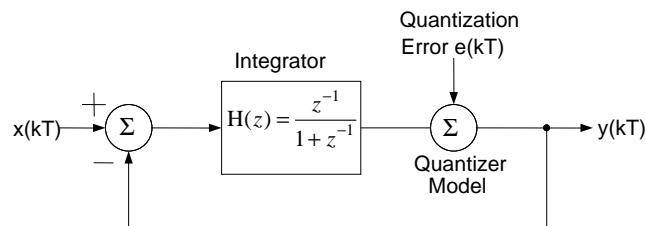
Noise Transfer Function Qualitative Analysis



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STF and NTF



Signal transfer function:

$$\text{STF} = \frac{Y(z)}{X(z)} = \frac{H(z)}{1 + H(z)} = z^{-1} \Rightarrow \text{Delay}$$

Noise transfer function:

$$\text{NTF} = \frac{Y(z)}{E(z)} = \frac{1}{1 + H(z)} = 1 - z^{-1} \Rightarrow \text{Differentiator}$$

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Noise Transfer Function

$$NTF = \frac{Y(z)}{E(z)} = \frac{1}{1 + H(z)} = 1 - z^{-1}$$

$$NTF(j\omega) = (1 - e^{-j\omega T}) = 2e^{-j\omega T/2} \left(\frac{e^{j\omega T/2} - e^{-j\omega T/2}}{2} \right)$$

$$= 2e^{-j\omega T/2} j \sin(\omega T/2)$$

$$= 2e^{-j\omega T/2} \times e^{-j\pi/2} [\sin(\omega T/2)]$$

$$= [2 \sin(\omega T/2)] e^{-j(\omega T - \pi)/2}$$

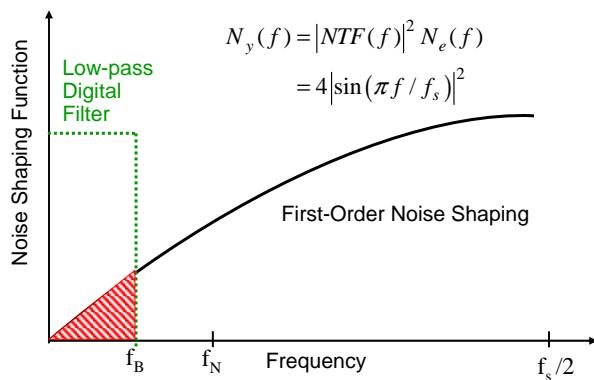
where $T = 1/f_s$

Thus:

$$|NTF(f)| = 2 |\sin(\omega T/2)| = 2 |\sin(\pi f / f_s)|$$

$$N_y(f) = |NTF(f)|^2 N_e(f)$$

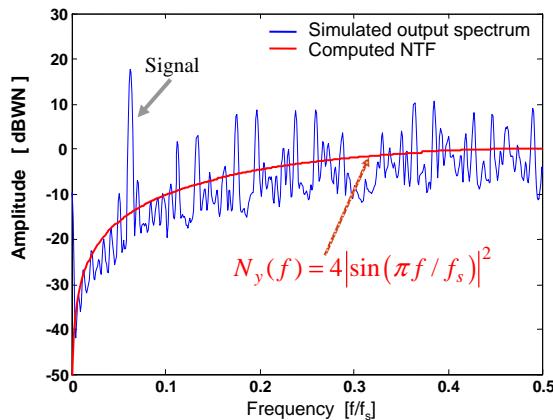
First Order $\Sigma\Delta$ Modulator Noise Transfer Characteristics



Key Point:

Most of quantization noise pushed out of frequency band of interest

First Order $\Sigma\Delta$ Modulator Simulated Noise Transfer Characteristic



Quantizer Error

- For quantizers with many bits

$$\overline{e^2(kT)} = \frac{\Delta^2}{12}$$

- Let's use the same expression for the 1-Bit case
- **Use simulation to verify validity**
- Experience: Often sufficiently accurate to be useful, with enough exceptions to be very careful

First Order $\Sigma\Delta$ Modulator In-Band Quantization Noise

$$\begin{aligned}
 NTF(z) &= 1 - z^{-1} \\
 |NTF(f)|^2 &= 4 |\sin(\pi f / f_s)|^2 \quad \text{for } M \gg 1 \\
 \overline{S_Y} &= \int_{-B}^B S_Q(f) |NTF(z)|_{z=e^{j2\pi fT}}^2 df \\
 &\approx \int_{-\frac{f_s}{2M}}^{\frac{f_s}{2M}} \frac{1}{f_s} \frac{\Delta^2}{12} (2\sin\pi fT)^2 df
 \end{aligned}$$

$$\rightarrow \overline{S_Y} \approx \frac{\pi^2}{3} \frac{1}{M^3} \frac{\Delta^2}{12}$$

Dynamic Range

$$\begin{aligned}
 DR &= 10 \log \left[\frac{\text{peak signal power}}{\text{peak noise power}} \right] = 10 \log \left[\frac{\overline{S_X}}{\overline{S_Y}} \right] \\
 \overline{S_X} &= \frac{1}{2} \left(\frac{\Delta}{2} \right)^2 \quad \text{sinusoidal input, STF = 1} \\
 \overline{S_Y} &= \frac{\pi^2}{3} \frac{1}{M^3} \frac{\Delta^2}{12} \\
 \frac{\overline{S_X}}{\overline{S_Y}} &= \frac{9}{2\pi^2} M^3
 \end{aligned}$$

M	DR
16	33 dB
32	42 dB
1024	87 dB

$$DR = 10 \log \left[\frac{9}{2\pi^2} M^3 \right] = 10 \log \left[\frac{9}{2\pi^2} \right] + 30 \log M$$

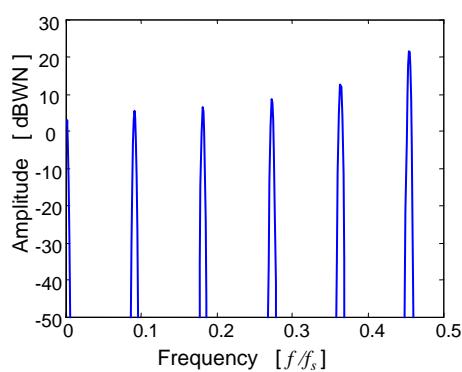
$$DR = -3.4dB + 30 \log M$$

2X increase in M \rightarrow 9dB (1.5-Bit) increase in dynamic range

Oversampling and Noise Shaping

- $\Sigma\Delta$ modulators have interesting characteristics
 - Unity gain for input signal V_{IN}
 - Large in-band attenuation of quantization noise injected at quantizer input
 - Performance significantly better than 1-Bit noise performance possible for frequencies $\ll f_s$
- Increase in oversampling ($M = f_s/f_N \gg 1$) improves SQNR considerably
 - 1st order $\Sigma\Delta$: DR increases 9dB for each doubling of M
 - To first order, SQNR independent of circuit complexity and accuracy
- Analysis assumes that the quantizer noise is “white”
 - Not true in practice, especially for low-order modulators
 - Practical modulators suffer from other noise sources also (e.g. thermal noise)

DC Input

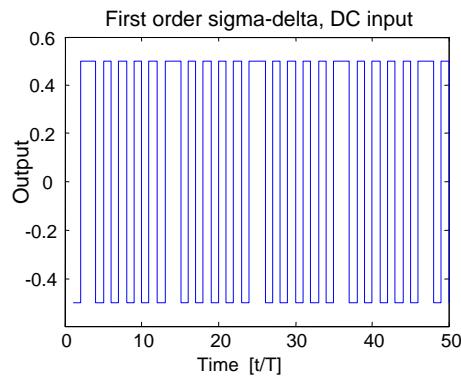


- DC input $A = 1/11$
- Doesn't look like spectrum of DC at all
- Tones frequency shaped the same as quantization noise
 - More prominent at higher frequencies
- Seems like periodic quantization “noise”

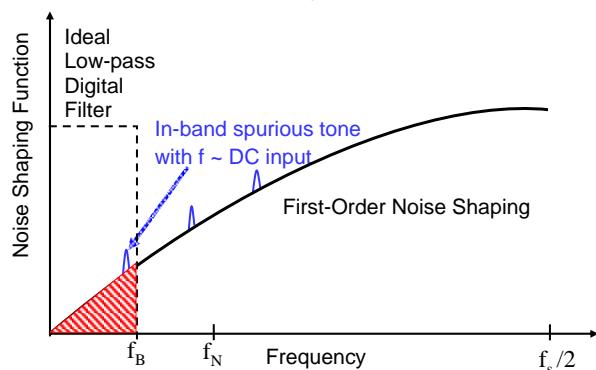
Limit Cycle

DC input 1/11 →
Periodic sequence:

1	+1
2	+1
3	-1
4	+1
5	-1
6	+1
7	-1
8	+1
9	-1
10	+1
11	-1

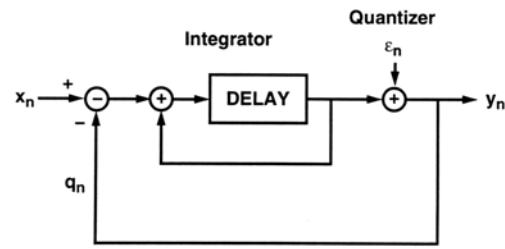


Limit Cycle



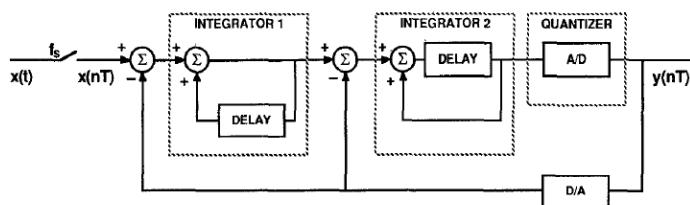
- Problem: quantization noise is periodic
- Solution:
 - Use dithering: randomizes quantization noise
 - Thermal noise → acts as dither
 - Second order loop

1st Order ΣΔ Modulator



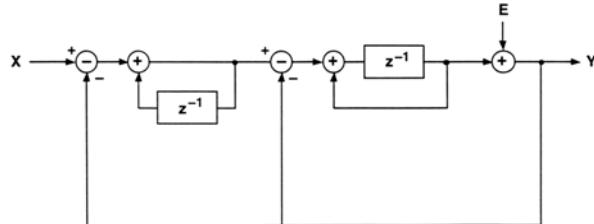
$$Y(z) = z^{-1}X(z) + (1 - z^{-1})E(z)$$

2nd Order ΣΔ Modulator



- Two integrators
- 1st integrator non-delaying
- Feedback from output to both integrators
- Tones less prominent compared to 1st order

2nd Order ΣΔ Modulator



Recursive derivation:

$$Y_n = X_{n-1} + (E_n - 2E_{n-1} + E_{n-2})$$

$$\text{Using the delay operator } z^{-1}: \quad Y(z) = z^{-1}X(z) + (1 - z^{-1})^2 E(z)$$

2nd Order ΣΔ Modulator In-Band Quantization Noise

$$H(z) = \frac{z^{-1}}{1 - z^{-1}}$$

$$G = 1$$

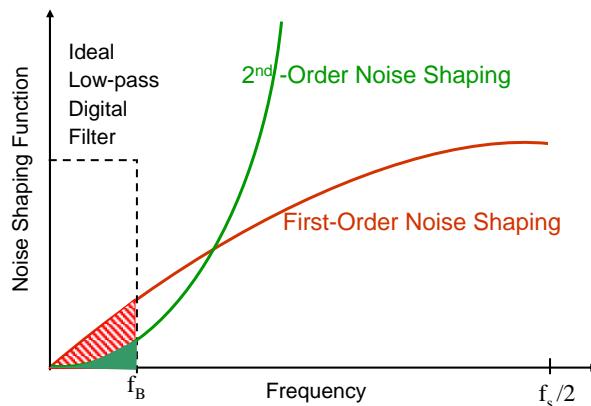
$$NTF(z) = (1 - z^{-1})^2$$

$$|NTF(f)|^2 =$$

$$= 2^4 |\sin(\pi f / f_s)|^4 \quad \text{for } M \gg 1$$

$$\begin{aligned} \overline{S_Y} &= \int_{-B}^B S_Q(f) |NTF(z)|^2_{z=e^{j2\pi fT}} df \\ &\approx \int_{-f_s/2M}^{f_s/2M} \frac{1}{f_s} \frac{\Delta^2}{12} (2\sin\pi fT)^4 df \\ &\approx \frac{\pi^4}{5} \frac{1}{M^5} \frac{\Delta^2}{12} \end{aligned}$$

Quantization Noise 2nd Order ΣΔ Modulator



2nd Order ΣΔ Modulator Dynamic Range

$$DR = 10 \log \left[\frac{\text{peak signal power}}{\text{peak noise power}} \right] = 10 \log \left[\frac{\overline{S_X}}{\overline{S_Y}} \right]$$

$$\overline{S_X} = \frac{1}{2} \left(\frac{\Delta}{2} \right)^2 \quad \text{sinusoidal input, STF} = 1$$

$$\overline{S_Y} = \frac{\pi^4}{5} \frac{1}{M^5} \frac{\Delta^2}{12}$$

$$\frac{\overline{S_X}}{\overline{S_Y}} = \frac{15}{2\pi^4} M^5$$

$$DR = 10 \log \left[\frac{15}{2\pi^4} M^5 \right] = 10 \log \left[\frac{15}{2\pi^4} \right] + 50 \log M$$

$$DR = -11.1 \text{ dB} + 50 \log M$$

M	DR
16	49 dB
32	64 dB
1024	139 dB

2X increase in M → 15dB (2.5-bit) increase in DR

2nd Order ΣΔ Modulator Example

- Digital audio application
- Signal bandwidth 20kHz
- Resolution 16-bit

16-bit → 98dB Dynamic Range

$$DR = -11.1dB + +50\log M$$

$$M_{\min} = 153$$

$M \rightarrow 256=2^8$ to allow some margin & also for ease of digital filter implementation
 → Sampling rate $(2 \times 20\text{kHz} + 5\text{kHz})M = 12\text{MHz}$

Higher Order ΣΔ Modulator Dynamic Range

$$Y(z) = z^{-1}X(z) + (1-z^{-1})^L E(z), \quad L \rightarrow \Sigma\Delta \text{ order}$$

$$\overline{S_X} = \frac{1}{2} \left(\frac{\Delta}{2} \right)^2 \quad \text{sinusoidal input, } STF = 1$$

$$\overline{S_Y} = \frac{\pi^{2L}}{2L+1} \frac{1}{M^{2L+1}} \frac{\Delta^2}{12}$$

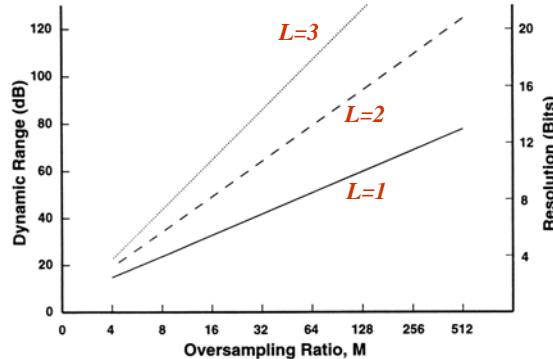
$$\frac{\overline{S_X}}{\overline{S_Y}} = \frac{3(2L+1)}{2\pi^{2L}} M^{2L+1}$$

$$DR = 10\log \left[\frac{3(2L+1)}{2\pi^{2L}} M^{2L+1} \right]$$

$$DR = 10\log \left[\frac{3(2L+1)}{2\pi^{2L}} \right] + (2L+1) \times 10 \times \log M$$

2X increase in M → $(6L+3)$ dB or $(L+0.5)$ -bit increase in DR

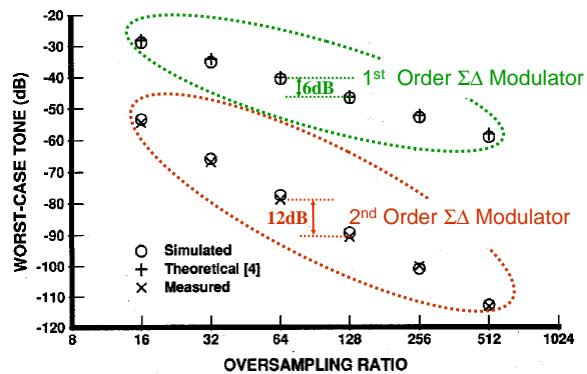
$\Sigma\Delta$ Modulator Dynamic Range As a Function of Modulator Order



- Potential stability issues for $L > 2$

Tones in 1st Order & 2nd Order $\Sigma\Delta$ Modulator

- Higher oversampling ratio \rightarrow lower tones
- 2nd order much lower tones compared to 1st
- 2X increase in M decreases the tones by 6dB for 1st order loop and 12dB for 2nd order loop

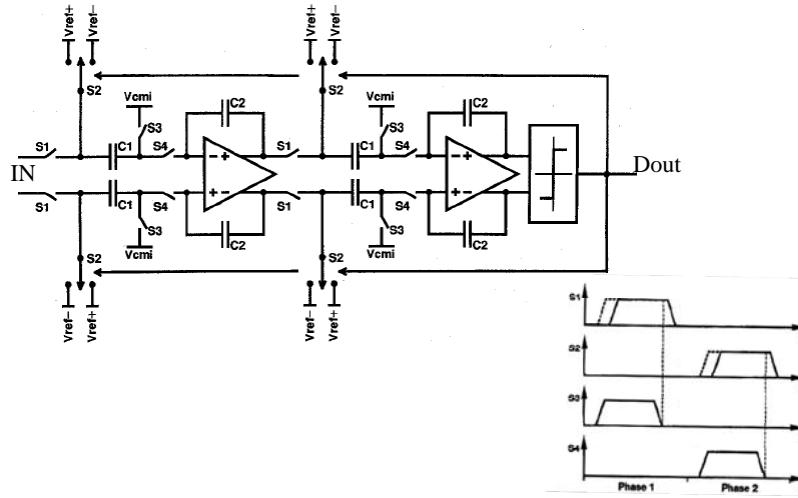


Ref:

B. P. Brandt, et al., "Second-order sigma-delta modulation for digital-audio signal acquisition," IEEE Journal of Solid-State Circuits, vol. 26, pp. 618 - 627, April 1991.

R. Gray, "Spectral analysis of quantization noise in a single-loop sigma-delta modulator with dc input," IEEE Trans. Commun., vol. 37, pp. 588-599, June 1989.

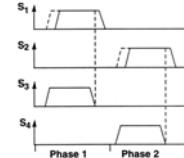
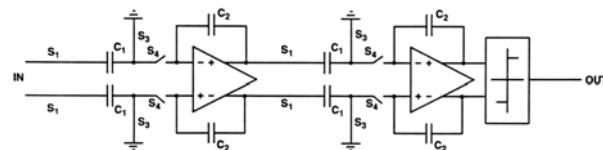
2nd Order $\Sigma\Delta$ Modulator Switched-Capacitor Implementation



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Switched-Capacitor Implementation 2nd Order $\Sigma\Delta$ Phase 1

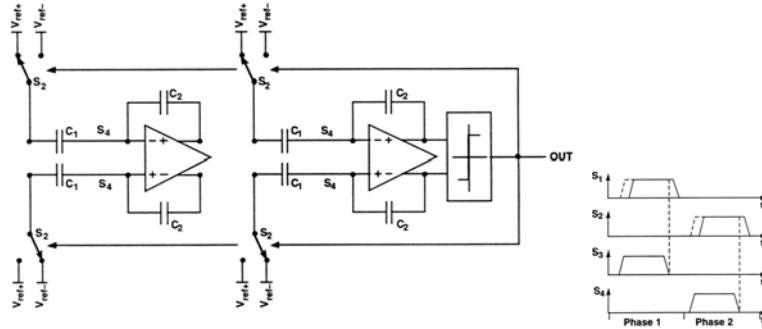


- Sample inputs
- Compare output of 2nd integrator
- At the end of phase1, S3 opens prior to S1 opening

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Switched-Capacitor Implementation 2nd Order $\Sigma\Delta$ Phase 2

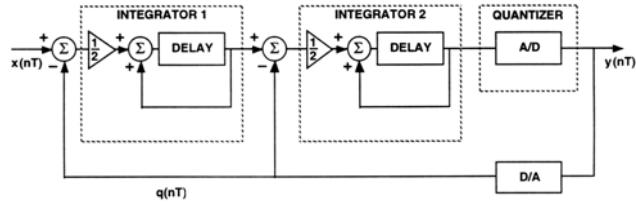


- Enable feedback from output to input of both integrators
- Integrate
- Reset comparator
- At the end of phase2 S4 opens before S2

$\Sigma\Delta$ Implementation Practical Design Considerations

- Internal nodes scaling & clipping
- Finite opamp gain & linearity
- Capacitor ratio errors
- KT/C noise
- Opamp noise
- Power dissipation considerations

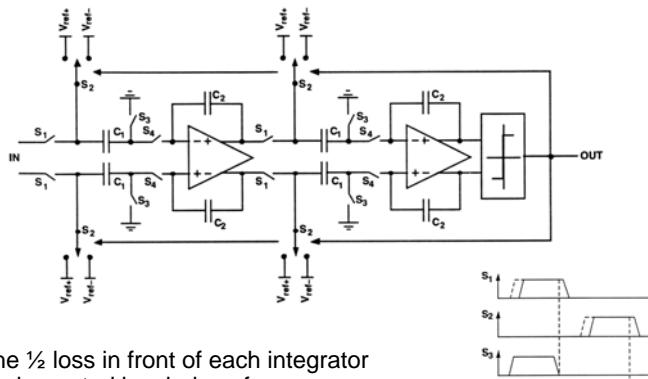
Switched-Capacitor Implementation 2nd Order $\Sigma\Delta$ Nodes Scaled for Maximum Dynamic Range



- Modification (gain of $1/2$ in front of integrators) reduce & optimize required signal range at the integrator outputs $\sim 1.7x$ input full-scale (Δ)

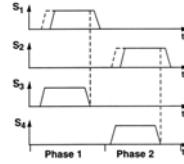
Ref: B.E. Boser and B.A. Wooley, "The Design of Sigma-Delta Modulation A/D Converters," IEEE J. Solid-State Circuits, vol. 23, no. 6, pp. 1298-1308, Dec. 1988.

2nd Order $\Sigma\Delta$ Modulator Switched-Capacitor Implementation



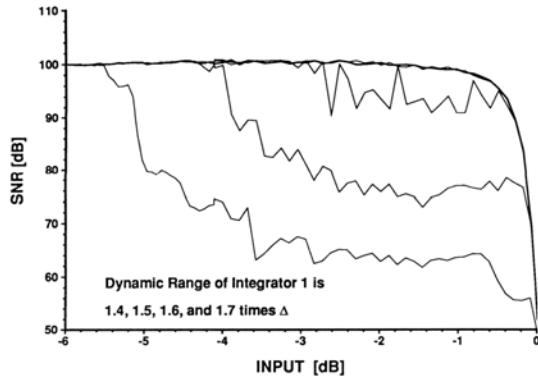
- The $1/2$ loss in front of each integrator implemented by choice of:

$$C_2 = 2C_1$$



2nd Order $\Sigma\Delta$

Effect of Integrator Maximum Signal Handling Capability on SNR

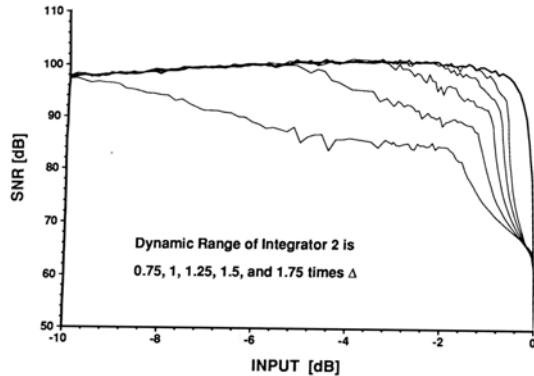


- Effect of 1st Integrator maximum signal handling capability on converter SNR

Ref: B.E. Boser and B.A. Wooley, "The Design of Sigma-Delta Modulation A/D Converters," IEEE J. Solid-State Circuits, vol. 23, no. 6, pp. 1298-1308, Dec. 1988.

2nd Order $\Sigma\Delta$

Effect of Integrator Maximum Signal Handling Capability on SNR

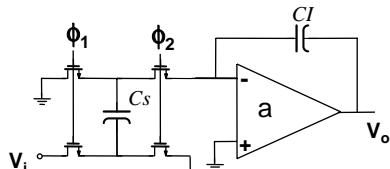


- Effect of 2nd Integrator maximum signal handling capability on SNR

Ref: B.E. Boser and B.A. Wooley, "The Design of Sigma-Delta Modulation A/D Converters," IEEE J. Solid-State Circuits, vol. 23, no. 6, pp. 1298-1308, Dec. 1988.

2nd Order $\Sigma\Delta$

Effect of Integrator Finite DC Gain

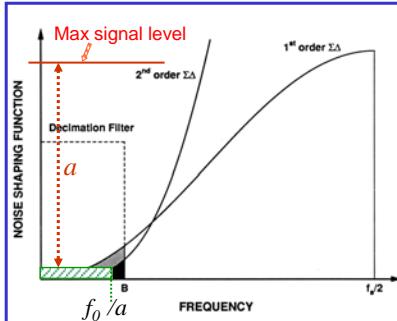
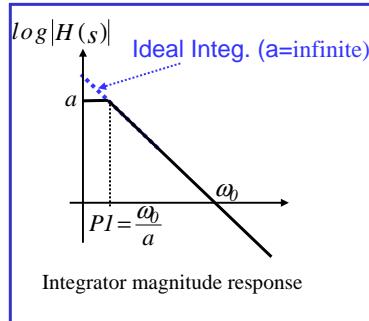


$$H(z)_{ideal} = \frac{Cs}{CI} \times \frac{z^{-1}}{1-z^{-1}}$$

$$H(z)_{Finite DC Gain} = \frac{Cs}{CI} \times \frac{\left(\frac{a}{1+a+\frac{Cs}{CI}} \right) z^{-1}}{1 - \left(\frac{1+a}{1+a+\frac{Cs}{CI}} \right) z^{-1}}$$

2nd Order $\Sigma\Delta$

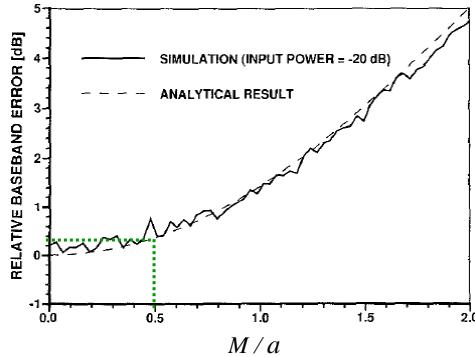
Effect of Integrator Finite DC Gain



- Low integrator DC gain → Increase in total in-band noise
- Can be shown: If $a > M$ (oversampling ratio) → Insignificant degradation in SNR
- Normally DC gain designed to be $\gg M$ in order to suppress nonlinearities

2nd Order $\Sigma\Delta$

Effect of Integrator Finite DC Gain

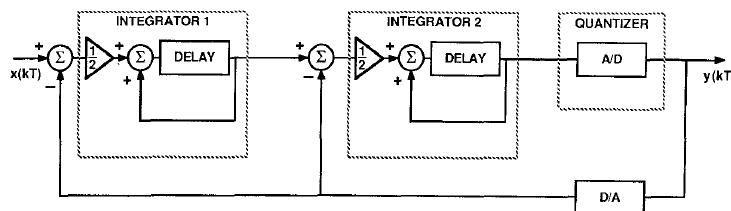


- Example: $a = 2M \rightarrow 0.4\text{dB}$ degradation in SNR

Ref: B.E. Boser and B.A. Wooley, "The Design of Sigma-Delta Modulation A/D Converters," IEEE J. Solid-State Circuits, vol. 23, no. 6, pp. 1298-1308, Dec. 1988.

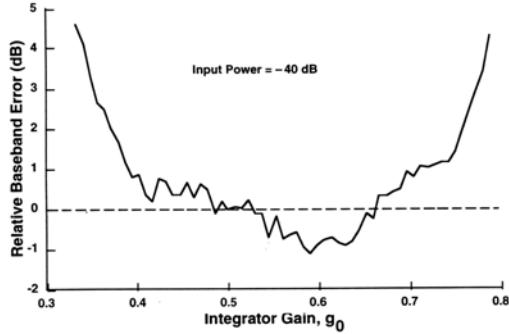
2nd Order $\Sigma\Delta$

Effect of Integrator Overall Integrator Gain Inaccuracy



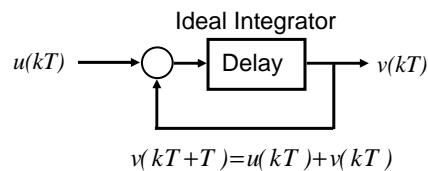
- Gain of $1/2$ in front of integrators determined by ratio of C_1/C_2
- Effect of inaccuracy in ratio of C_1/C_2 inspected by simulation

2nd Order $\Sigma\Delta$ Effect of Integrator Overall Gain Inaccuracy



- Simulation show gain can vary by 20% w/o loss in performance
→ Confirms insensitivity of $\Sigma\Delta$ to component variations
- Note that for gain >0.65 system becomes unstable & SNR drops rapidly

2nd Order $\Sigma\Delta$ Effect of Integrator Nonlinearities

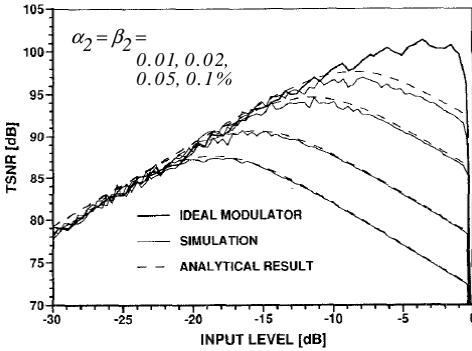


With non-linearity added:

$$v(kT+T) = u(kT) + \alpha_2 [u(kT)]^2 + \alpha_3 [u(kT)]^3 + \dots + v(kT) + \beta_2 [v(kT)]^2 + \beta_3 [v(kT)]^3 + \dots$$

Ref: B.E. Boser and B.A. Wooley, "The Design of Sigma-Delta Modulation A/D Converters," IEEE J. Solid-State Circuits, vol. 23, no. 6, pp. 1298-1308, Dec. 1988

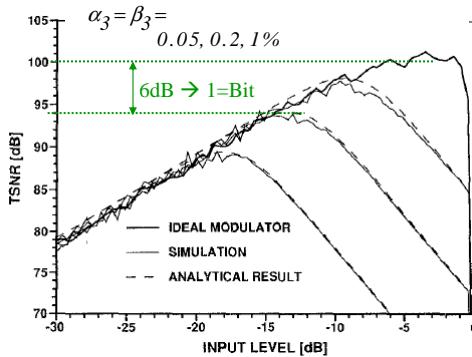
2nd Order $\Sigma\Delta$ Effect of Integrator Nonlinearities



- Simulation for single-ended topology
- Even order nonlinearities can be significantly attenuated by using differential circuit topologies

Ref: B.E. Boser and B.A. Wooley, "The Design of Sigma-Delta Modulation A/D Converters," IEEE J. Solid-State Circuits, vol. 23, no. 6, pp. 1298-1308, Dec. 1988.

2nd Order $\Sigma\Delta$ Effect of Integrator Nonlinearities



- Simulation for single-ended topology
- Odd order nonlinearities (3rd in this case)

Ref: B.E. Boser and B.A. Wooley, "The Design of Sigma-Delta Modulation A/D Converters," IEEE J. Solid-State Circuits, vol. 23, no. 6, pp. 1298-1308, Dec. 1988.