EE247
Lecture 26

- Administrative
  - Final exam:
    - Date: Wed. Dec. 15th
    - Time: 12:30pm-3:30pm
    - Location: 289 Cory
    - Closed book/course notes
    - No calculators/cell phones/PDAs/Computers
    - You can bring two 8x11 paper with your own notes
    - Final exam covers the entire course material

Oversampled Converters
Cont'd

- Higher order ΣΔ modulators
  - Single-loop single-quantizer modulators with multi-order filtering in the forward path
    - Example: 5th order ΣΔ
      - Modeling
      - Noise shaping
      - Complex loop filters
      - Stability
      - Voltage scaling, input range scaling
      - Tones, Dither, kT/C noise
      - Interference via V_{ref}

      → Effect of component nonlinearities on ΣΔ performance

Modeling ΣΔ Nonlinearities

- Many component nonlinearities contribute errors
  - Important to identify the ones which incur significant errors and analyze those only
  - Unnecessarily complex models reduce the chance to find relevant problems, and, perhaps, solutions
  - As with all nonidealities, model one at a time
- Expect errors from the 2nd integrator to be reduced by the gain of the 1st integrator
  - Errors further downstream are even less significant

Capacitor Voltage Coefficient

- Ideal capacitor

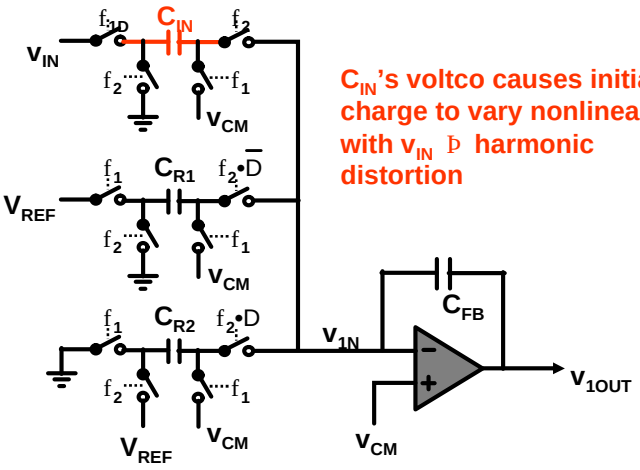
$$Q = CV$$

- Practical capacitor (1st order model)

$$Q = C(V)V \qquad \text{with}$$
$$Q(V) = C_o(1 + aV + \ldots)V$$

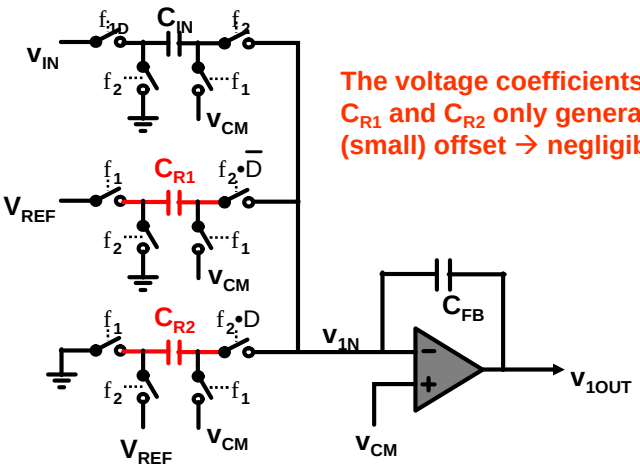
- Typical voltage coefficients
  - Poly-poly capacitors 10 ppm/V
  - Metal-metal capacitors 1 … 10 ppm/V

Integrator 1



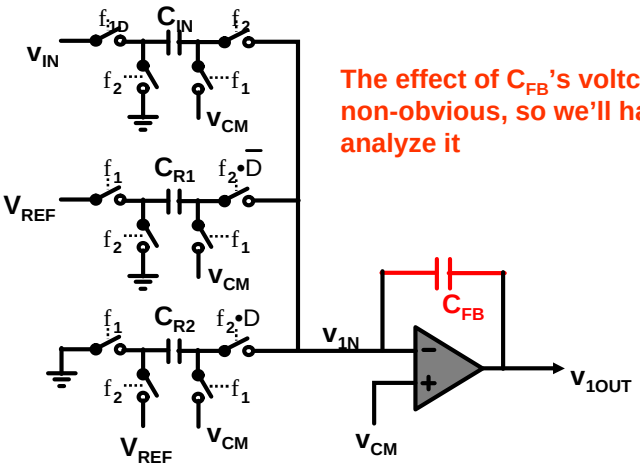
C_{IN}'s voltco causes initial charge to vary nonlinearly with v_{IN} Þ harmonic distortion

Integrator 1



The voltage coefficients of C_{R1} and C_{R2} only generates a (small) offset → negligible

Integrator 1



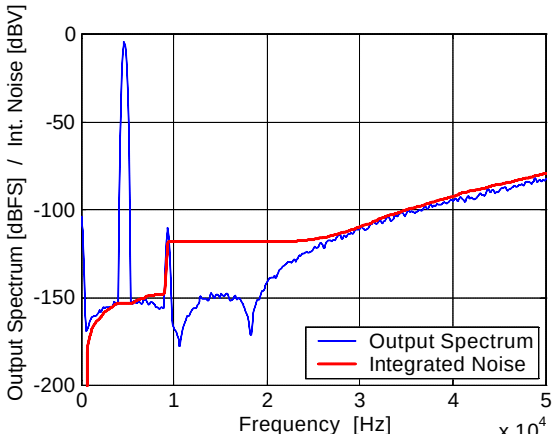
The effect of C_{FB}'s voltco is non-obvious, so we'll have to analyze it

C_{IN} Voltage Coefficient

- From charge conservation (V_{CM}=0, C_{R1}=C_{R2}=C_R):

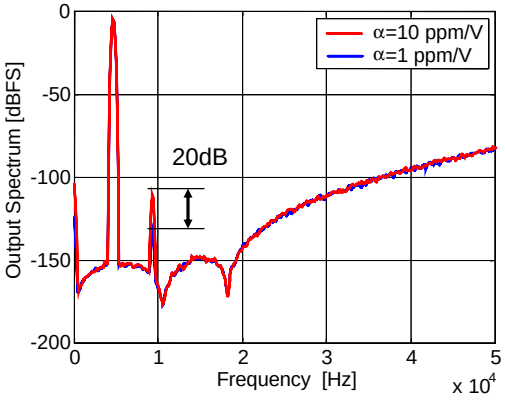
$$V_{1OUT}(k) = \underbrace{V_{1OUT}(k-1)}_{\text{integration}} + \underbrace{\frac{C_{IN}}{C_{FB}} V_{IN}(k-1) + a\frac{C_{IN}}{C_{FB}} V_{IN}^2(k-1)}_{\text{converter input}} \underbrace{- D\frac{C_R}{C_{FB}} V_{REF}}_{\text{1-bit feedback}}$$

C_{IN} Voltage Coefficient



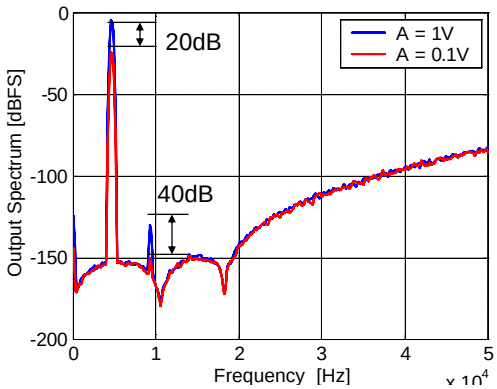
- $V_{in} = V_{FS} = 1V$
- Spectrum scaled for V_{FS} → 0dB (window lowers peak)
- Noise integral excludes DC, fundamental
- α = 10 ppm/V
- 2nd harmonic at –103dB dominates noise!
- Let's characterize it …

C_{IN} Voltage Coefficient



2nd harmonic increases 1dB per 1dB increase of α

C_{IN} Voltage Coefficient



2nd harmonic increases 2dB per 1dB increase of the input signal amplitude

C_{FB} Voltage Coefficient

- Let's look next at the voltage coefficient of the feedback capacitor in the 1st integrator
- We "turn off" all other nonidealities – C_{IN} voltage coefficients, noise, etc.
  - Makes it easier to find the effect of C_{FB} on the modulator
  - Downside: we miss potential interactions between nonidealities
  - Often they are negligible: nonidealities (like voltage coefficients) produce small errors … linear superposition applies
  - Of course it's a good idea to run a complete verification at the end
  - And we'll get to diagnose the "real thing" soon enough … without the insight gained from such idealized simulations it's next to impossible to diagnose a complex chip
- Evaluating the effect of the C_{FB} voltage coefficient requires solving a quadratic equation, as shown in the next slide …

C_{FB} Voltage Coefficient

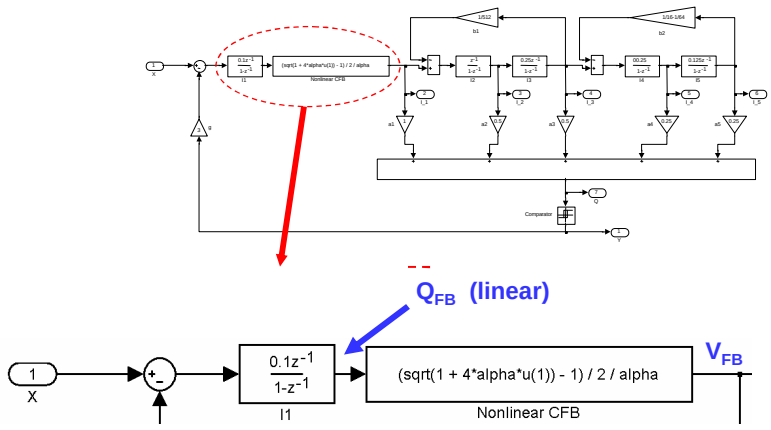
$$V_{OUT1} = \frac{Q_{FB}}{C_{FB1}(V_{OUT1})}$$

$$= \frac{-1 + \sqrt{1 + \frac{4aQ_{FB}}{C_{FB1}}}}{2a}$$

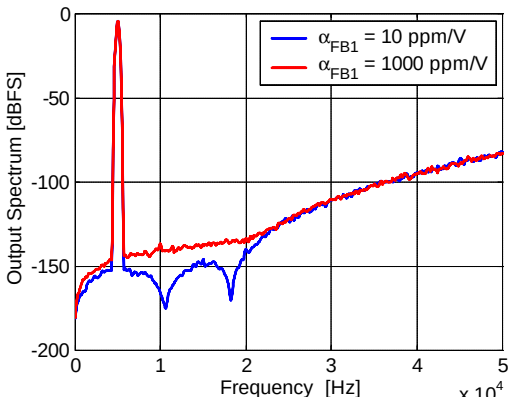
$$Q_{FB}(k) = Q_{FB}(k-1) + C_{IN}V_{IN} + DC_RV_{REF}$$

(same as output from linear integrator)

C_{FB} Voltage Coefficient

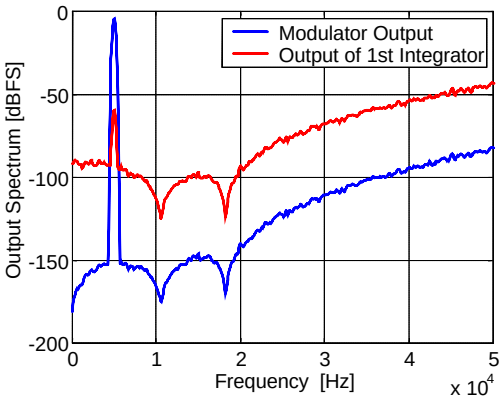


C_{FB} Voltage Coefficient



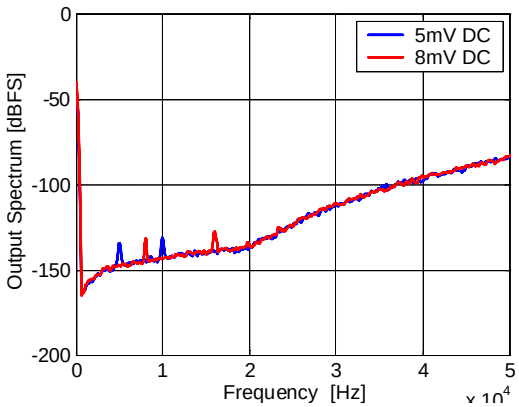
- Effect less pronounced than for C_{IN}
- Noise remains zero at DC
- First order noise for large α
- Nonlinearities operating on shaped noise change the shape of the noise …
  - No linear model can predict this
- No harmonics … why?

1st Integrator Output



- The input signal appears much attenuated at the output of the 1st Integrator
- This signal appears across C_{FB} … and since it contains no strong tones it produces no harmonics

DC Input



- For α = 1000 ppm/V, tones produced by C_{FB} are much larger than native tones, but move with the same velocity as native tones (1.2kHz/mV)
- Where are these tones coming from?

Quantization Noise Nonlinearity

- Native tones at a frequency f_D close to $f_s/2$ have much higher power than in-band tones

$$f_D = \frac{f_s}{2} - \frac{f_d}{2}$$

- When this tone passes a nonlinearity in the modulator loop filter, it produces distortion

$$\sin^2(2\pi f_D t) = \frac{1}{2} - \frac{1}{2}\cos[2\pi(2f_D)t]$$

Quantization Noise Nonlinearity

$$\sin^2(2pf_D t) = \frac{1}{2} - \frac{1}{2}\cos[2p(2f_D)t]$$

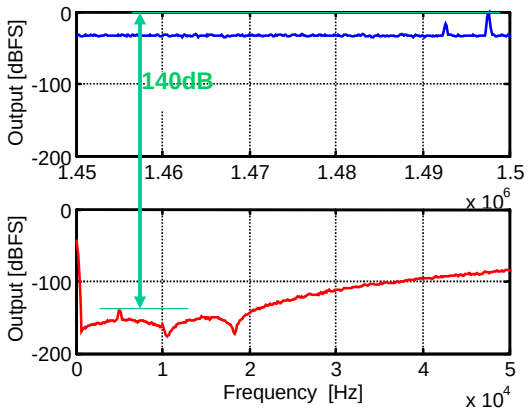
- In the sampled data system,

$$2f_D = f_s - f_d$$

  maps to f_d

- Small nonlinearities applied to aggressively shaped quantization noise can produce big tone problems …

C_{FB} Voltage Coefficient



- α = 10 ppm/V used in simulation
- Tones appear near $f_s/2$, as expected
- Apparently these are "folded" to the base-band
- As long as the tones are below -100dB→ acceptable

Effect of Circuit Non-Idealities

- In principle, the digital filter removes out-of-band tones
  - Except their distortion components falling in the baseband, caused by nonlinearities in the modulator loop filter
  - Except components that are mixed down to baseband due to noise in the DAC reference
- The C_{FB1} voltage coefficient adds only a small nonlinearity to the quantization noise path
  - Fortunately this nonlinearity is applied to the integral of the quantization noise and sees only a small signal component
- Nonlinearities in the amplifier are much more Other source of nonlinearity→ switch induced distortion
  - Including those in the model is left as an exercise …including effect of 3rd order nonlinearities
- Maintaining extremely high levels of linearity in H(z) is the most significant transistor-level design challenge of high resolution ΣΔ modulators

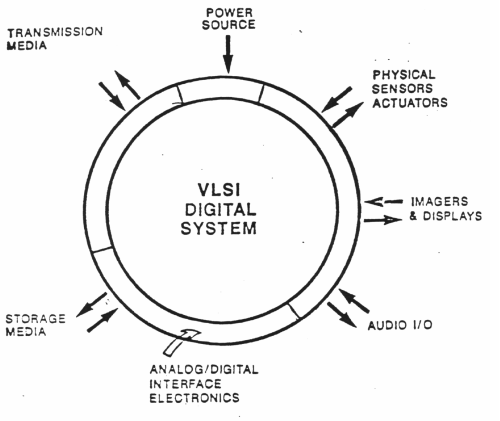
Summary
Oversampled ADCs

- Speed is traded for resolution
- Noise shaping utilized to reduce baseband quantization noise power
- Reduced precision requirement for analog building blocks compared to Nyquist rate converters
- Relaxed transition band requirements for analog anti-aliasing filters
- Utilizes low cost, low power digital filtering

Material Covered in EE247

- Filters
  - Continuous-time filters
    - Biquads & ladder type filters
    - Opamp-RC, Opamp-MOSFET-C, gm-C filters
    - Automatic frequency tuning
  - Switched capacitor (SC) filters
- Data Converters
  - D/A converter architectures
  - A/D converter
    - Nyquist rate ADC- Flash, Interpolating & Folding, Pipeline ADCs,….
    - Self-calibration techniques
    - Oversampled converters

Role of Analog Interfaces in VLSI Systems

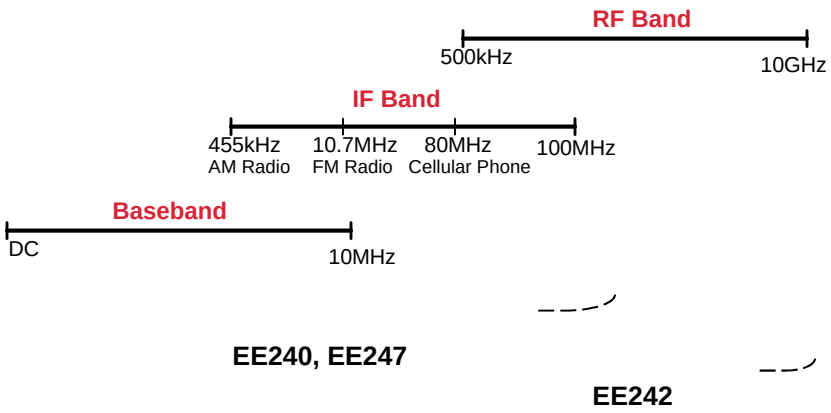


Ref: Prof. P. R. Gray, University of California @ Berkeley EECS249

Systems Including Analog-Digital Interface Circuitry

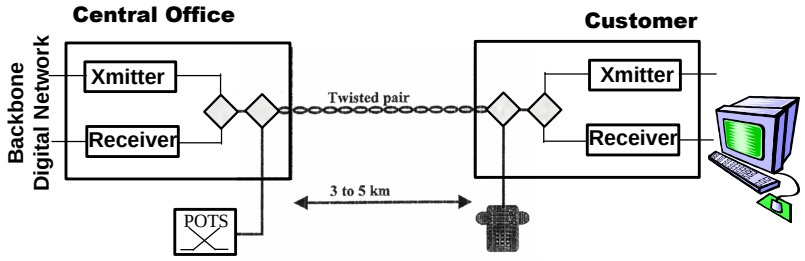
- Wireline communications
  - Telephone related (DSL, ISDN, CODEC)
  - Television circuitry (Cable modems, TV tuners…)
  - Ethernet (Gigabit, 10/100BaseT…)
- Wireless
  - Cellular telephone (CDMA, Analog, GSM….)
  - Wireless LAN (Blue tooth, 802.11a/b/g…..)
  - Radio (analog & digital), Television
- Disk drives
- Fiber-optics systems

Frequency Range



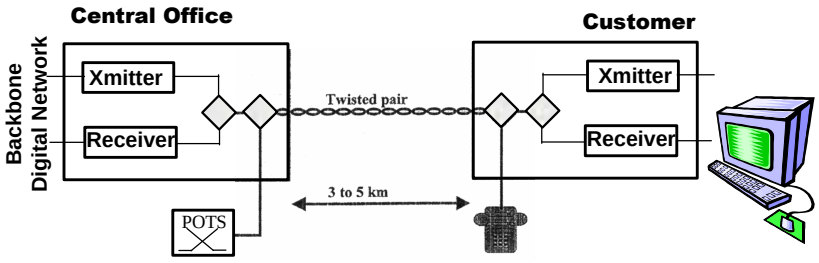
Wireline Communications Telephone Based

Data Transmission Over Existing Twisted-Pair Phone Lines



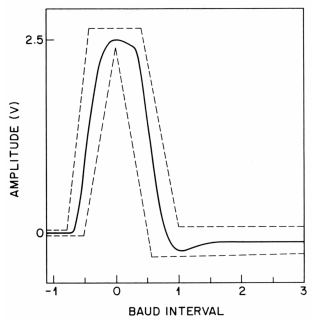
- Data transmitted over existing phone lines covering distances close to 3.5miles
  - ISDN
  - HDSL, SDSL,……
  - ADSL

Data Transmission Over Twisted-Pair Phone Lines
ISDN (U-Interface) Transceiver



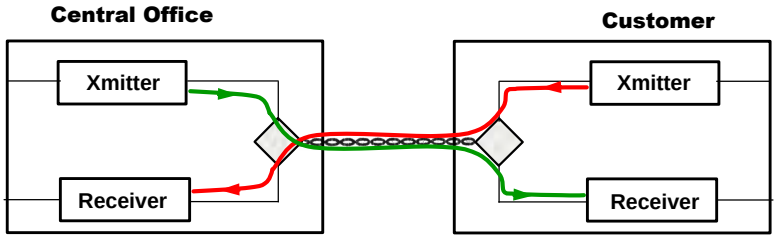
- Full duplex transmission (RX & TX signals sent simultaneous)
- 160kbit/sec baseband data (80kHz signal bandwidth)
- Standardized line code 2B1Q (4 level code 3:1:-1:-3)
- Max. desired loop coverage 18kft (~36dB signal attenuation)
- BER (bit-error-rate) 10^{-7} →(min. SNDR=27dB)

Analog Front-End
Transmit Pulse Shape

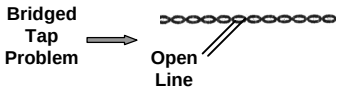


Standard mandates a pulse mask → Ensure min. high-frequency content on the line to avoid spurious coupling into other lines

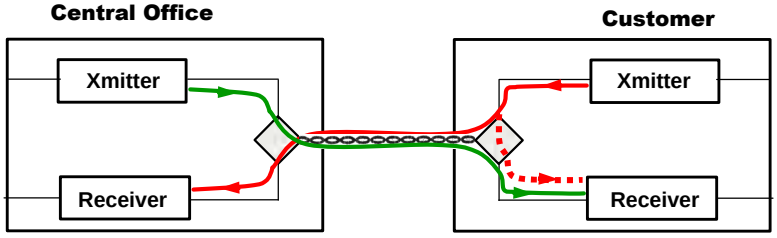
ISDN (U-Interface) Transceiver
Echo Problem



- Transformer coupling to line
  - For a perfectly matched system, no leakage of TX signal into RX path.
  - Unfortunately, system has poor matching + complicating factor of bridged-taps

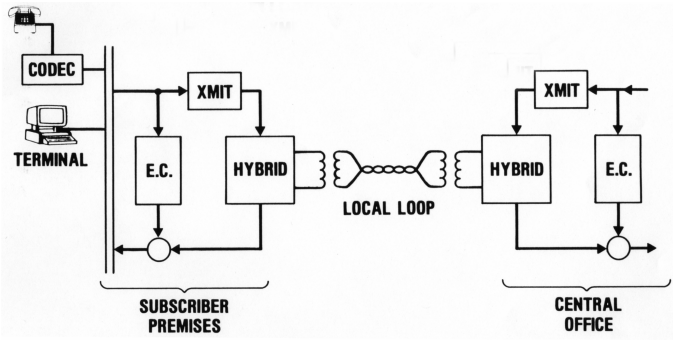


ISDN (U-Interface) Transceiver
Echo Problem



- System full duplex transmission → RX & TX signals sent simultaneous (& at the same frequency band)
  - Leakage of TX signal to RX path (echo)
  - In the worst case the echo could be *30dB* higher compared to the received signal!!

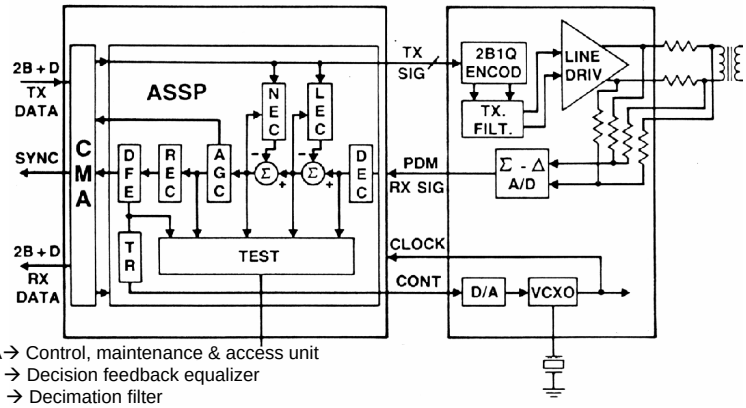
ISDN (U-Interface) Transceiver Echo Cancellation



- Echo cancellation performed in the digital domain
  - Transversal adaptive digital filter → echo cancellation
- Any non-linearity incurred by the analog circuitry makes echo canceller much more complex

  → Desirable to have high linearity analog circuitry (75dB range)

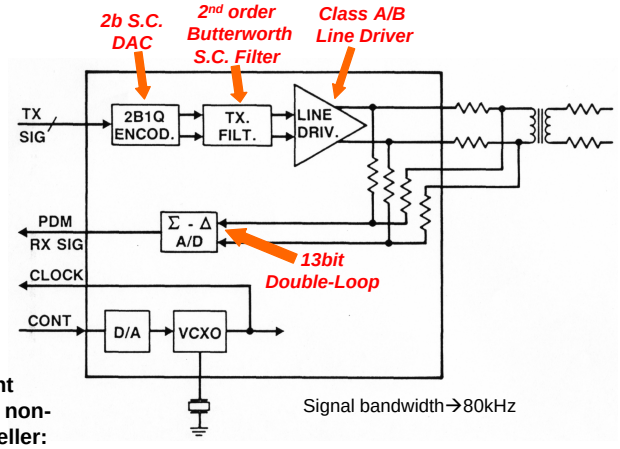
Simplified Transceiver Block Diagram



CMA→ Control, maintenance & access unit
DFE → Decision feedback equalizer
DEC → Decimation filter
REC → Reconstruction filter
LEC & NEC →Linear/non-linear echo-canceller

Ref: H. Khorramabadi, O. E. Agazzi, et. al"An ANSI standard ISDN transceiver chip set, " *IEEE International Solid-State Circuits Conference*, vol. XXXII, pp. 256 - 257, February 1989.

Analog Front-End

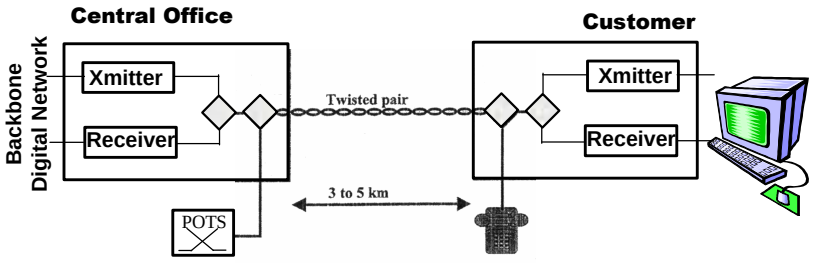


To avoid stringent requirements for non-linear echo canceller: -> high linearity analog circuitry needed (~ 75dB)

Signal bandwidth→80kHz

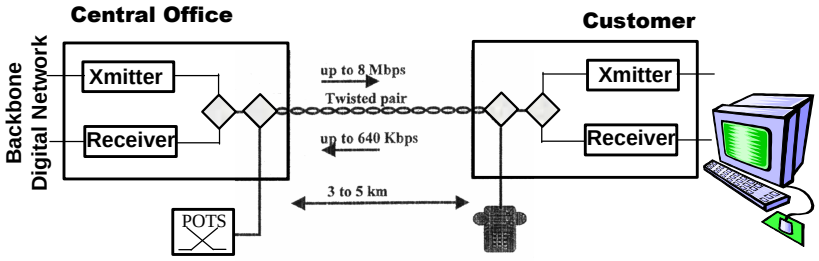
Chip Photo

Data Transmission Over Twisted-Pair Phone Lines
DSL (Digital Subscriber Loop)



- HDSL &SDSL more like ISDN @ higher frequencies
  - Full duplex transmission with RX & TX signals on the same frequency band

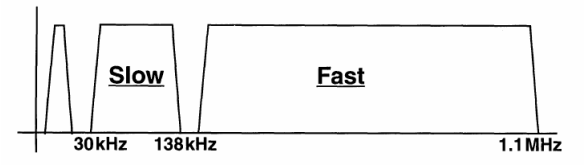
Data Transmission Over Twisted-Pair Phone Lines
ADSL (Digital Subscriber Loop)



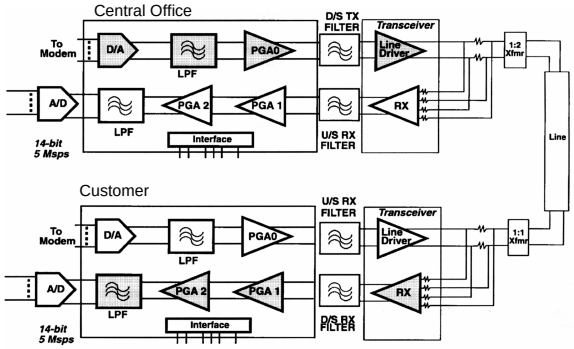
- In USA mostly ADSL → FDM (frequency division multiplex)
  - Signal from CO to customer on a different band compared to customer to CO
    - Echo cancellation can be performed by simple filtering
  - Data rates up to 8Mbps (much higher compared to ISDN)

ADSL Signal Characteristics

- Main difference compared to ISDN: TX & RX signals on different frequency bands
  - Downstream (*fast*, from CO to customer) 138kHz to 1.1MHz
  - Upstream (*slow*, from customer to CO) 30kHz to 138kHz
    - Echo cancellation much easier
- More severe signal attenuation at high frequencies (1MHz DSL v.s. 80kHz ISDN)



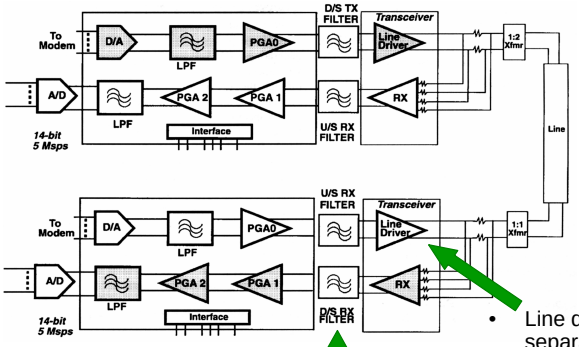
Typical ADSL Analog Front-End



- ADC 16/14b with 14bit linearity, pipeline with auto. calibration @ 4.4Ms/s
- DAC 16/14b with 14bit linearity, S.C. with auto. calibration
- On-chip filters 3rd to 4th order LPF with f_c 1.1MHz for downstream and 138kHz upstream (typically continuous-time type filters with on-chip frequency tuning)

Ref: D.S. Langford, et al, "A BiCMOS Analog Front-End Circuit for an FDM-Based ADSL System," *IEEE Journal of Solid State Circuits*, Vol. 33, No. 9, pp. 1383-1393, Dec. 1998.

Typical ADSL Analog Front-End



- Notice band selection filters are off-chip due to stringent noise requirements (3nV/rtHz)
  - Discrete LC type

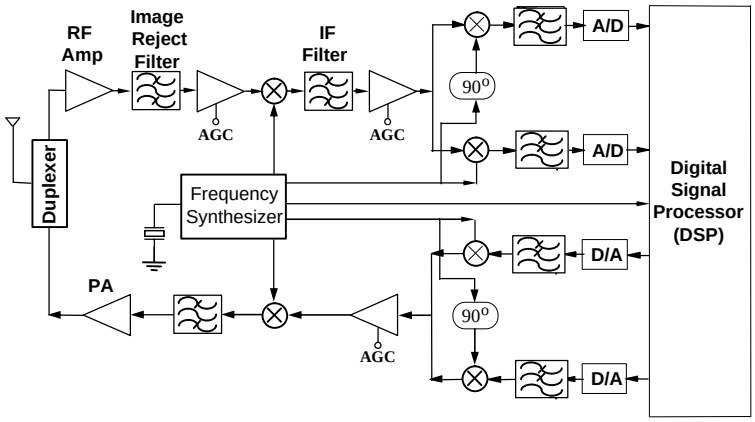
- Line driver on a separate bipolar chip to achieve the required high output signal levels with high power efficiency

Wireless Communication Circuits

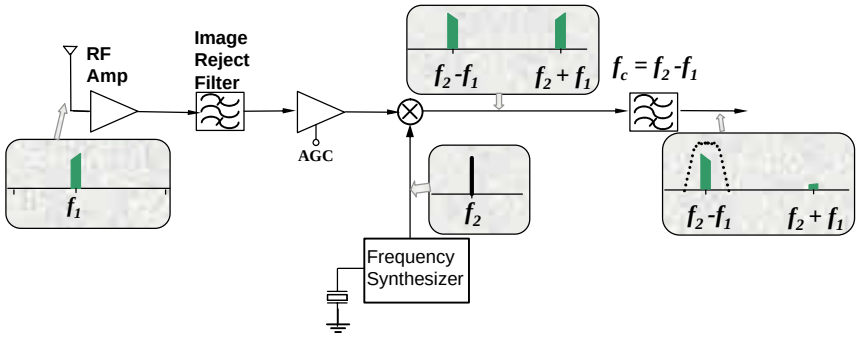
Wireless Circuits

- Differ from wired comm. circuits
  - Includes RF circuitry+IF circuitry+baseband circuits (three different frequency ranges)
  - Signal scenarios in wireless receivers more challenging
  - Requirement for received signal BER in the order of 10^{-3} →(min. SNR~9dB)

Typical Cellular Phone Block Diagram

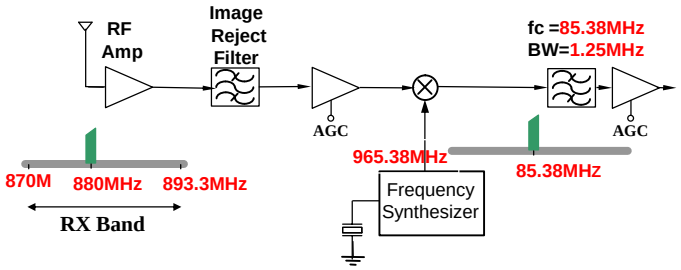


Superheterodyne Receiver



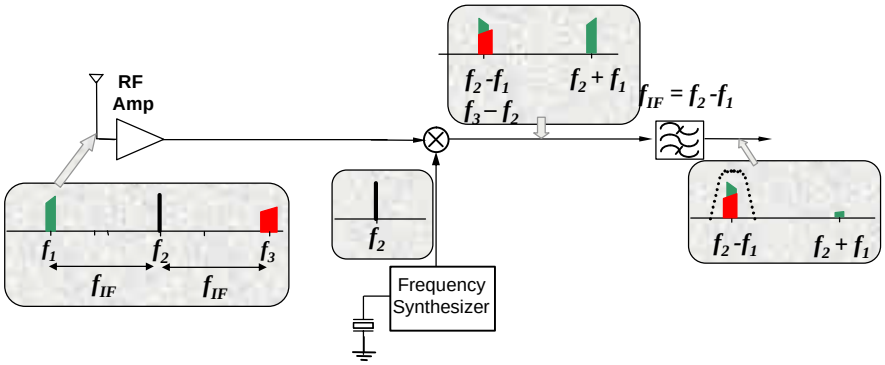
- One or more intermediate frequency (IF)
- Periodic signal at a frequency equal to the desired RX signal + or – IF frequency is provided by a Local Oscillator
- RX signal is frequency shifted to a fixed frequency (IF filter center frequency)

RF Superheterodyne Receiver Example: CDMA Receiver



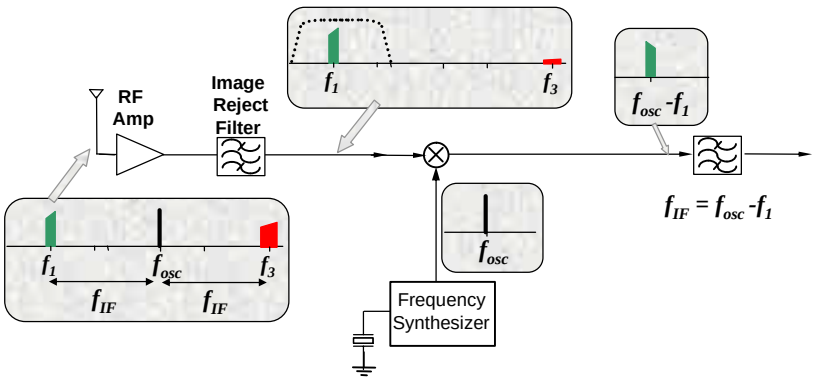
- Received frequency is mixed down to a <u>fixed</u> IF frequency and then filtered with a bandpass filter

Why Image Reject Filter?



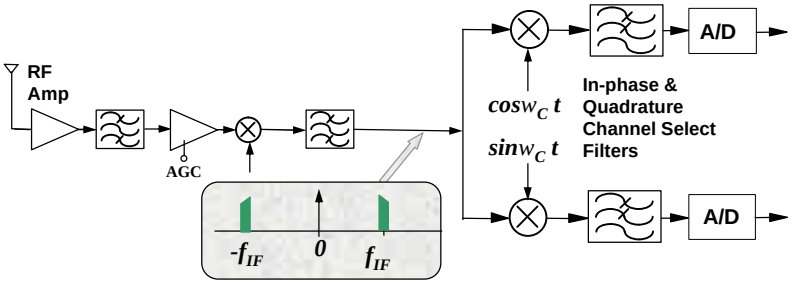
- Any signal @ the image frequency of the RX signal with respect to Osc. frequency will fall on the desired RX signal and cause impairment

Why Image Reject Filter?



- Image reject filter attenuate signals out of the RX band
- Typically, image reject filters are ceramic or LC type filters

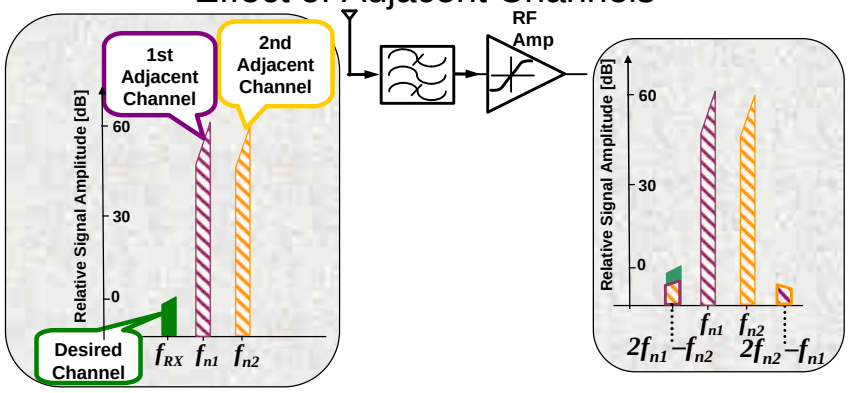
Quadrature Downconversion



- In systems with phase or freq. modulation, since signal is not symmetric around f_{IF} , directly converting down to baseband corrupts the sidebands

  → Quadrature downconversion overcomes the problem

Effect of Adjacent Channels



- Adjacent channels can be as much as 60dB higher compared to the desired RX signal!
- Linearity of stages prior and including channel selection filters extremely important

Effect of Adjacent Channels

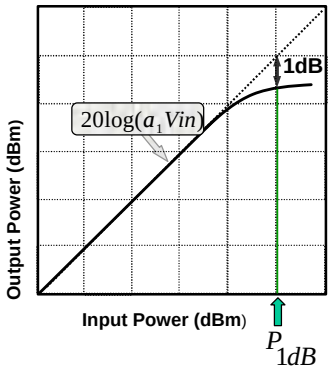
- Due to existence of large unwanted signals & limited dynamic range for the front-end circuitry:
  - Can not amplify the signal up front due to linearity issues
  - Need to allocate amplification/filtering numbers to RX blocks carefully
  - Can only amplify when unwanted signals are filtered adequately
  - System design critical with respect to tradeoffs affecting:
    - Gain
    - Linearity
    - Power dissipation
    - Chip area

Wireless Communications Linearity

- Most critical contributor to non-linearity in wireless communications circuits 3rd order intermod.:
- Two forms of linearity measurements:
  - 1dB compression point→ Useful for the cases where the desired received channel is strong
  - 3rd order intercept point → Good measure for when interferers much larger compared to the desired channel

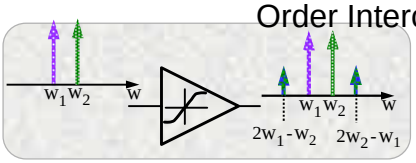
Wireless Communications Measure of Linearity

1dB Compression Point



$$Vout = a_1 Vin + a_2 Vin^2 + a_3 Vin^3 + ...$$

Wireless Communications Measure of Linearity Third Order Intercept Point

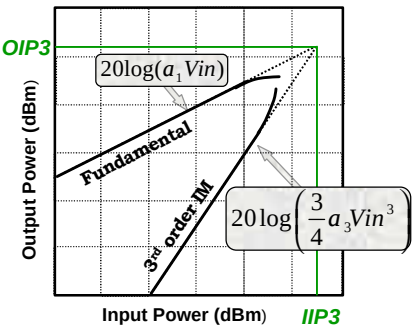


$$Vout = a_1 Vin + a_2 Vin^2 + a_3 Vin^3 + ...$$

$$IM_3 = \frac{3rd}{1st}$$

$$= \frac{3}{4}\frac{a_3}{a_1} Vin^2 + \frac{25}{8}\frac{a_5}{a_1} Vin^4 + ...$$

$$= 1 @ IP3$$

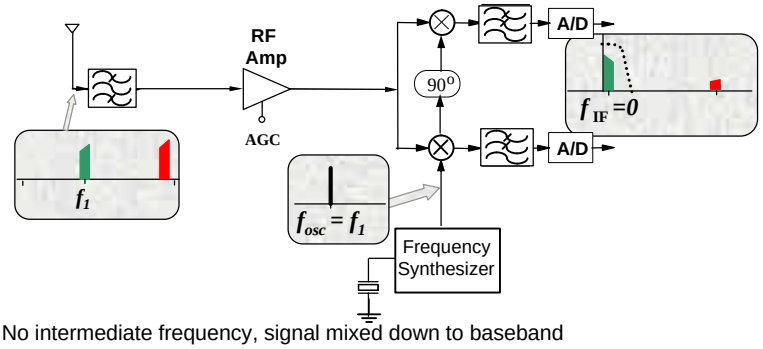


Typically:

$$IIP_3 - P_{1dB} = 9.6dB$$

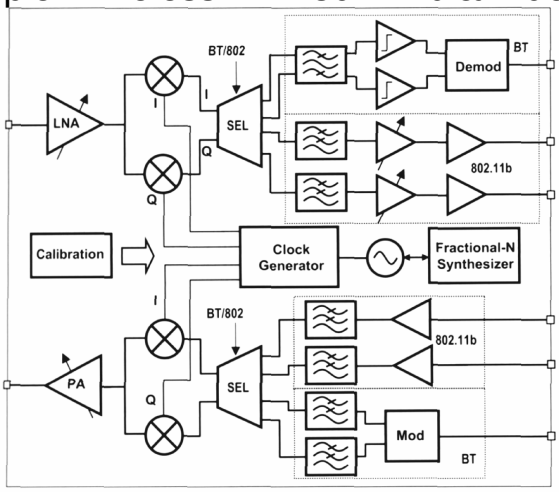
Most common measure of linearity for wireless circuits:
→ OIP3 & IIP3, Third order output/input intercept point

Homodyne Receiver



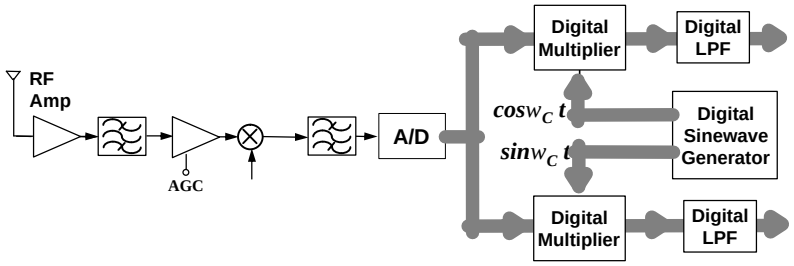
- No intermediate frequency, signal mixed down to baseband
- Almost all of the filtering performed at baseband
  - Higher levels of integration possible
  - Issue to be aware of:
    - Requirements for the baseband filters very stringent
    - Since the local oscillator frequency is exactly at the same freq. as the RX signal freq. → can cause major DC offsets can drive the receiver front-end into non-linear region

Example: Wireless LAN 802.11b & Bluetooth



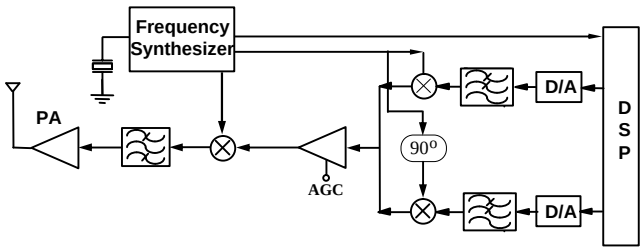
Ref: H. Darabi, et al, "A Dual Mode 802.11b/Bluetooth Radio in 0.35um CMOS," *International Solid State Circuits Conference*, 2003 pp. 86-87.

Digital IF Receiver (IF sampling)



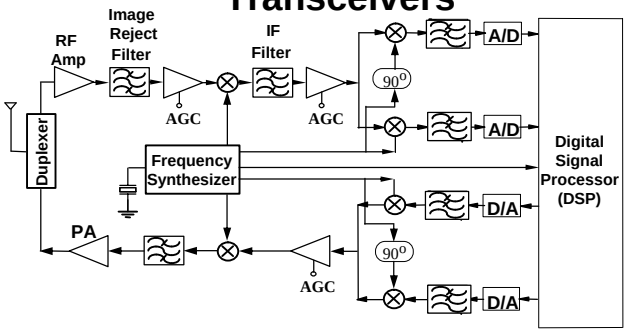
- IF signal is converted to digital →most of signal processing performed in the digital domain
- Performance requirement for ADC extremely demanding in terms of noise, linearity, and dynamic range!
- With advancement of ADCs may be the architecture of choice in the future

Typical Wireless Transmitter



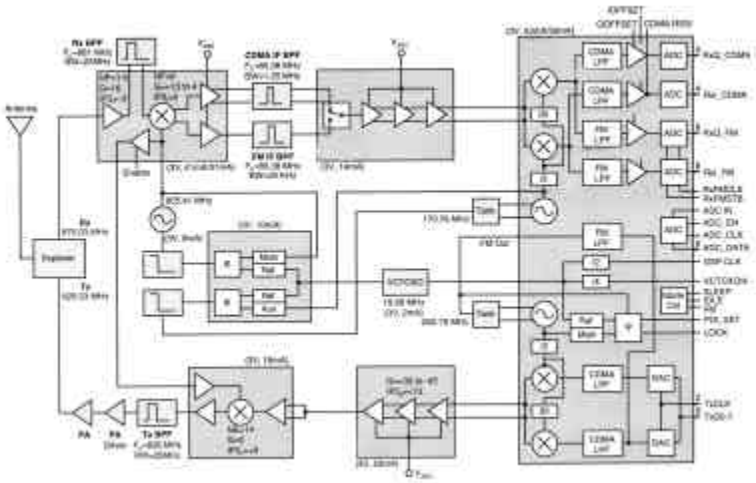
•Transmit signal shipped from DSP to the analog front-end in the form of I& Q signals
•Signal converted to analog form by D/A
•Lowpass filter provides pulse shaping
•In-phase & Quad. Components combined and then mixed up to RF
•Power amplifier amplifies and provides the low-impedance output

Analog Filters in Typical Wireless Transceivers



Filters	***Function***	***Type***
RF Filter	Image Rejection	Ceramic or LC
IF Filter	Channel selection	SAW
Base-band Filters	Channel Selection & Anti-aliasing for ADC	Integrated Cont.-Time or S.C.

Example: Dual Mode CDMA (IS95)& Analog Cellular Phone



Example: Dual Mode CDMA (IS95)& Analog Cellular Phone

- Baseband analog circuitry includes:
  - CDMA
    - 4bit flash type ADC clock rate 10MHz
    - 8bit segmented TX DAC clock rate 10MHz (shared with FM)
    - 7^{th} order elliptic RX lowpass filter corner freq. 650kHz
    - 3^{rd} order chebyshev TX lowpass filter corner freq. 650kHz
  - FM (analog)
    - 8bit successive approximation ADCs clock rate 360kHz
    - 5^{th} order chebyshev RX lowpass filter corner frequency 14kHz
    - 3^{rd} order butterworth TX lowpass filter corner frequency 27kHz

Summary

- Examples from wireline & wireless systems utilizing analog & RF circuitry discussed
- Analog circuits still remain the interface→ connecting the digital world to the real world!