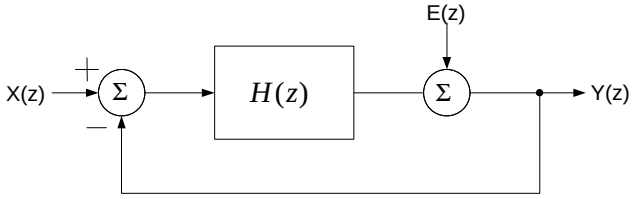
EE247
Lecture 25

- Higher order ΣΔ modulators
  - Last lecture→ Cascaded ΣΔ modulators (MASH)
  - This lecture → Forward path multi-order filter
    - Example: 5th order ΣΔ
      - Modeling
      - Noise shaping
      - Effect of various nonidealities on the ΣΔ performance

Higher Order ΣΔ Modulators
Forward Path Multi-Order Filter



$$Y(z) = \frac{H(z)}{1+H(z)}X(z) + \frac{1}{1+H(z)}E(z)$$

$$NTF = \frac{Y(z)}{E(z)} = \frac{1}{1+H(z)}$$

- Zeros of NTF (poles of H(z)) can be positioned to flatten baseband noise spectrum
- Main issue → Ensuring stability for 3rd and higher orders

Overview

- Building behavioral models in stages
- A 5th-order, 1-Bit ΣΔ modulator
  - Noise shaping
  - Complex loop filters
  - Stability
  - Voltage scaling
  - Effect of component nonidealities

Building Models in Stages

- When modeling a complex system like a 5th-order ΣΔ modulator, model development proceeds in stages
  - Each stage builds on its predecessor
- Design goal → detect and eliminate problems at the highest possible level of abstraction
  - Each successive stage consumes progressively more engineering time
- Our ΣΔ model development proceeds in stages:
  - Stage 0 gets to the starting line: Collect references, talk to veterans
  - Stage 1 develops a practical system built with ideal subcircuits
  - Stage 2 models key subcircuit nonidealities and translates the results into real-world subcircuit performance specifications
  - Real-world model development includes a critical stage 3: Adding elements to earlier stages to model significant surprises found in silicon

Stage 1

- In stage 1, we'll study a model for a practical ΣΔ modulator topology built with ideal blocks
- Stage 1 model focus
  - Signal amplitudes
  - Stability
    - Worst-case inputs
    - Unstable systems can't graduate to stage 2
  - Quantization noise shaping
- Verify performance and functionality for all regions of operation, find and test worst-case inputs
- Determine appropriate performance metrics and build up (software) infrastructure

ΣΔ Modulator Filter Design

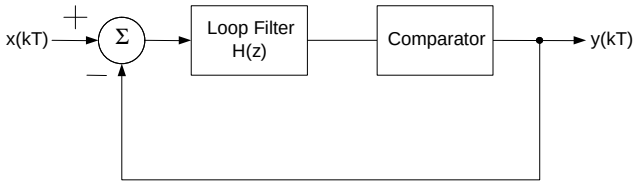
- Procedure
  - Establish requirements
  - Design noise-transfer function, NTF
  - Determine loop-filter, H
  - Synthesize filter
  - Evaluate performance, stability

Ref: R. W. Adams and R. Schreier, "Stability Theory for ΔΣ Modulators," in Delta-Sigma Data Converters, S. Norsworthy et al. (eds), IEEE Press, 1997, pp. 141-164.

Example: Modulator Specification

- Example: Audio ADC
  - Dynamic range — DR — 16 Bits
  - Signal bandwidth — B — 20 kHz
  - Nyquist frequency — f_N — 44.1 kHz
  - Modulator order — L — 5
  - Oversampling ratio — $M = f_s/f_N$ — 64
  - Sampling frequency — f_s — 2.822 MHz
- The order L and oversampling ratio M are chosen based on
  - SQNR > 120dB (20dB below thermal noise)

Modulator Block Diagram



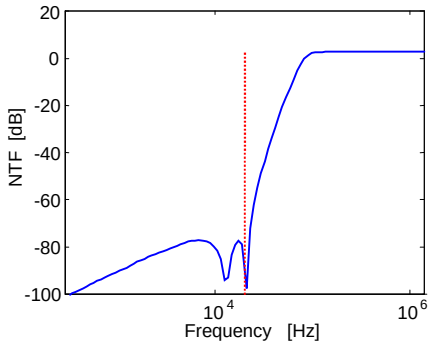
$$\text{STF} = \frac{Y(z)}{X(z)} = \frac{H(z)}{1+H(z)}$$

$$\text{NTF} = \frac{Y(z)}{E(z)} = \frac{1}{1+H(z)}$$

Approach:
Design NTF and solve for H(z)

Noise Transfer Function, NTF(z)

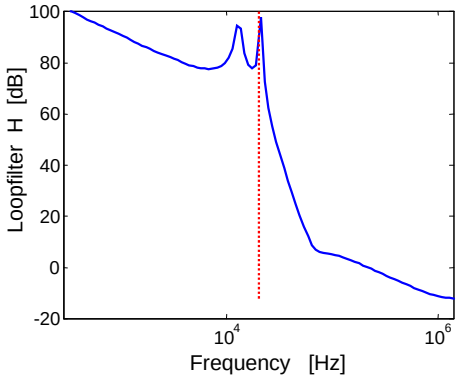
```
% stop-band attenuation Rstop ...

Rstop = 80;
[b,a] = cheby2(L, Rstop, 1/M, 'high');

% normalize
b = b/b(1);
NTF = filt(b, a, 1/fs);
```



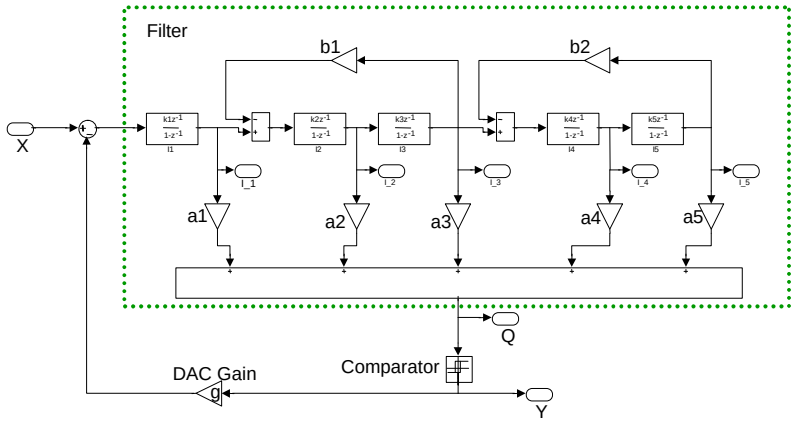
Loop-Filter, H(z)

$$\text{NTF} = \frac{Y(z)}{E(z)} = \frac{1}{1+H(z)}$$

$$\rightarrow H(z) = \frac{1}{NFT} - 1$$



Modulator Topology
Simulation Model

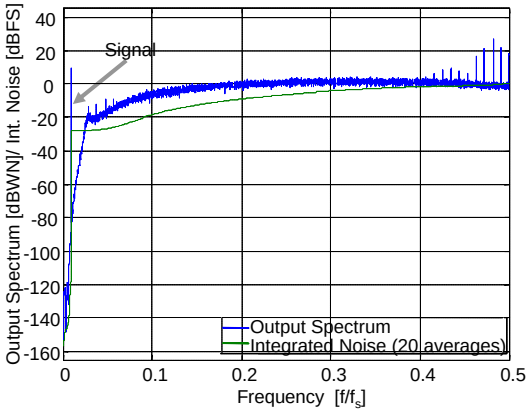


Rounded Filter Coefficients

```
a1=1;          k1=1;          b1=1/1024;
a2=1/2;        k2=1;          b2=1/16-1/64;
a3=1/4;        k3=1/2;
a4=1/8;        k4=1/4;
a5=1/8;        k5=1/8;        g =1;
```

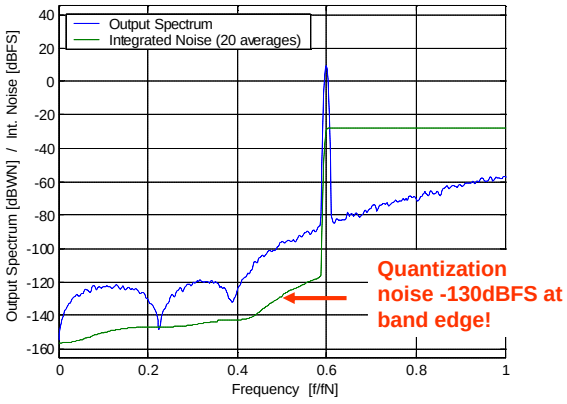
Ref: Nav Sooch, Don Kerth, Eric Swanson, and Tetsuro Sugimoto, “Phase Equalization System for a Digital-to-Analog Converter Using Separate Digital and Analog Sections”, U.S. Patent 5061925, 1990, figure 3 and table 1.

5th Order Noise Shaping



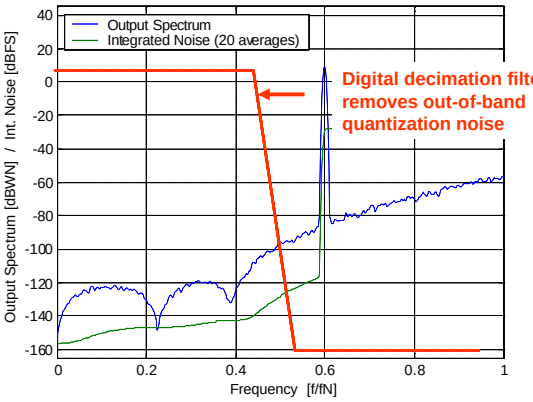
- Mostly quantization noise, except at low frequencies
- Let's zoom into the baseband portion…

5th Order Noise Shaping



sigma_delta_L5.m

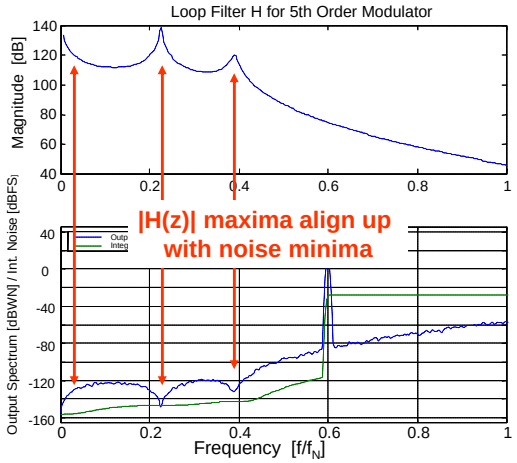
5th Order Noise Shaping



sigma_delta_L5.m

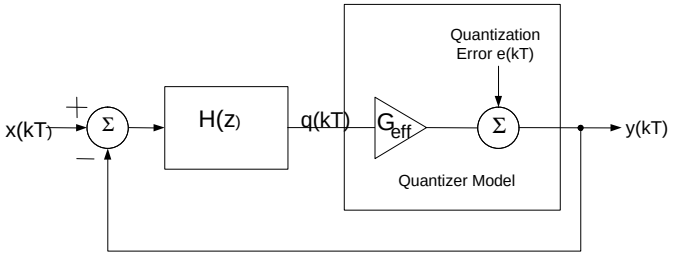
- SQNR > 120dB
- Sigma-delta modulators are usually designed for negligible quantization noise
- Other error sources dominate, e.g. thermal noise

In-Band Noise Shaping



- Lot's of gain in the pass-band
- Remember that
  - NTF ~ 1/H
  - STF=H/(1+H)

Stability Analysis

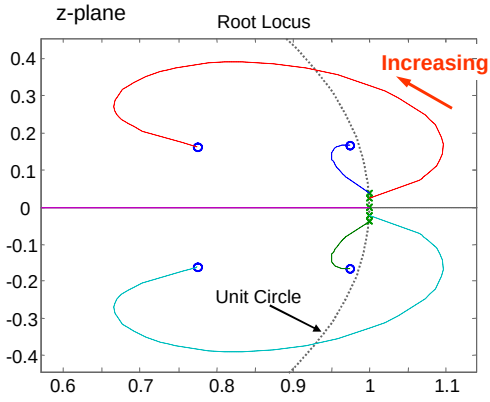


- Approach: linearize quantizer and use linear system theory!
- Effective quantizer gain

$$G_{eff}^2 = \overline{y^2} / \overline{q^2}$$

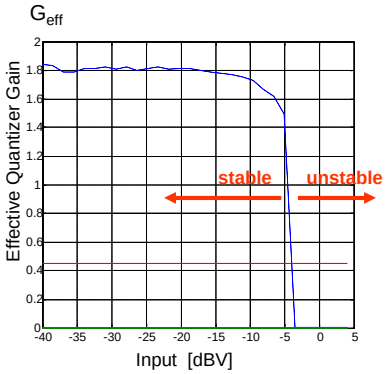
- Obtain G_{eff} from simulation

Modulator Root-Locus



- As G_{eff} increases, poles of STF move from
  - poles of H(z) (G_{eff} = 0) to
  - zeros of H(z) (G_{eff} = ∞)
- Pole-locations inside unit-circle correspond to stable STF and NTF
- G_{eff} > 0.45 for stability

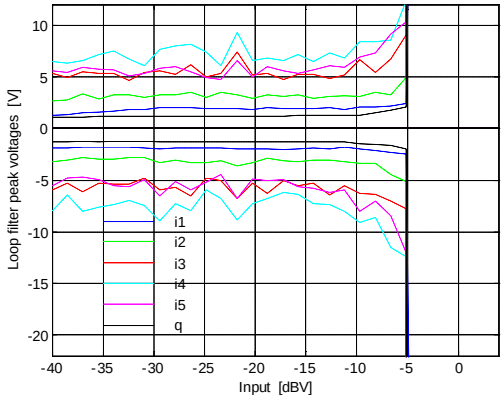
Effective Quantizer Gain, G_{eff}



- Large inputs → comparator input grows
- Output is fixed (±1)
  - → G_{eff} drops
  - → modulator unstable for large inputs

- Solution:
  - Limit input amplitude
  - Detect instability (long sequence of +1 or -1) and reset integrators
  - Beware of "worst-case inputs" (e.g. square waves near high-Q poles – attenuate with anti-aliasing filter)
  - Note that signals grow slowly for nearly stable systems → use long simulations

Loop Voltages



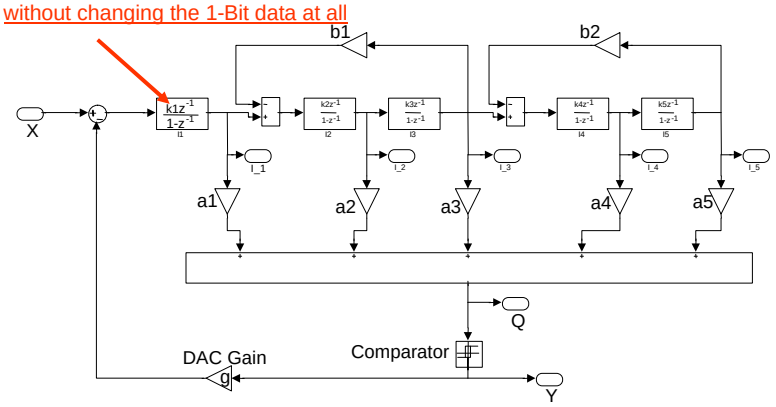
- Internal signal amplitudes are weak function of input level (except near overload)
- Exceed supply voltage
- Solutions:
  - Reduce V_{ref} ??
  - Scaling

Loop Voltage Scaling

- If we scale k_1 by 0.1,
  - All state variables and Q scale by 0.1
  - But since the comparator output is fixed and input is decreased by 10, G increases 10X
- The change in k_1 doesn't change the shape of the root locus, either
  - The effective gain for each root position is increased 10X
  - G > 4 is now required for stability

5th Order Modulator – Scaling

Only the sign of Q matters,
so we can make k_1 whatever we want
without changing the 1-Bit data at all

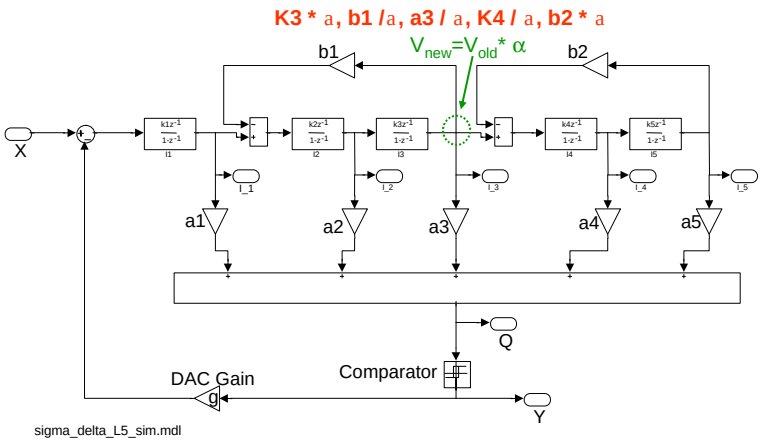


Loop Voltage Scaling (cont.)

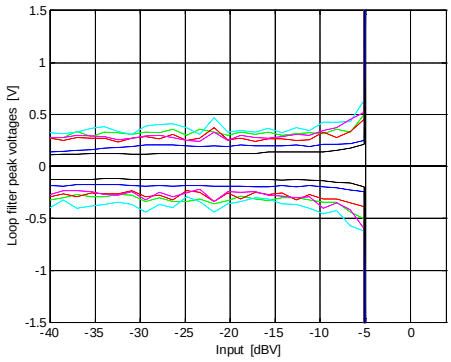
- Note that ∫3, ∫4, and ∫5 have substantially larger swings than ∫1 and ∫2
- Just about any filter topology allows node scaling which change internal state variable amplitudes without changing the filter output
  - The next slide shows an example

Node Scaling Example:

3rd Integrator Output Voltage Scaled by α



Voltage Scaling



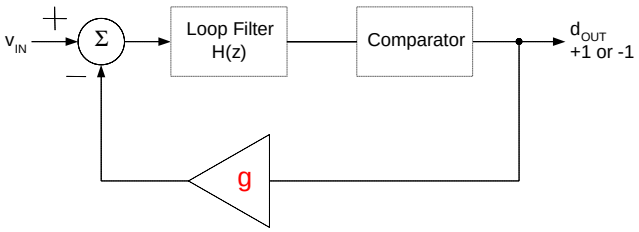
k1=1/10;
k2=1;
k3=1/4;
k4=1/4;
k5=1/8;
a1= 1;
a2=1/2;
a3=1/2;
a4=1/4;
a5=1/4;
b1=1/512;
b2=1/16-1/64;
g =1;

- Integrator output range is fine now
- But: maximum input signal limited to -5dB (-7dB with safety) – fix?

Input Range Scaling

Increasing the DAC levels by g reduces the analog to digital conversion gain:

$$\frac{D_{OUT}(z)}{V_{IN}(z)} = \frac{H(z)}{1+gH(z)} \cong \frac{1}{g}$$

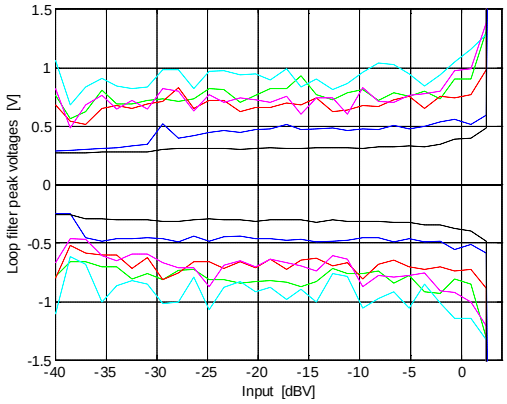


Increasing v_{IN} & g by the same factor leaves 1-Bit data unchanged

Input Range Scaling

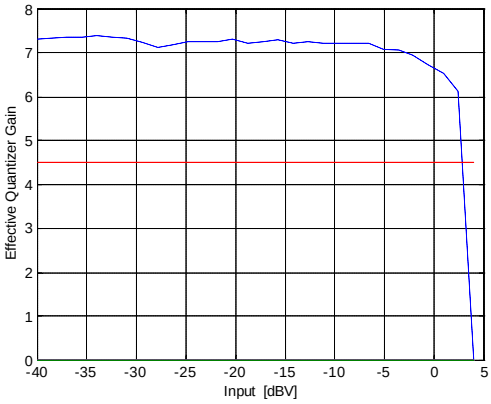
- Scaling the DAC output levels adjusts the modulator input range
  - If V_{IN} and the DAC outputs are scaled up by the same factor g, the 1-Bit data is completely unchanged
  - Of course, increasing the range also increases the quantization noise … the dynamic range and peak SQNR stay the same!
  - If the DAC output levels are increased and the analog full scale is held constant, the stability margin improves … at the expense of reduced SQNR

Scaled Stage 1 Model



g = 2.5;

Scaled Stage 1 Model

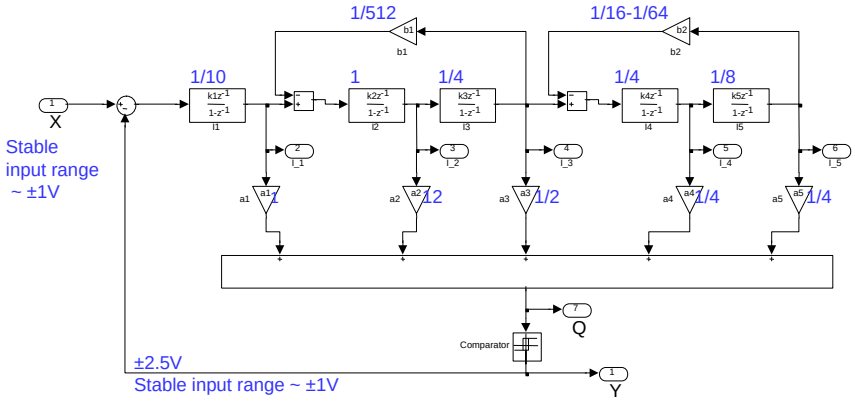


2dB safety margin for stability

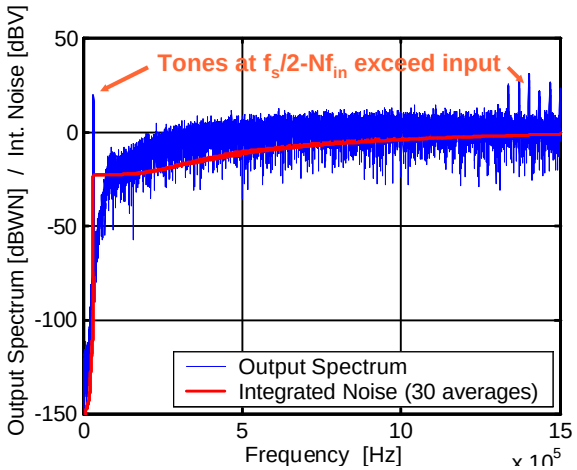
Summary

- Stage 1 model verified –
  stable and meets SQNR specification
- Stage 2 issues in 5th order $\Sigma\Delta$ modulator
  - DC inputs
  - Tones
  - Dither
  - kT/C noise

5th Order Modulator

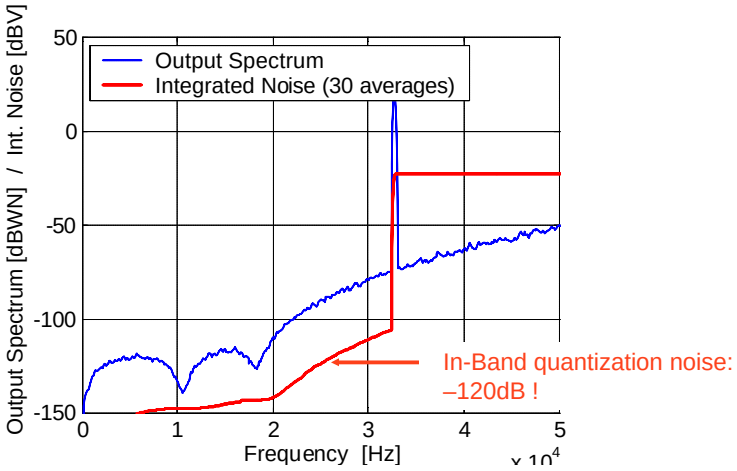


5th Order Noise Shaping

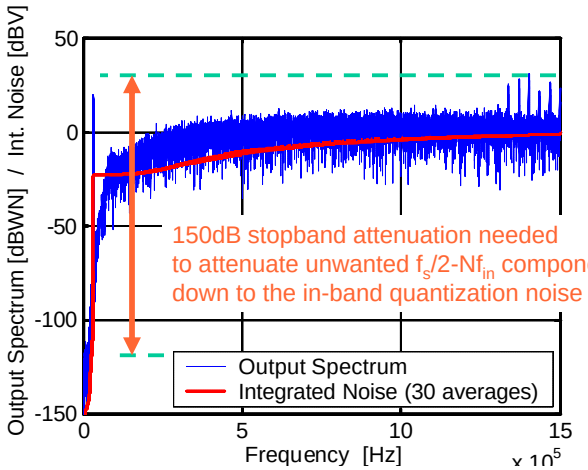


Input: 0.1V, sinusoid
2^{15} point DFT
30 averages

In-Band Noise



5th Order Noise Shaping

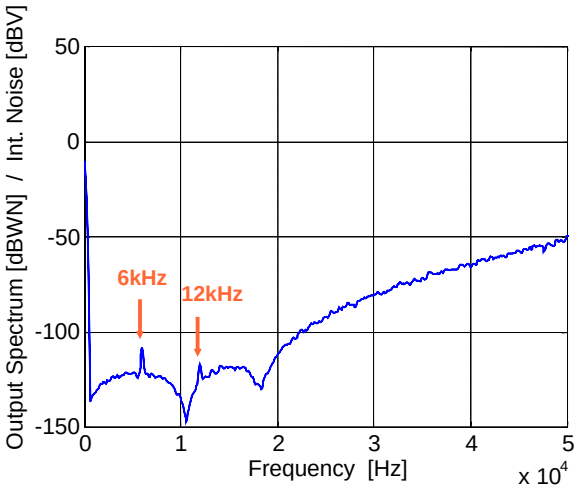


Input: 0.1V, sinusoid
2^{15} point DFT
30 averages

Out-of-Band vs In-Band Signals

- A digital (low-pass) filter with suitable coefficient precision can eliminate out-of-band quantization noise
- No filter can attenuate unwanted in-band components without attenuating the signal
- We'll spend some time making sure the components at $f_s/2-Nf_{in}$ will not "mix" down to the signal band
- But first, let's look at the modulator response to small DC inputs (or offset) …

ΣΔ Tones

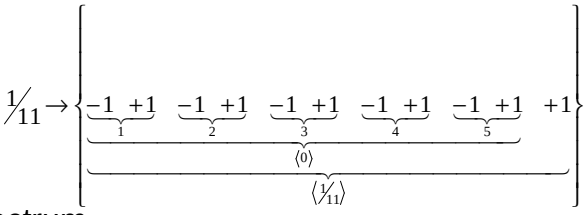


5mV DC input
(V_{DAC} → 2.5V)

Simulation technique:
A random 1st sample randomizes the noise from DC input and enables averaging. Otherwise the small tones are not visible.

Limit Cycles

- Representing a DC term with a –1/+1 pattern … e.g.



- Spectrum

$$\frac{f_s}{11} \quad 2\frac{f_s}{11} \quad 3\frac{f_s}{11} \quad \ldots$$

Limit Cycles

- Fundamental

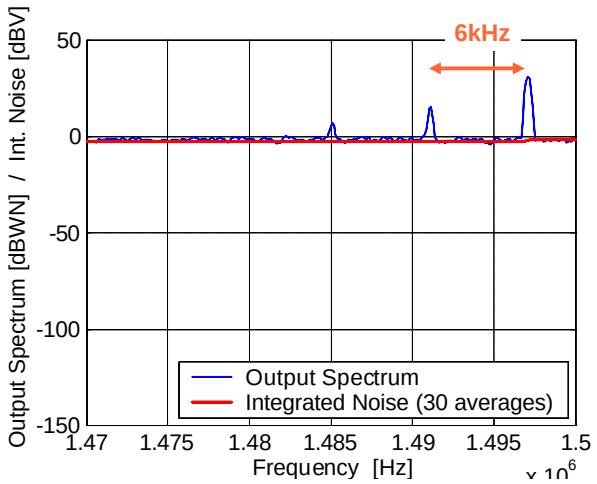
$$\begin{aligned} f_d &= f_s \frac{V_{DC}}{V_{DAC}} \\ &= 3MHz \frac{5mV}{2.5V} \\ &= \underline{6kHz} \end{aligned}$$

- Tone velocity (useful for debugging)

$$\frac{df_d}{dV_{DC}} = \frac{f_s}{V_{DAC}}$$

$$\frac{df_d}{dV_{DC}} = \underline{1.2kHz/mV}$$

ΣΔ Tones



ΣΔ Tones

- In-band tones look like signals
- Can be a big problem in some applications
  - E.g. audio → even tones with power below the quantization noise floor can be audible
- Tones near $f_s/2$ can be aliased down into the signal band
  - Since they are often strong, even a small alias can be a big problem
  - We will look at mechanisms that alias tones later
- First let's look at dither as a means to reduce or eliminate in-band tones

Dither

- DC inputs can of course be represented by many possible bit patterns
- Including some that are random but still average to the DC input
- The spectrum of such a sequence has no tones
- How can we get a ΣΔ modulator to produce such "randomized" sequences?

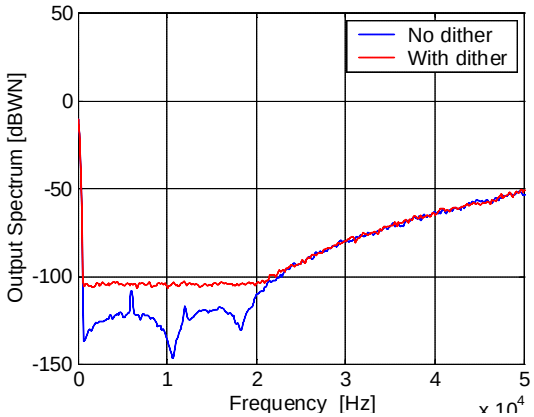
Dither

- The target DR for our audio ΣΔ is 16 Bits, or 98dB
- Let's choose the sampling capacitor such that it limits the dynamic range:

$$DR = \frac{\frac{1}{2}(V_{FS})^2}{\sqrt{\overline{v_n^2}}} \qquad V_{FS} = 1Vp$$

$$\rightarrow \qquad \sqrt{\overline{v_n^2}} = \sqrt{\frac{1}{2DR}}(V_{FS}) = \underline{9\mu V}$$

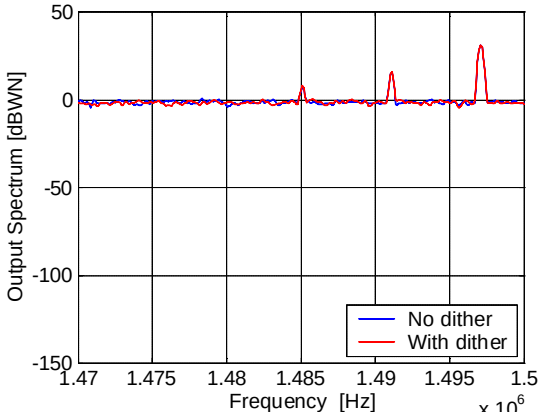
Dither



2mV DC input

- Tones disappear
- Note: they are not just buried
- How can we tell?

Dither

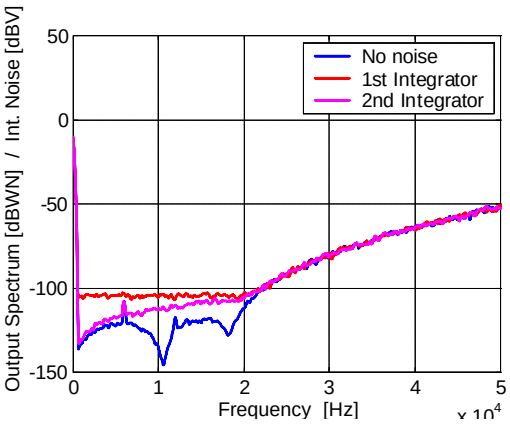


Dither at an amplitude which buries the in-band tones has virtually no effect on tones near $f_s/2$

kT/C Noise

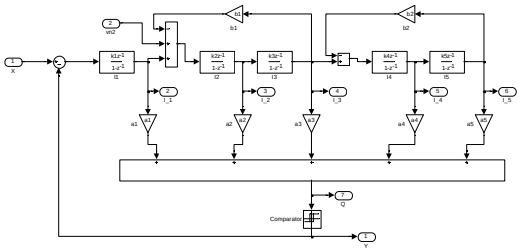
- So far we've looked at noise added to the input of the ΣΔ modulator, which is also the input of the first integrator
- Now let's add noise also to the input of the second integrator
- Let's assume a 1/12 sampling capacitor for the 2nd integrator wrt the 1st integrator
  - This gives 32μV rms noise

kT/C Noise



- 5mV DC input
- Noise from 2nd integrator
  - smaller than 1st integrator noise
  - shaped
- Why?

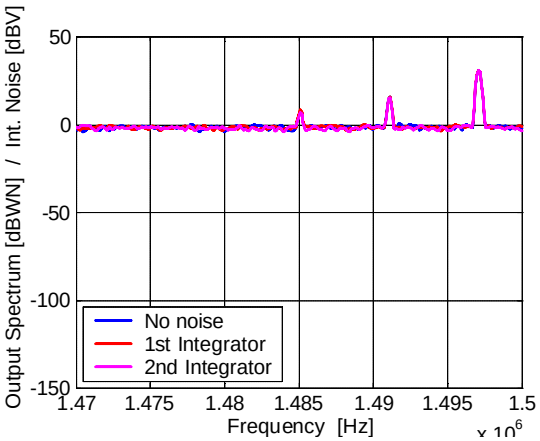
kT/C Noise



- Noise from 1st integrator is added directly to the input
- Noise from 2nd integrator is first-order noise shaped
- Noise from subsequent integrators is attenuated even further

→ Especially for high oversampling ratios, only the first 1 or 2 integrators add significant thermal noise. This is true also for other imperfections.

Dither



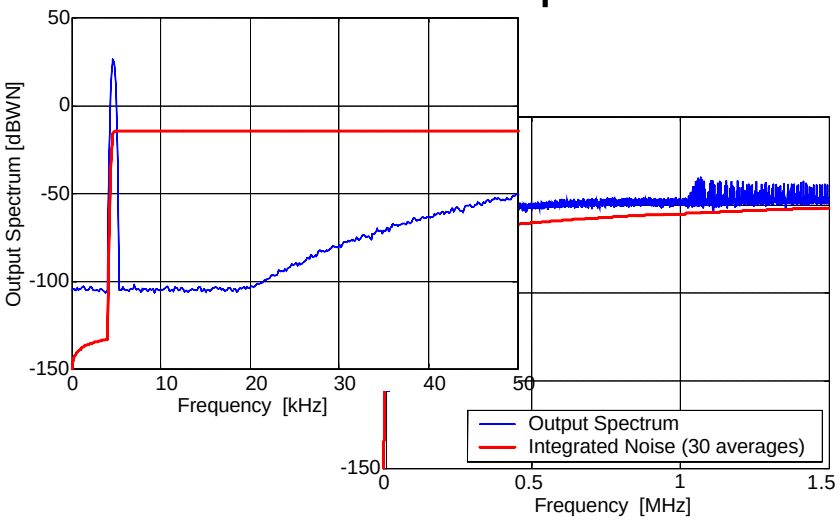
No practical amount of dither eliminates the tones near $f_s/2$

Full-Scale Inputs

- With practical levels of thermal noise added, let's try a 5kHz sinusoidal input near full-scale

- No distortion is visible in the spectrum
  - 1-Bit modulators are intrinsically linear
  - But tones exist at high frequencies
    - → to the oversampled modulator, a sinusoidal input looks like two "slowly" alternating DCs … hence giving rise to limit cycles

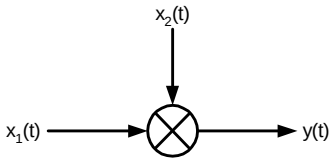
Full-Scale Inputs



V_{ref} Interference

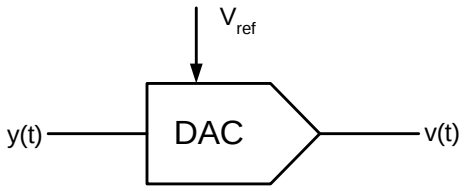
- Dither successfully removes in-band tones that would corrupt the signal
- The high-frequency tones in the quantization noise spectrum will be removed by the digital filter following the modulator
- What if some of these strong tones are demodulated to the base-band before digital filtering?
- Why would this happen?

AM Modulation



$$x_1(t) = X_1 \cos(w_1 t)$$
$$x_2(t) = X_2 \cos(w_2 t)$$
$$x_1(t) \times x_2(t) = \frac{X_1 X_2}{2}\left[\cos(w_1 t + w_2 t) + \cos(w_1 t - w_2 t)\right]$$

AM Modulation in DAC

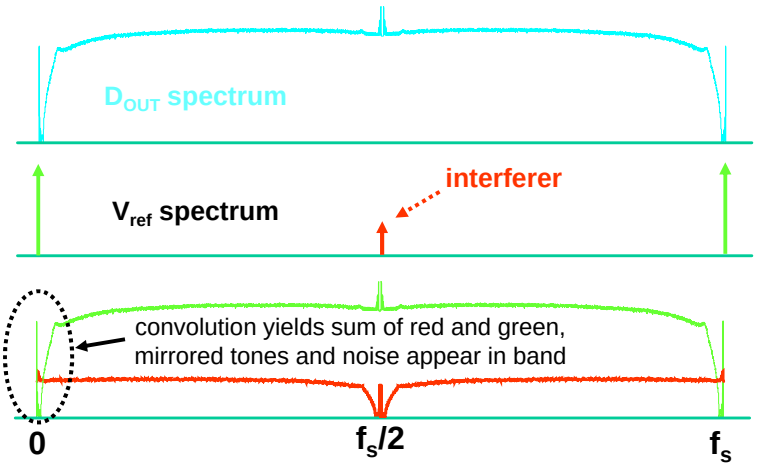


$y(t) = D_{out} = \pm 1$

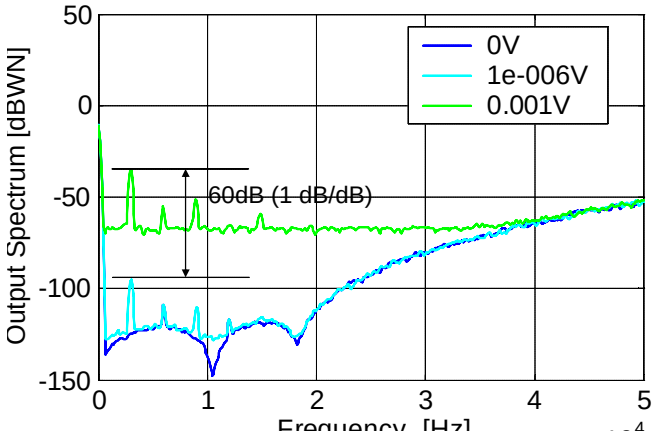
$V_{ref} = 2.5V + 1mV \quad f_s/2 \ square \ wave$

$v(t) = y(t) \times V_{ref}$

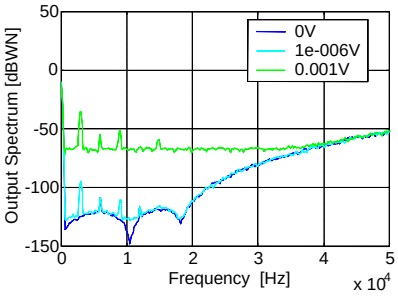
AM Modulation in DAC

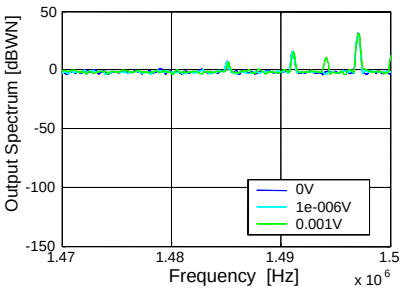


V_{ref} Interference



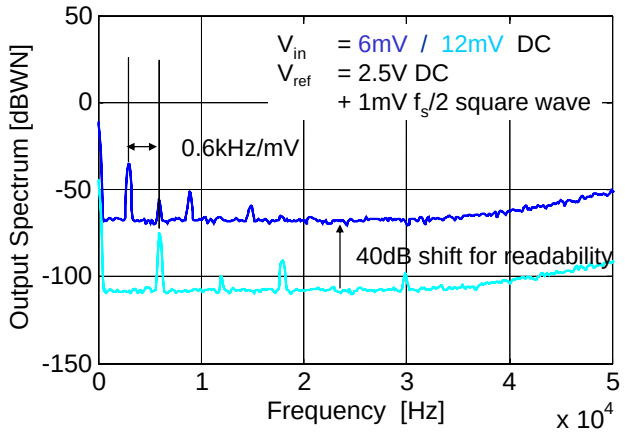
V_{ref} Interference





Symmetry of the spectra at $f_s/2$ and DC confirm that this is AM modulation

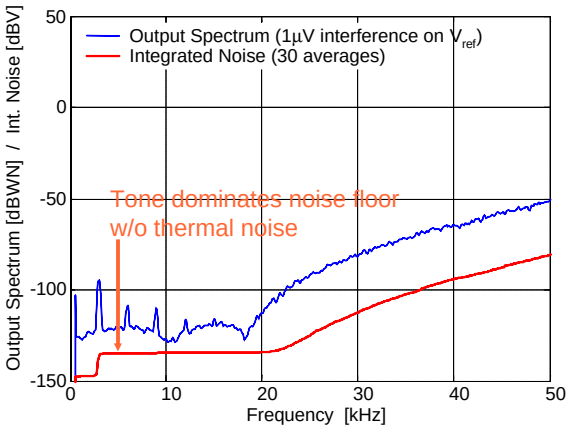
V_{ref} Tone Velocity



V_{ref} Interference

- Simulations are for specified amounts of $f_s/2$ interference in the DAC reference
- Interference demodulates the high-frequency tones
- Since the high frequency tones are strong, a small amount (1µV) of interference suffices to create huge base-band tones
- Stronger interference (1mV) raises the noise floor also
- Amplitude of demodulated tones is proportional to interference
- The velocity of AM demodulated tones is half that of the native tone
- Such differences help debugging of real silicon
- How clean does the reference have to be?

V_{ref} Interference



Summary

- Our stage 2 model can drive almost all capacitor sizing decisions
  - Gain scaling
  - kT/C noise
  - Dither
- Dither removes effectively in-band tones
  - Actual tonality determined by demodulation of limit cycles near $f_s/2$
- Extremely high clock-to-V_{ref} isolation is required for digital audio applications
- Next we will add relevant component imperfections, e.g.
  - Real capacitors aren't perfect
  - Real opamps aren't ideal

  → Effect of component nonlinearities on ΣΔ performance