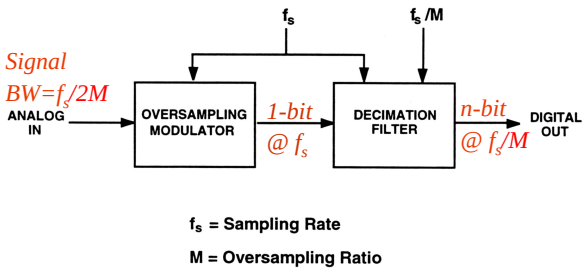
EE247
Lecture 23

- Oversampled ADCs
  - 1-Bit quantization
    - Quantization error spectrum
    - SQNR analysis
    - Limit cycle oscillations
  - 2nd order ΣΔ modulator
    - Dynamic range
    - Practical implementation
      - Effect of various nonidealities on the ΣΔ performance

Oversampled ADCs
Last Lecture

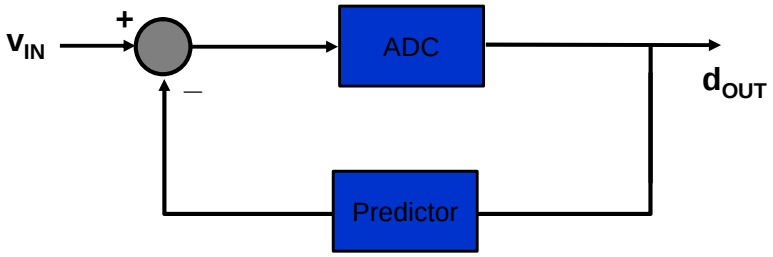
- Why Oversampling?
  - Allows trading speed for resolution
  - Relaxed transition band requirements for analog anti-aliasing filters
  - Reduced baseband quantization noise power
  - Utilizes low cost, low power digital filtering
  - Issue of limit cycle oscillation (spurious inband tones)
- By simply increasing oversampling ratio: 2X increase in sampling ratio → 0.5-bit increase in resolution
- To achieve greater improvement in resolution:
  - Embed quantizer in a feedback loop
    - → Predictive (delta modulation)
    - → Noise shaping (sigma delta modulation)

Oversampling A/D Conversion



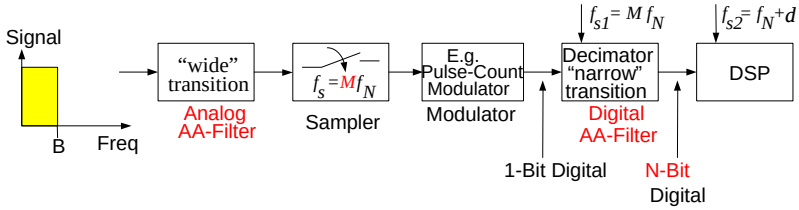
- Analog front-end → oversampled noise-shaping modulator
  - •Converts original signal to a 1-bit digital output at the high rate of ($2MX\ f_{signal}$)
- Digital back-end → digital filter
  - •Removes out-of-band quantization noise
  - •Provides anti-aliasing to allow re-sampling @ lower sampling rate

Oversampled ADC Predictive Coding



- Quantize the difference signal rather than the signal itself
- Smaller input to ADC → Buy dynamic range
- Only works if combined with oversampling
- 1-Bit digital output
- Digital filter computes "average" →n-Bit output

Oversampled ADC



Decimator:

- Digital (low-pass) filter
- Removes quantization error for f > B
- Provides most anti-alias filtering
- Narrow transition band, high-order
- 1-Bit input, N-Bit output (essentially computes "average")

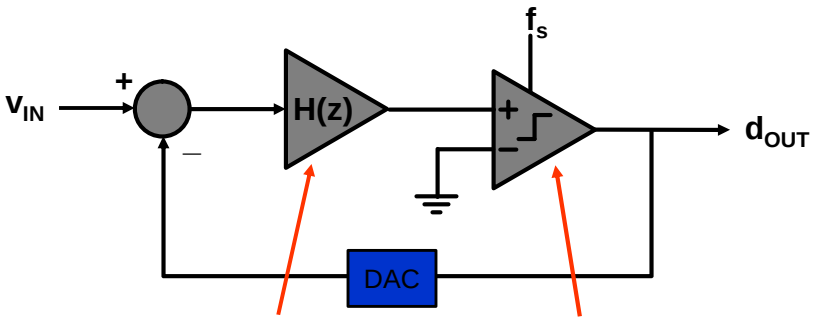
Modulator

- Objectives:
  - Convert analog input to 1-Bit pulse density stream
  - Move quantization error to high frequencies f >>B
  - Operates at high frequency $f_s >> f_N$
    - M = 8 … 256 (typical)….1024
    - Better be "simple"

→ ΣΔ = ΔΣ Modulator

Sigma- Delta Modulators

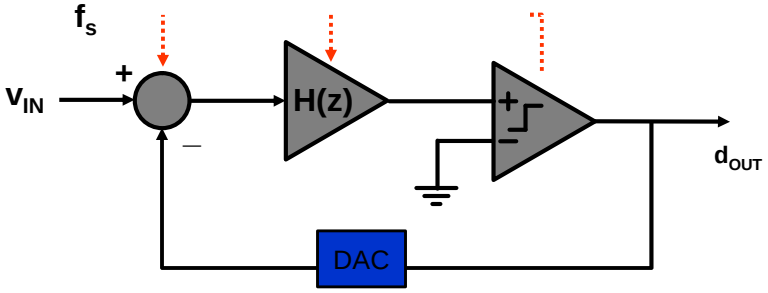
Analog 1-Bit ΣΔ modulators convert a continuous time analog input v_{IN} into a 1-Bit sequence d_{OUT}



Loop filter **1b Quantizer (a comparator)**

Sigma-Delta Modulators

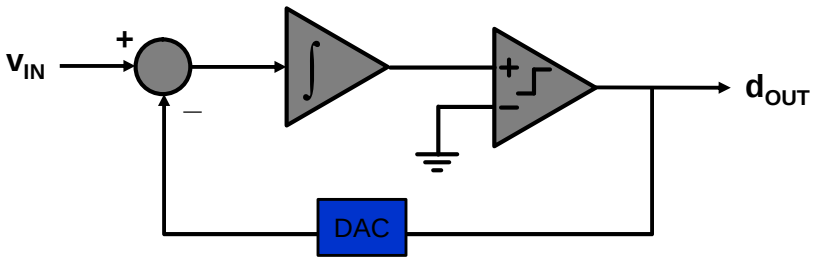
- The loop filter H can be either a switched-capacitor or continuous time
- Switched-capacitor filters are “easier” to implement and scale with the clock rate
- Continuous time filters provide anti-aliasing protection
- Can be realized with passive LC’s at very high frequencies



1st Order ΣΔ Modulator

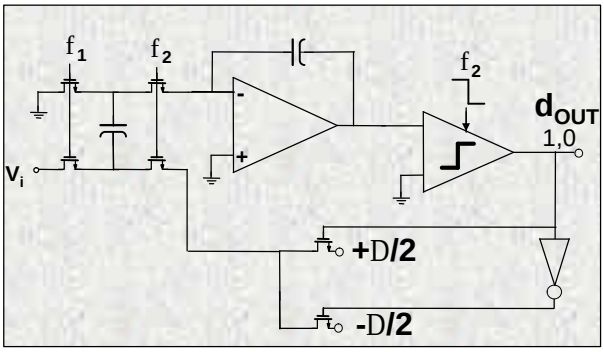
In a 1st order modulator, simplest loop filter → an integrator

$$H(z) = \frac{z^{-1}}{1 - z^{-1}}$$

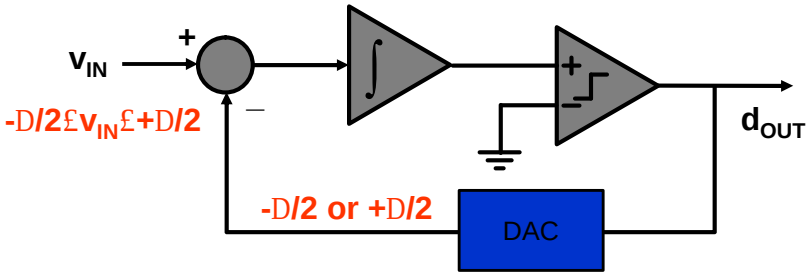


1st Order ΣΔ Modulator

Switched-capacitor implementation

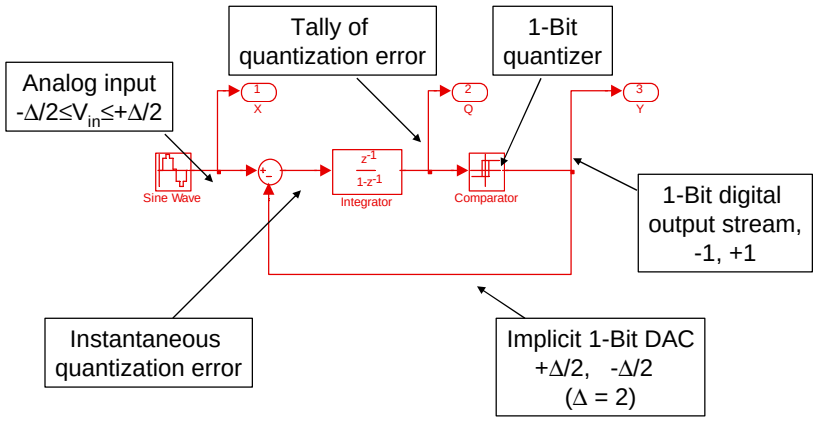


1st Order ΔΣ Modulator

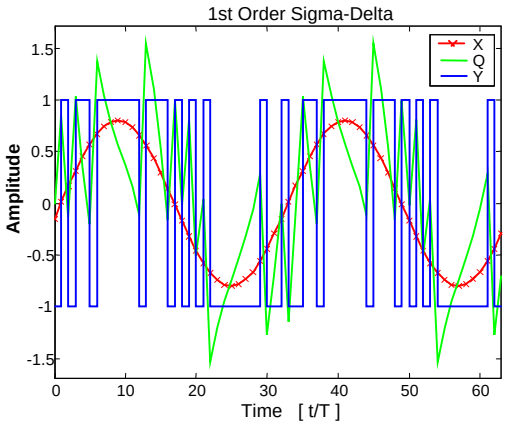


- Properties of the first-order modulator:
  - Analog input range is equal to the DAC reference
  - The average value of d_{OUT} must equal the average value of v_{IN}
  - +1's (or –1's) density in d_{OUT} is an inherently monotonic function of v_{IN}
    → linearity is not dependent on component matching
  - Alternative multi-bit DAC (and ADCs) solutions reduce the quantization error but loose this inherent monotonicity

1st Order ΣΔ Modulator



1st Order Modulator Signals



X analog input
Q tally of q-error
Y digital/DAC output

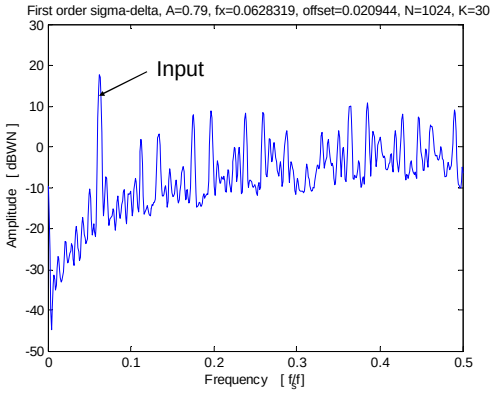
Mean of Y approximates X

$T = 1/f_s = 1/ (M f_N)$

ΣΔ Modulator Characteristics

- Quantization noise and thermal noise (KT/C) distributed over –fs/2 to +fs/2
  → Total noise reduced by 1/M
- Very high SQNR achievable (> 20 Bits!)
- Inherently linear for 1-Bit DAC
- Quantization error independent of component matching
- Limited to moderate to low speed

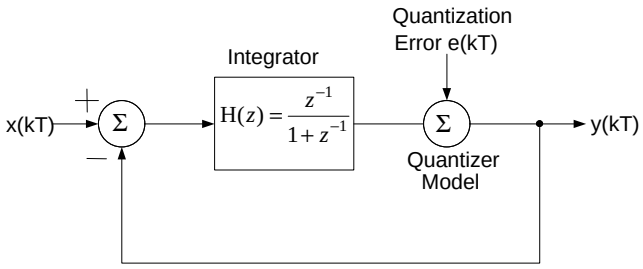
Output Spectrum



- Definitely not white!
- Skewed towards higher frequencies
- Tones
- dBWN (dB White Noise) scale sets the 0dB line at the noise per bin of a random -1, +1 sequence

sigma_delta_L1_sin.m

Quantization Noise Analysis

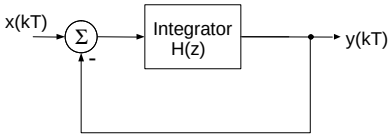


- Sigma-Delta modulators are nonlinear systems with memory → very difficult to analyze directly
- Representing the quantizer as an additive noise source linearizes the system

Signal Transfer Function

$$H(z) = \frac{z^{-1}}{1 + z^{-1}}$$

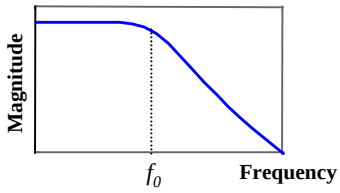
$$H(jw) = \frac{w_0}{jw}$$



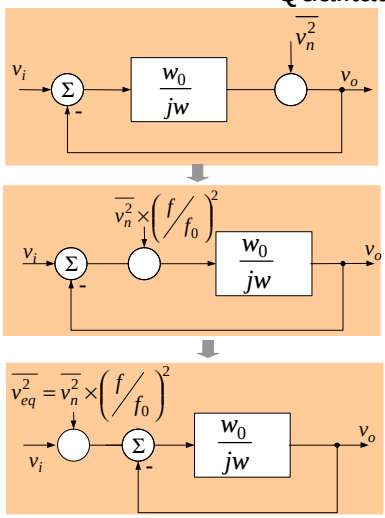
Signal transfer function
→ low pass function:

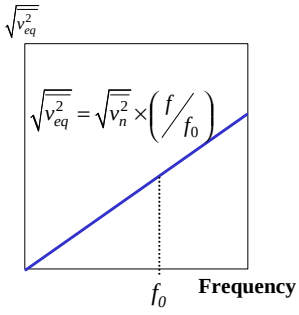
$$H_{Sig}(jw) = \frac{1}{1 + \frac{s}{w_0}}$$

$$H_{Sig}(z) = \frac{Y(z)}{X(z)} = \frac{H(z)}{1 + H(z)} = z^{-1} \quad \Rightarrow \quad \text{Delay}$$

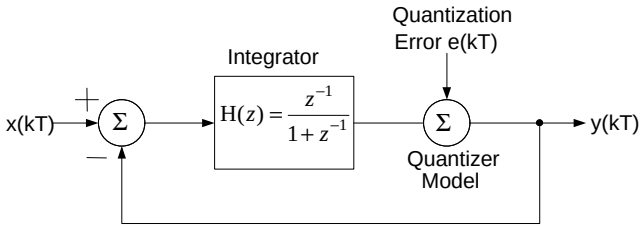


Noise Transfer Function
Qualitative Analysis





STF and NTF



Signal transfer function:

$$\text{STF} = \frac{Y(z)}{X(z)} = \frac{H(z)}{1+H(z)} = z^{-1} \quad \Rightarrow \quad \text{Delay}$$

Noise transfer function:

$$\text{NTF} = \frac{Y(z)}{E(z)} = \frac{1}{1+H(z)} = 1 - z^{-1} \quad \Rightarrow \quad \text{Differentiator}$$

Noise Transfer Function

$$NTF = \frac{Y(z)}{E(z)} = \frac{1}{1+H(z)} = 1 - z^{-1}$$

$$NTF(jw) = (1 - e^{-jwT}) = 2e^{-jwT/2}\left(\frac{e^{jwT/2} - e^{-jwT/2}}{2}\right)$$

$$= 2e^{-jwT/2} j \sin(wT/2)$$

$$= 2e^{-jwT/2} \times e^{-jp/2}\left[\sin(wT/2)\right]$$

$$= \left[2\sin(wT/2)\right]e^{-j(wT-p)/2}$$

where $T = 1/f_s$

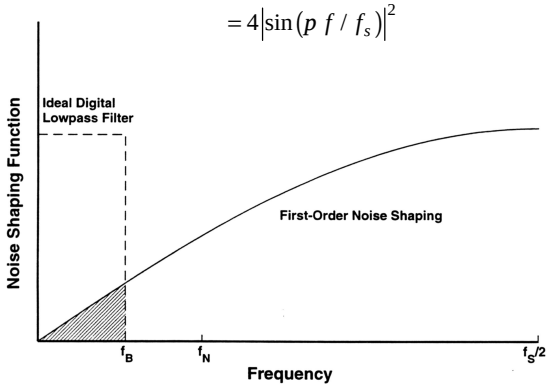
Thus:

$$|NTF(f)| = 2|\sin(wT/2)| = 2|\sin(p\, f/f_s)|$$

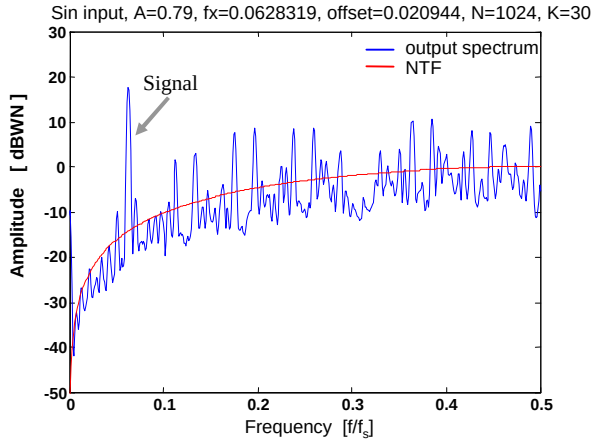
$$N_y(f) = |NTF(f)|^2 N_e(f)$$

First Order ΣΔ Modulator
Noise Transfer Characteristics

$$N_y(f) = |NTF(f)|^2 \, N_e(f)$$
$$= 4\left|\sin(p\, f / f_s)\right|^2$$



First Order ΣΔ Modulator
Simulated Noise Transfer Characteristic



Quantizer Error

- For quantizers with many bits

$$\overline{e^2(kT)} = \frac{\Delta^2}{12}$$

- Let's use the same expression for the 1-Bit case
- **Only simulation can tell if the result is useful**

  Experience: Often sufficiently accurate to be useful, with enough exceptions to be very careful

In-Band Quantization Noise

$$H(z) = \frac{z^{-1}}{1 - z^{-1}}$$

$$NTF(z) = 1 - z^{-1}$$

$$\left|NTF(f)\right|^2 = 4\left|\sin(\pi f / f_s)\right|^2 \quad \text{for} \quad M >> 1$$

$$\overline{S_Y} = \int_{-B}^{B} S_Q(f)\left|NTF(z)\right|^2_{z=e^{2\pi jfT}}\, df$$

$$\cong \int_{-f_s/2M}^{f_s/2M} \frac{1}{f_s}\frac{\Delta^2}{12}(2\sin \pi fT)^2\, df$$

$$\approx \frac{\pi^2}{3}\frac{1}{M^3}\frac{\Delta^2}{12}$$

Dynamic Range

$$DR = 10\log\left[\frac{\text{peak signal power}}{\text{peak noise power}}\right] = 10\log\left[\frac{\overline{S_X}}{\overline{S_Y}}\right]$$

$$\overline{S_X} = \frac{1}{2}\left(\frac{\Delta}{2}\right)^2 \qquad \text{sinusoidal input,} \quad STF = 1$$

$$\overline{S_Y} = \frac{p^2}{3}\frac{1}{M^3}\frac{\Delta^2}{12}$$

$$\frac{\overline{S_X}}{\overline{S_Y}} = \frac{9}{2p^2}M^3$$

$$DR = 10\log\left[\frac{9}{2p^2}M^3\right] = 10\log\left[\frac{9}{2p^2}\right] + 30\log M$$

$$DR = -3.4dB + +30\log M$$

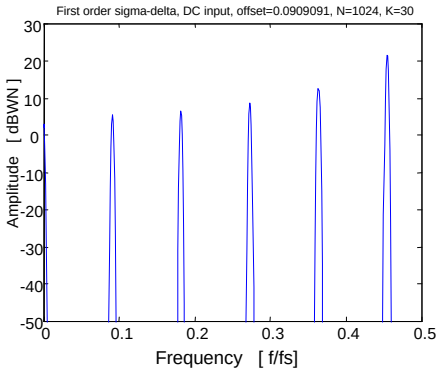
M	DR
16	33 dB
32	42 dB
1024	87 dB

2X increase in M➔9dB (1.5-bit) increase in DR

Oversampling and Noise Shaping

- ΣΔ modulators have interesting characteristics
  - Unity gain for input signal V_{IN}
  - Large attenuation of quantization noise injected at quatizer input
  - Performance significantly better than 1-Bit noise performance possible for frequencies << f_s
- Oversampling ($M = f_s/f_N > 1$) improves SQNR considerably
  - 1st-Order ΣΔ: DR increases 9dB for each doubling of M
  - SQNR independent of circuit complexity and accuracy
- Analysis assumes that the quantizer noise is "white"
  - Not true in practice, especially for low-order modulators
  - Practical modulators suffer from other noise sources also (e.g. thermal noise)

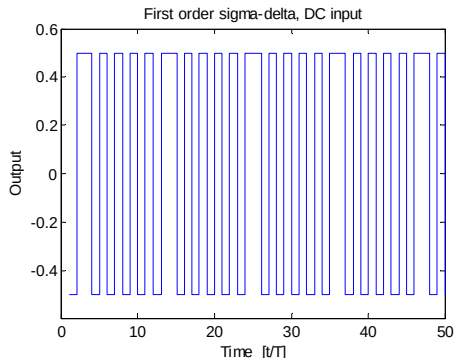
DC Input



- DC input A = 1/11
- Doesn't look like spectrum of DC at all
- Tones frequency shape the same as quantization noise
  → more prominent at higher frequencies

  → Quantization "noise" is periodic

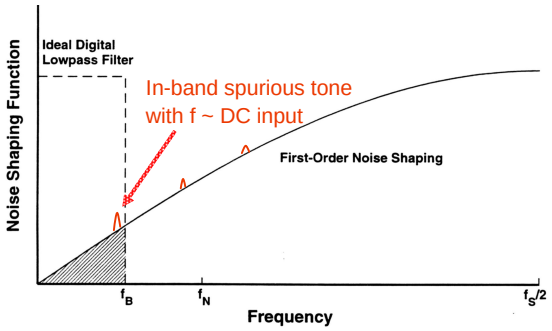
Limit Cycle



DC input 1/11 →
Periodic sequence:

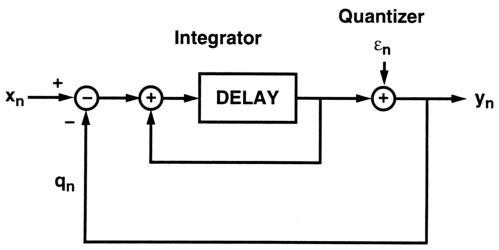
1	+1
2	+1
3	-1
4	+1
5	-1
6	+1
7	-1
8	+1
9	-1
10	+1
11	-1

Limit Cycle



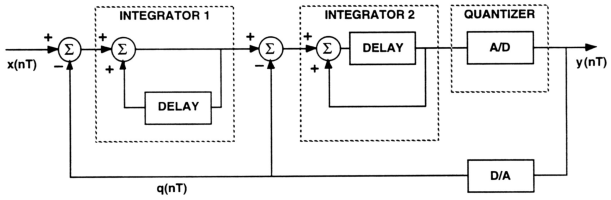
- Problem: quantization noise is periodic
- Solution:
  - Dither: randomizes quantization noise
    - thermal noise → dither
  - Second order loop

1st Order ΣΔ Modulator



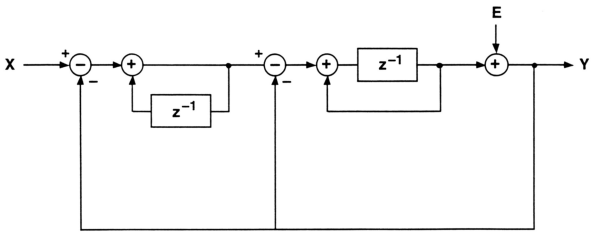
$$Y(z) = z^{-1}X(z) + \left(1 - z^{-1}\right)E(z)$$

2nd Order ΣΔ Modulator



- Two integrators
- 1st integrator non-delaying
- Feedback from output to both integrators
- Tones less prominent compared to 1st order

2nd Order ΣΔ Modulator



$$Y_n = X_{n-1} + \left(E_n - 2E_{n-1} + E_{n-2}\right)$$

$$Y(z) = z^{-1}X(z) + \left(1 - z^{-1}\right)^2 E(z)$$

2nd Order ΣΔ Modulator
In-Band Quantization Noise

$$H(z) = \frac{z^{-1}}{1 - z^{-1}}$$

$$G = 1$$

$$NTF(z) = \left(1 - z^{-1}\right)^2$$

$$\left|NTF(f)\right|^2 =$$

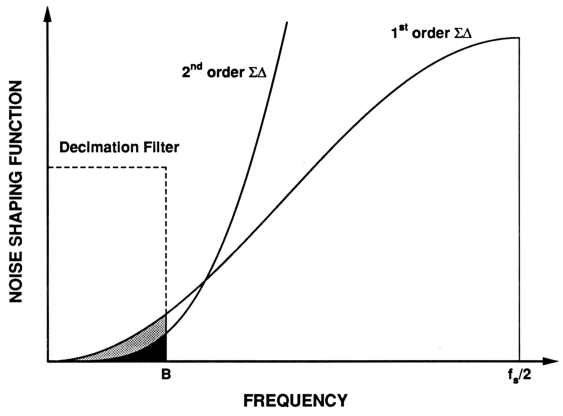
$$= 2^4 \left|\sin(p\, f / f_s)\right|^4 \quad \text{for} \quad M >> 1$$

$$\overline{S_Y} = \int_{-B}^{B} S_Q(f) \left|NTF(z)\right|^2_{z=e^{2p\,jfT}}\, df$$

$$\cong \int_{-f_s/2M}^{f_s/2M} \frac{1}{f_s} \frac{\Delta^2}{12} (2 \sin p\, fT)^4\, df$$

$$\approx \frac{p^4}{5} \frac{1}{M^5} \frac{\Delta^2}{12}$$

Quantization Noise
2nd Order ΣΔ Modulator



2nd Order ΣΔ Modulator Dynamic Range

$$DR = 10\log\left[\frac{\text{peak signal power}}{\text{peak noise power}}\right] = 10\log\left[\frac{\overline{S_X}}{\overline{S_Y}}\right]$$

$$\overline{S_X} = \frac{1}{2}\left(\frac{\Delta}{2}\right)^2 \qquad \text{sinusoidal input,} \quad STF = 1$$

$$\overline{S_Y} = \frac{p^4}{5}\frac{1}{M^5}\frac{\Delta^2}{12}$$

$$\frac{\overline{S_X}}{\overline{S_Y}} = \frac{15}{2p^4}M^5$$

$$DR = 10\log\left[\frac{15}{2p^4}M^5\right] = 10\log\left[\frac{15}{2p^4}\right] + 50\log M$$

$$DR = -11.1dB + +50\log M$$

M	DR
16	49 dB
32	64 dB
1024	139 dB

2X increase in M➔15dB (2.5-bit) increase in DR

2nd Order ΣΔ Modulator Example

- Digital audio application
  - Signal bandwidth 20kHz
  - Resolution 16-bit

$16-bit \rightarrow 98dB$ Dynamic Range

$$DR = -11.1dB + +50\log M$$

$$M_{\min} = 153$$

M➔256 to allow some margin
➔ Sampling rate (2x20kHz + 5kHz)M = 12MHz

Higher Order ΣΔ Modulator Dynamic Range

$$Y(z) = z^{-1}X(z) + \left(1 - z^{-1}\right)^{L} E(z) \quad , \quad \text{L} \rightarrow \Sigma\Delta \text{ order}$$

$$\overline{S_X} = \frac{1}{2}\left(\frac{\Delta}{2}\right)^2 \qquad \text{sinusoidal input,} \quad STF = 1$$

$$\overline{S_Y} = \frac{p^{2L}}{2L+1}\frac{1}{M^{2L+1}}\frac{\Delta^2}{12}$$

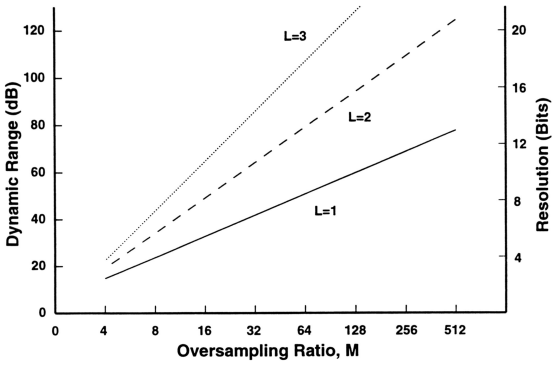
$$\frac{\overline{S_X}}{\overline{S_Y}} = \frac{3(2L+1)}{2p^{2L}}M^{2L+1}$$

$$DR = 10\log\left[\frac{3(2L+1)}{2p^{2L}}M^{2L+1}\right]$$

$$DR = 10\log\left[\frac{3(2L+1)}{2p^{2L}}\right] + (2L+1)\times 10\times \log M$$

2X increase in M➔(6L+3)dB or (L+0.5)-bit increase in DR

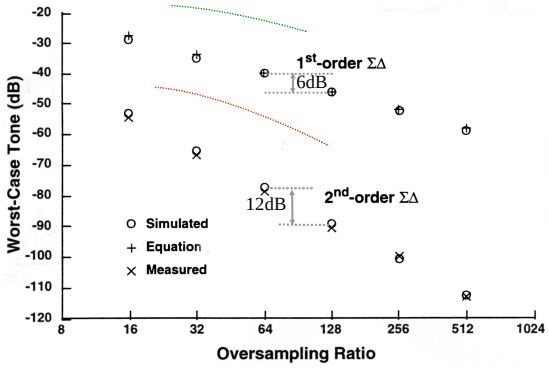
ΣΔ Modulator Dynamic Range As a Function of Modulator Order



- Stability issues for L>2

Tones in 1st Order & 2nd Order ΣΔ Modulator

- Higher oversampling ratio → lower tones
- 2nd order much lower tones compared to 1st
- 2X increase in M decreases the tones by 6dB for 1st order loop and 12dB for 2nd order loop

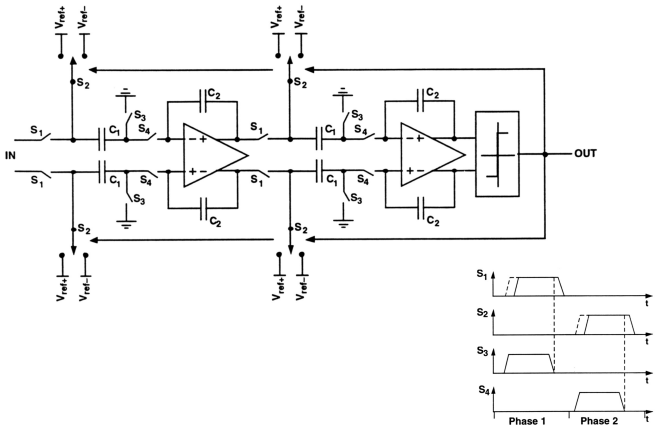


Ref:

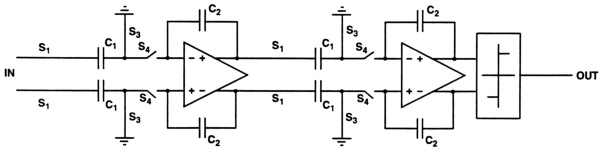
B. P. Brandt, D. E. Wingard, and B. A. Wooley, "Second-order sigma-delta modulation for digital-audio signal acquisition," IEEE Journal of Solid-State Circuits, vol. 26, pp. 618 - 627, April 1991.

R. Gray, "Spectral analysis of quantization noise in a single-loop sigma–delta modulator with dc input," *IEEE Trans. Commun.*, vol. 37, pp. 588–599, June 1989.

2nd Order ΣΔ Modulator Switched-Capacitor Implementation

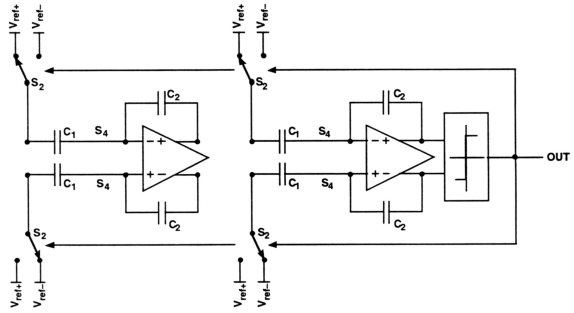


Switched-Capacitor Implementation 2nd Order ΣΔ
Phase 1



- Sample inputs
- Compare output of 2nd integrator
- At the end of phase1 S3 opens prior to S1

Switched-Capacitor Implementation 2nd Order ΣΔ
Phase 2

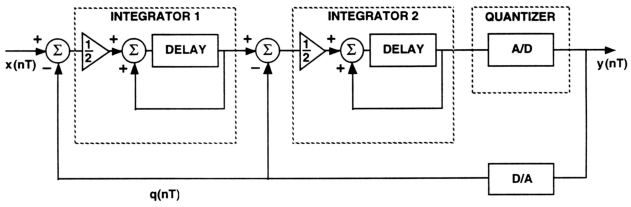


- Enable feedback
- Integrate
- Reset comparator
- At the end of phase2 S4 opens before S2

Practical Design Considerations for ΣΔ Implementation

- Internal nodes scaling & clipping
- Finite opamp gain & linearity
- Capacitor ratio errors
- KT/C noise
- Opamp noise
- Power dissipation considerations

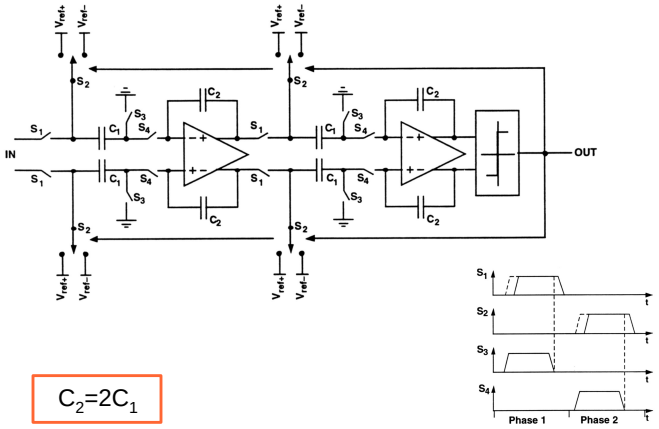
Switched-Capacitor Implementation 2nd Order ΣΔ Nodes Scaled for Maximum Dynamic Range



- Modification (gain of ½ in front of integrators) reduce & optimize required signal range at the integrator outputs ~ 1.7x input full-scale (Δ)

Ref: B.E. Boser and B.A. Wooley, "The Design of Sigma-Delta Modulation A/D Converters," IEEE J. Solid-State Circuits, vol. 23, no. 6, pp. 1298-1308, Dec. 1988.

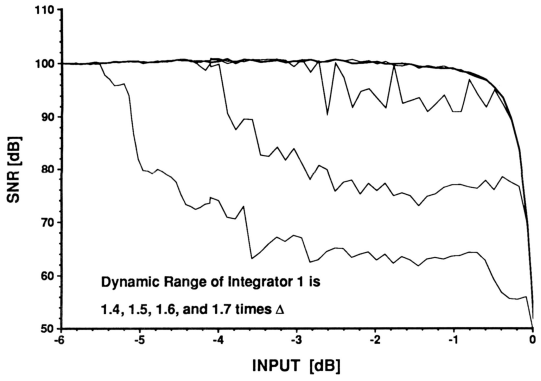
2nd Order ΣΔ Modulator
Switched-Capacitor Implementation



$C_2=2C_1$

2nd Order ΣΔ

Effect of Integrator Maximum Signal Handling Capability on SNR

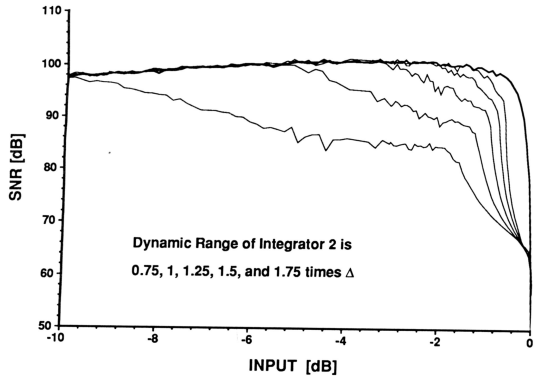


- Effect of 1st Integrator maximum signal handling capability on converter SNR

Ref: B.E. Boser and B.A. Wooley, "The Design of Sigma-Delta Modulation A/D Converters," IEEE J. Solid-State Circuits, vol. 23, no. 6, pp. 1298-1308, Dec. 1988.

2nd Order ΣΔ

Effect of Integrator Maximum Signal Handling Capability on SNR

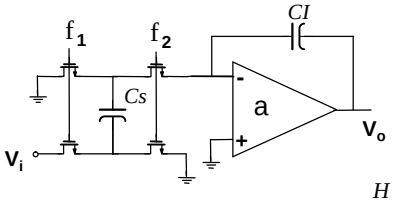


•Effect of 2nd Integrator maximum signal handling capability on SNR

Ref: B.E. Boser and B.A. Wooley, "The Design of Sigma-Delta Modulation A/D Converters," IEEE J. Solid-State Circuits, vol. 23, no. 6, pp. 1298-1308, Dec. 1988.

2nd Order ΣΔ

Effect of Integrator Finite DC Gain

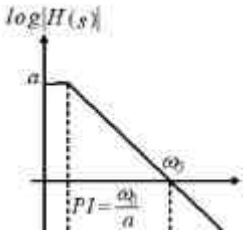


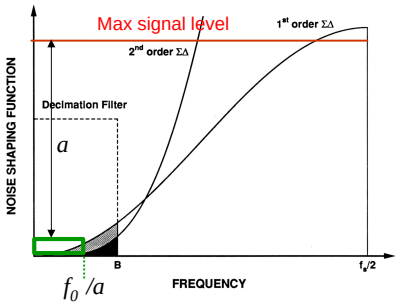
$$H(z)_{ideal} = \frac{Cs}{CI} \times \frac{z^{-1}}{1 - z^{-1}}$$

$$H(z)_{Finit\,DC\,Gain} = \frac{Cs}{CI} \times \frac{\left(\frac{a}{1 + a + \frac{Cs}{CI}}\right) z^{-1}}{1 - \left(\frac{1 + a}{1 + a + \frac{Cs}{CI}}\right) z^{-1}}$$

2nd Order ΣΔ

Effect of Integrator Finite DC Gain

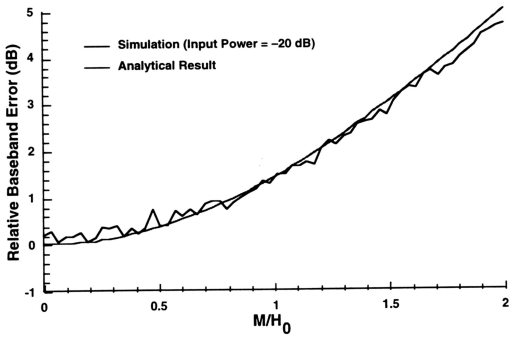




- Low integrator DC gain → degrades noise performance
- If a>M (oversampling ratio) → Insignificant degradation in SNR
- Normally DC gain designed to be >> M in order to suppress nonlinearities

2nd Order ΣΔ

Effect of Integrator Finite DC Gain

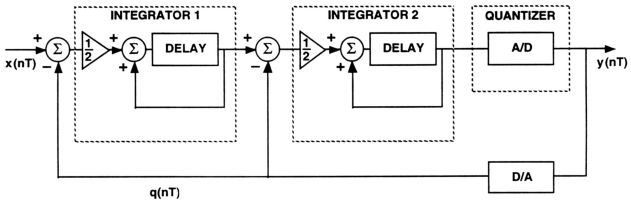


- Simulation results
- H_0=a → finite DC gain
- a> M → no degradation in SNR

Ref: B.E. Boser and B.A. Wooley, "The Design of Sigma-Delta Modulation A/D Converters," IEEE J. Solid-State Circuits, vol. 23, no. 6, pp. 1298-1308, Dec. 1988.

2nd Order ΣΔ

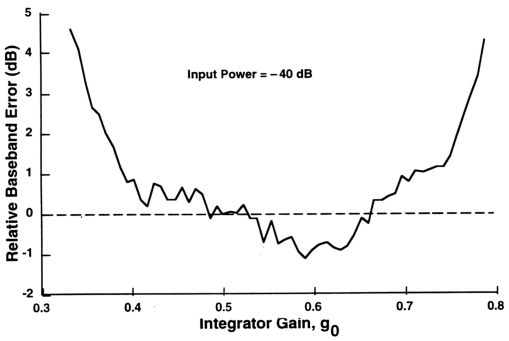
Effect of Integrator Overall Integrator Gain Inaccuracy



- Gain of ½ in front of integrators is a function of C1/C2 of the integrator
- The effect of C1/C2 inaccuracy inspected by simulation

2nd Order ΣΔ

Effect of Integrator Overall Gain Inaccuracy

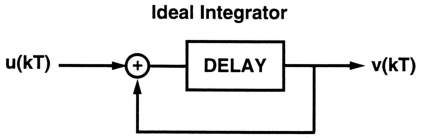


- Simulation show gain can vary by 20% w/o loss in performance
  → Confirms insensitivity of ΣΔ to component variations
- Note that for gain >0.65 system becomes unstable & SNR drops rapidly

Ref: B.E. Boser and B.A. Wooley, "The Design of Sigma-Delta Modulation A/D Converters," IEEE J. Solid-State Circuits, vol. 23, no. 6, pp. 1298-1308, Dec. 1988.

2nd Order ΣΔ

Effect of Integrator Nonlinearities



$$v(kT + T) = u(kT) + v(kT)$$

with nonlinearity

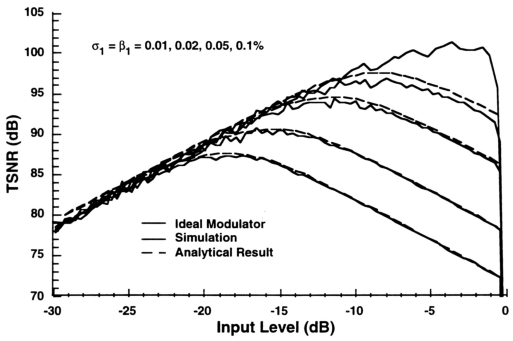
$$v(kT + T) = u(kT) + \alpha_1[u(kT)]^2 + \alpha_2[u(kT)]^3 + \ldots$$

$$+ v(kT) + \beta_1[v(kT)]^2 + \beta_2[v(kT)]^3 + \ldots$$

Ref: B.E. Boser and B.A. Wooley, "The Design of Sigma-Delta Modulation A/D Converters," IEEE J. Solid-State Circuits, vol. 23, no. 6, pp. 1298-1308, Dec. 1988.

2nd Order ΣΔ

Effect of Integrator Nonlinearities

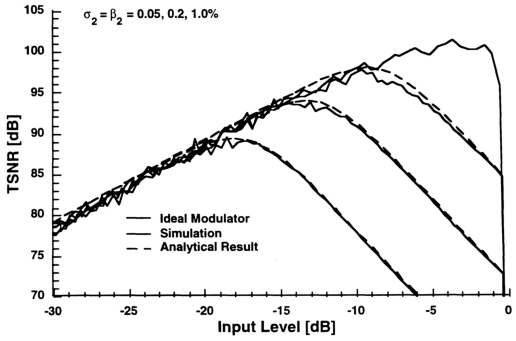


- Simulation for single-ended topology
- Even order nonlinearities can be significantly attenuated by using differential circuit topologies

Ref: B.E. Boser and B.A. Wooley, "The Design of Sigma-Delta Modulation A/D Converters," IEEE J. Solid-State Circuits, vol. 23, no. 6, pp. 1298-1308, Dec. 1988.

2nd Order ΣΔ

Effect of Integrator Nonlinearities

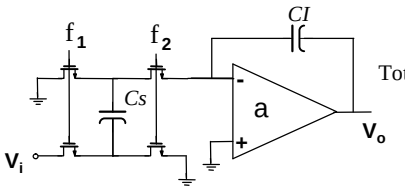


- Simulation for single-ended topology
- Odd order nonlinearities (3rd in this case)

Ref: B.E. Boser and B.A. Wooley, "The Design of Sigma-Delta Modulation A/D Converters," IEEE J. Solid-State Circuits, vol. 23, no. 6, pp. 1298-1308, Dec. 1988.

2nd Order ΣΔ

Effect of KT/C noise



$$\overline{v^2_n} = 2\frac{KT}{Cs}$$

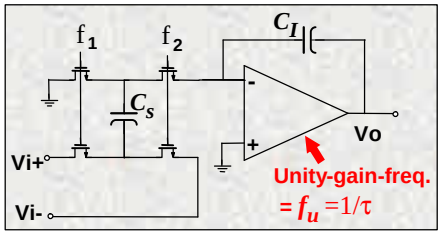
$$\overline{v^2_n}/f = 2\frac{kT}{Cs}\times\frac{1}{fs/2} = 4\frac{kT}{Cs\times fs}$$

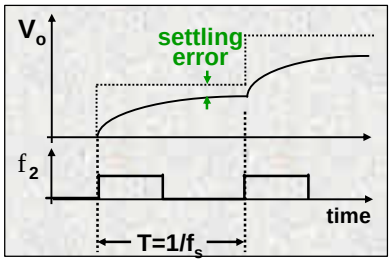
Total in-band noise:

$$\overline{v^2_{n\,input}} = 4\frac{kT}{Cs\times fs}\times f_0 = \frac{2kT}{Cs\times M}$$

- For the example of digital audio with 16-bit (100dB) & M=256
  - → Cs=1pF → 6μVrms noise
  - →If FS=4$V_{p\text{-}p\text{-}d}$ then noise is -107dB → almost no degradation in overall SNR
  - →Cs=1pF, CI=2pF → small cap area compared to Nyquist ADC caps
  - →Since thermal noise provides some level of dithering → better not choose much larger capacitors!

2nd Order ΣΔ
Effect of Finite Opamp Bandwidth



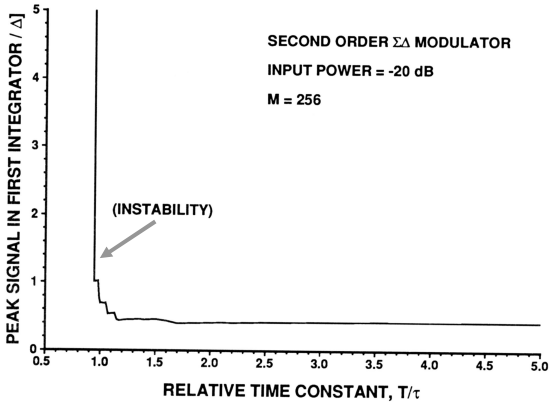


Assumption-

Opamp → does not slew

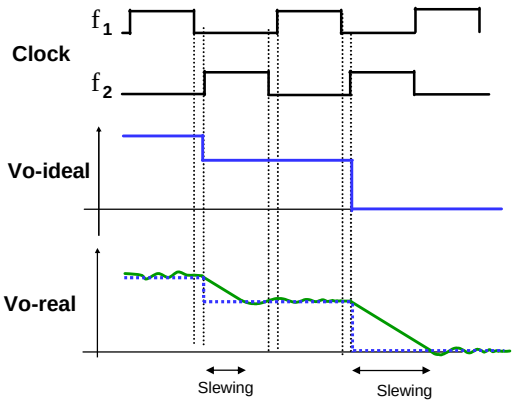
Opamp has only one pole → exponential settling

2nd Order ΣΔ
Effect of Finite Opamp Bandwidth

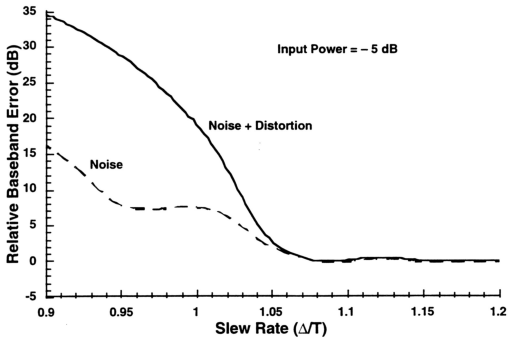


→ ΣΔ does not require high opamp bandwidth $f_u \sim 2f_s$ adequate

2nd Order ΣΔ
Effect of Slew Limited Settling



2nd Order ΣΔ
Effect of Slew Limited Settling



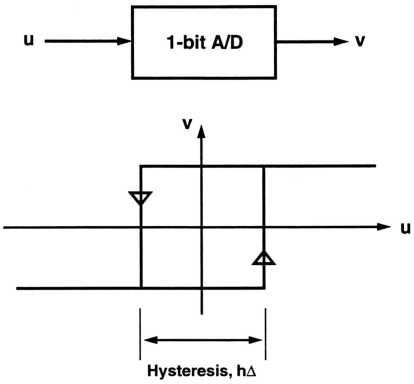
Assumption-

Opamp settling → slew limited

→Minimum slew rate of 1.2 (Δ x f_s) required

→Low slew rate degrade SNR rapidly

2nd Order ΣΔ
Comparator Hysteresis

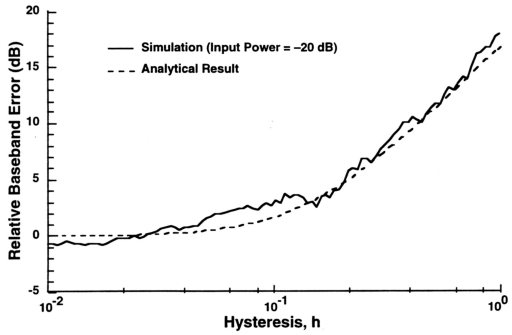


Assumption-

1-bit A/D → Comparator has hysteresis

Comparator offset similar effect

2nd Order ΣΔ
Comparator Hysteresis



→ Comparator hysteresis < Δ/40 does not affect SNR

→ E.g. Δ=1V, comparator offset up to 25mV tolerable