EE247
Lecture 20

ADC Converters

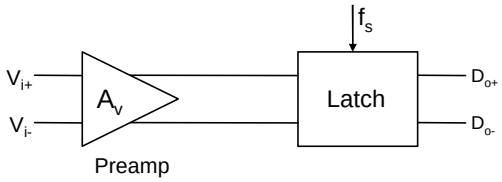
- Comparator architecture examples
- Flash ADC sources of error
  - Sparkle code
  - Meta-stability
- Techniques to reduce flash ADC complexity
  - Interpolating
  - Folding

Voltage Comparator Architectures

Comparator architectures

- High gain amplifier with differential analog input & single-ended large swing output
  - Output swing compatible with driving digital logic circuits
  - Open-loop amplification→ no frequency compensation required
  - Precise gain not required
- Latched comparators; in response to a strobe, input stage disabled & digital output stored in a latch till next strobe
  - Two options for implementation :
    - High-gain amplifier + simple digital latch
    - Low-gain amplifier + a high-sensitivity latch
- Sample-data comparators
  - S/H input
  - Offset cancellation
  - Pipelined stages

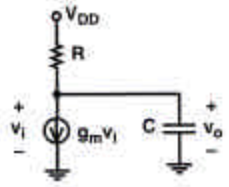
Latched Comparator



- Clock rate f_s
- Resolution
- Overload recovery
- Input capacitance (and linearity!)
- Power dissipation
- Input common-mode range
- Kickback noise
- …

Comparators Overdrive Recovery

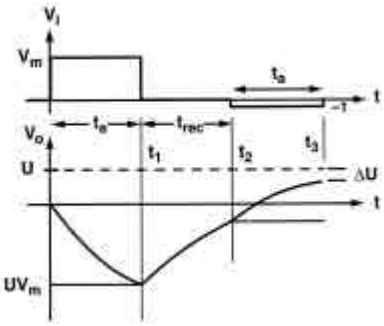
Linear model for a single-pole amplifier:



U→ amplification after time t_a

During reset amplifier settles exponentially to its zero input condition with τ_0=RC

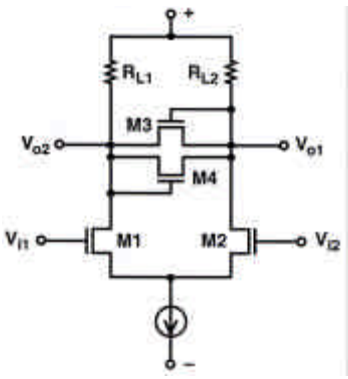
Assume Vm → maximum input normalized to 1/2lsb (=1)



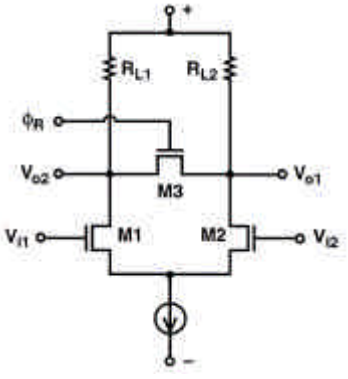
Example: Worst case input/output waveforms

→ Limit output voltage swing by
1. Passive clamp
2. Active restore
3. Low gain/stage

Comparators Overdrive Recovery Limiting Output

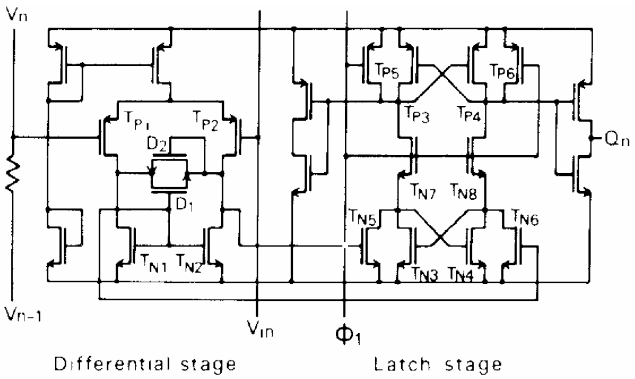


Clamp
Adds parasitic capacitance



Active Restore
After outputs are latched→ Activate ϕ_R & equalize output nodes

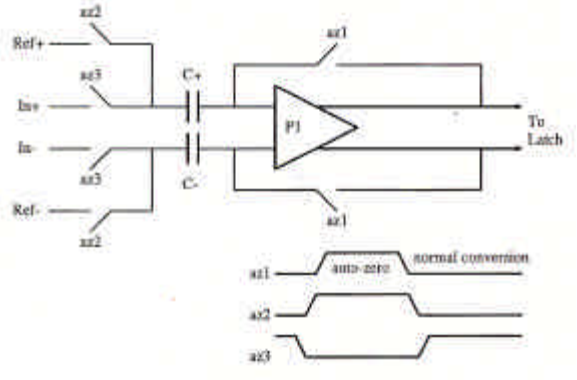
CMOS Comparator Example



- Flash ADC: 8bits, +-1/2LSB INL @ fs=15MHz (Vref=3.8V)
- No offset cancellation

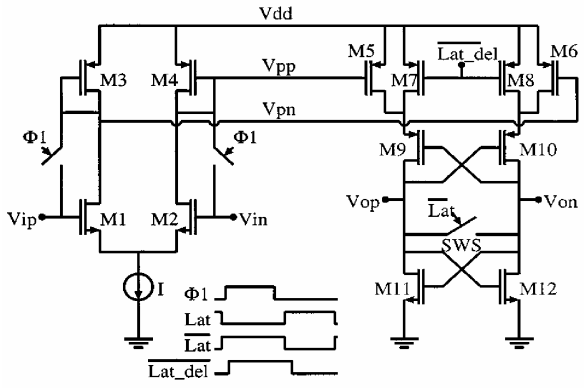
A. Yukawa, "A CMOS 8-Bit High-Speed A/D Converter IC," JSSC June 1985, pp. 775-9.

Comparator with Auto-Zero



I. Mehr and L. Singer, "A 500-Msample/s, 6-Bit Nyquist-Rate ADC for Disk-Drive Read-Channel Applications," JSSC July 1999, pp. 912-20.

Auto-Zero Implementation



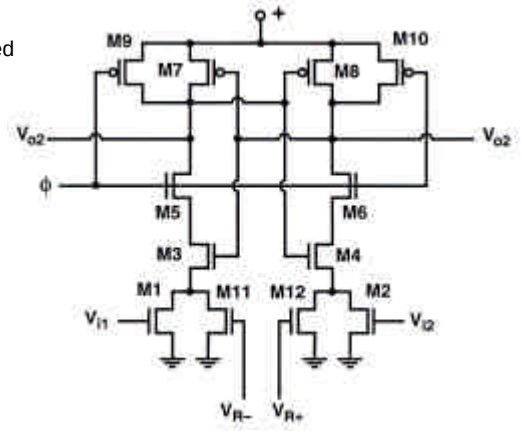
Ref:I. Mehr and L. Singer, "A 55-mW, 10-bit, 40-Msample/s Nyquist-Rate CMOS ADC," JSSC March 2000, pp. 318-25.

Comparator Example

- Variation on Yukawa latch used w/o preamp
- No dc power when ϕ high
- Good for low resolution ADCs
- M11 & M12 added to vary comparator threshold
- To 1st order, for W1=W2 & W11=W12

  $V_{th}^{latch} = W11/W1 \times V_R$

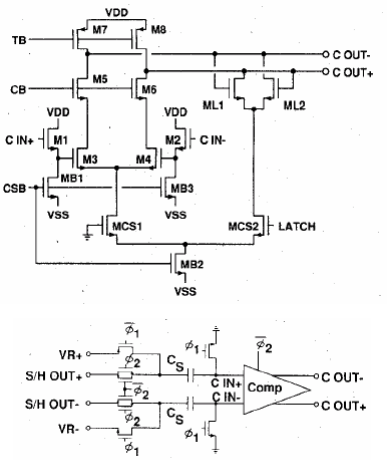
  where $V_R = V_{R+} - V_{R-}$



Ref: T. B. Cho and P. R. Gray, "A 10 b, 20 Msample/s, 35 mW pipeline A/D converter," *IEEE Journal of Solid-State Circuits,* vol. 30, pp. 166 - 172, March 1995.

Comparator Example

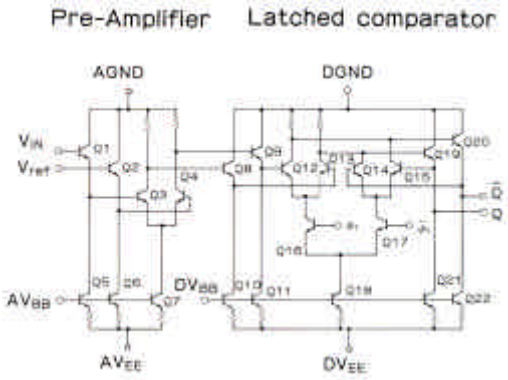
- Used in a pipelined ADC with digital correction
  → no offset cancellation
- Input buffers suppress kick-back
- Note differential reference
- M7, M8 operate in triode region
- Preamp gain ~10
- Current in MB2 switches by LATCH signal to flow either in the preamp or the latch.



Ref: S. Lewis, et al., "A Pipelined 5-Msample/s 9-bit Analog-to-Digital Converter" IEEE JSSC ,NO. 6, Dec. 1987

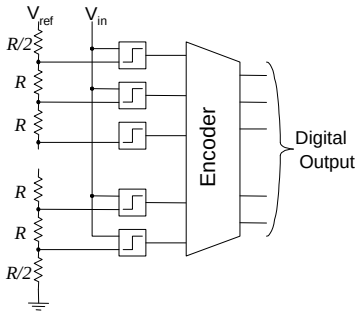
Bipolar Comparator Example

- Used in 8bit 400Ms/s & 6bit 2Gb/s flash ADC
- Signal amplification during $\phi 1$ high, latch operates when $\phi 1$ low
- Input buffers suppress kick-back & input current
- Separate ground and supply buses for front-end preamp → kick-back noise reduction



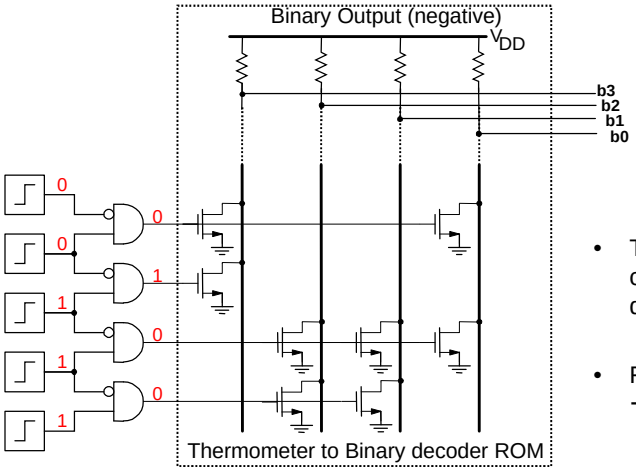
Ref: Y. Akazawa, et al., "A 400MSPS 8b flash AD conversion LSI," *IEEE International Solid-State Circuits Conference,* vol. XXX, pp. 98 - 99, February 1987.
Ref: T. Wakimoto, et al, "Si bipolar 2GS/s 6b flash A/D conversion LSI," *IEEE International Solid-State Circuits Conference,* vol. XXXI, pp. 232 - 233, February 1988.

Flash Converter Sources of Error



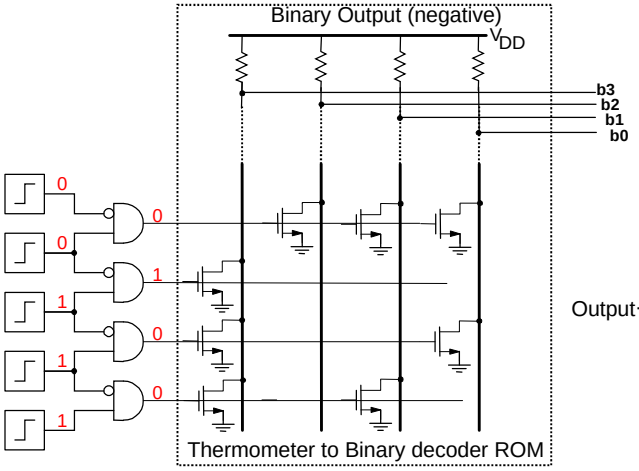
- Comparator input:
  - Offset
  - Nonlinear input capacitance
  - Kickback noise (disturbs reference)
  - Signal dependent sampling time
- Comparator output:
  - Sparkle codes (… 111101000 …)
  - Metastability

Typical Flash Output Encoder



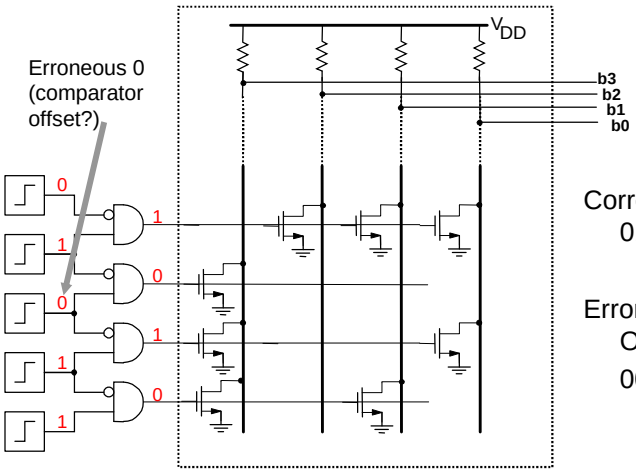
- Thermometer code → 1-of-n decoding
- Final encoding → NOR ROM

Typical Flash Output Decoder



	b3	b2	b1	b0
Output →	0	1	1	1

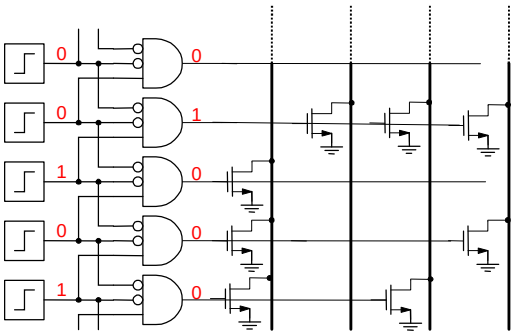
Sparkle Codes



Correct Output:
0111 … 1000

Erroneous Output:
0000

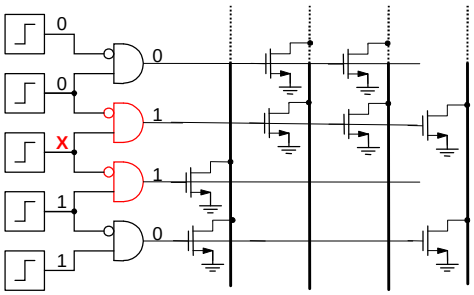
Sparkle Tolerant Encoder



Protects against a *single* sparkle.

Ref: C. Mangelsdorf et al, "A 400-MHz Flash Converter with Error Correction," JSSC February 1990, pp. 997-1002.

Meta-Stability



Different gates interpret metastable output X differently

Correct output: 0111 or 1000

Erroneous output: 0000

Solutions:
- –Latches (high power)
- –Gray encoding

Ref: C. Portmann and T. Meng, "Power-Efficient Metastability Error Reduction in CMOS Flash A/D Converters," JSSC August 1996, pp. 1132-40.

Gray Encoding

Thermometer Code							Gray			Binary		
T_1	T_2	T_3	T_4	T_5	T_6	T_7	G_3	G_2	G_1	B_3	B_2	B_1
0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	1	0	0	1
1	1	0	0	0	0	0	0	1	1	0	1	0
1	1	1	0	0	0	0	0	1	0	0	1	1
1	1	1	1	0	0	0	1	1	0	1	0	0
1	1	1	1	1	0	0	1	1	1	1	0	1
1	1	1	1	1	1	0	1	0	1	1	1	0
1	1	1	1	1	1	1	1	0	0	1	1	1

$$G_1 = T_1\overline{T_3} + T_5\overline{T_7}$$
$$G_2 = T_2\overline{T_6}$$
$$G_3 = T_4$$

- Each T_i affects only one G_i
  → Avoids disagreement of interpretation by multiple gates
- Protects also against sparkles
- Follow Gray encoder by (latch and) binary encoder

Reducing Flash ADC Complexity

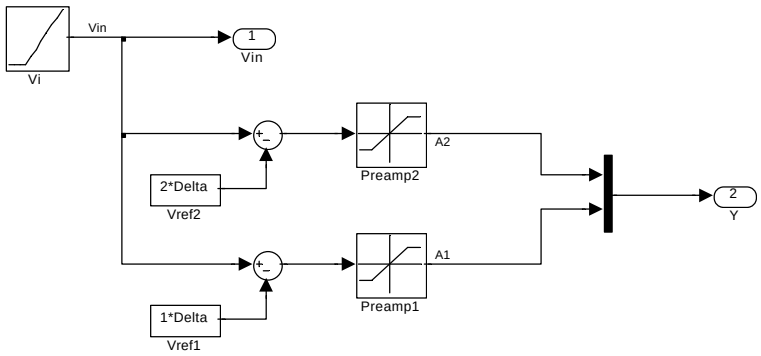
E.g. 10-bit "straight" flash
- Input range: 0 … 1V
- LSB = Δ: ~ 1mV
- Comparators: 1023 with offset << LSB
- Input capacitance: 1023 * 100fF = 102pF
- Power: 1023 * 3mW = 3W

Techniques:
- Interpolation
- Folding
- Folding & Interpolation
- Two-step, pipelining

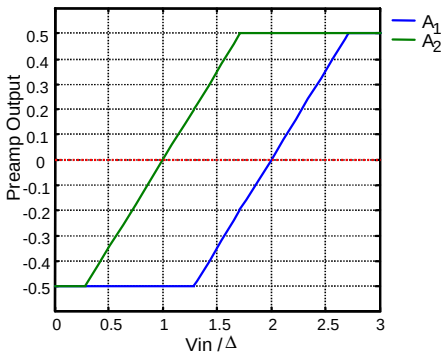
Interpolation

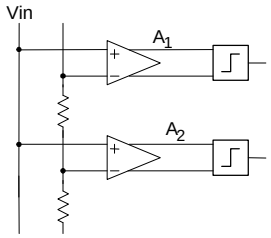
- Idea
  - Interpolation between preamp outputs
- Reduces number of preamps
  - Reduced input capacitance
  - Reduced area, power dissipation
- Same number of latches
- Important "side-benefit"
  - Decreased sensitivity to preamp offset
    → improved DNL

Simulink Model



Preamp Output



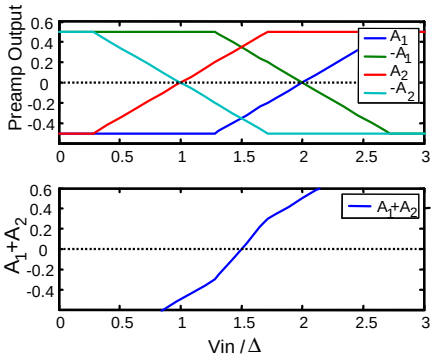


Zero crossings (to be detected by latches) at V_{in} =

$V_{ref1} = 1\ \Delta$

$V_{ref2} = 2\ \Delta$

Differential Preamp Output



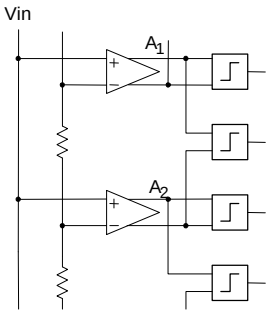
Zero crossings at V_{in} =

V_{ref1} = 1 Δ

V_{ref12} = 0.5*(1+2) Δ

V_{ref2} = 2 Δ

Interpolation in Flash ADC



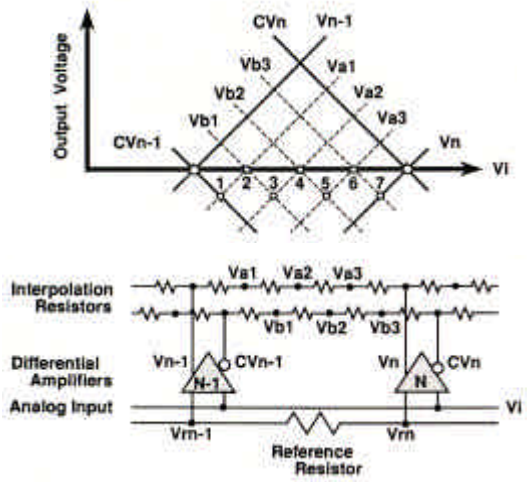
Half as many reference voltages and preamps

Interpolation factor:x2

Possible to accomplish higher interpolation factor

→ Resistive interpolation

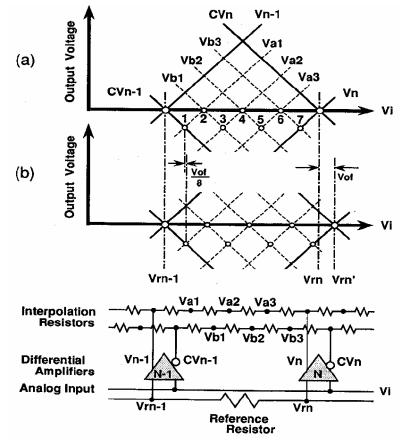
Resistive Interpolation



- Resistors produce additional levels
- With 4 resistors, the "interpolation factor" M=8 (ratio of latches/preamps)

Ref: H. Kimura et al, "A 10-b 300-MHz Interpolated-Parallel A/D Converter," JSSC April 1993, pp. 438-446.

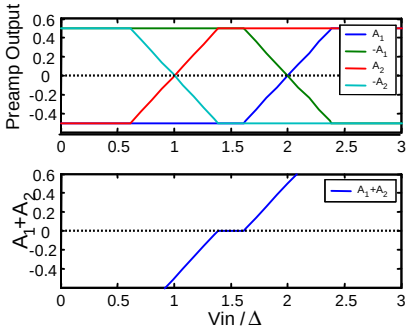
DNL Improvement



- Preamp offset distributed over M resistively interpolated voltages:
  → impact on DNL divided by M
- Latch offset divided by gain of preamp
  → use "large" preamp gain …

Ref: H. Kimura et al, "A 10-b 300-MHz Interpolated-Parallel A/D Converter," JSSC April 1993, pp. 438-446.

Preamp Input Range



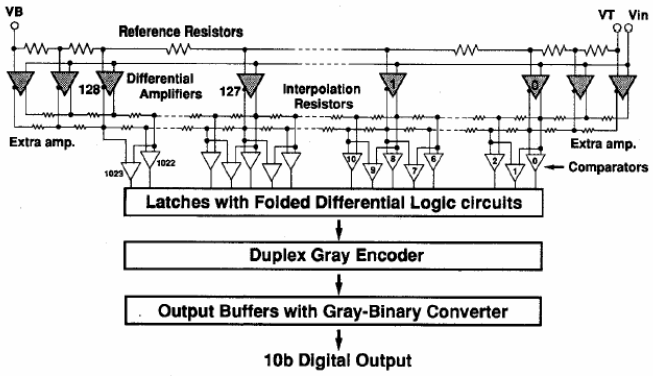
Linear preamp input ranges must overlap

i.e. range > Δ

Sets upper bound on gain

<< V_{DD} / Δ

Interpolated-Parallel ADC



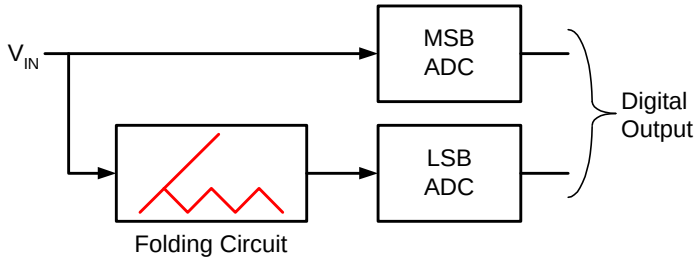
Ref: H. Kimura et al, "A 10-b 300-MHz Interpolated-Parallel A/D Converter," JSSC April 1993, pp. 438-446.

Measured Performance

Resolution		**10 b (7+3)**
Maximum conversion frequency		**300 MHz**
Integral non-linearity		**±1.0 LSB**
Differential non-linearity		**±0.4 LSB**
SNR/THD	**10MHz input**	**56/-59 dB**
	50MHz input	**48/-47 dB**
Input capacitance		**8 pF**
Input range		**2 V**
Power supply		**-5.2V**
Power dissipation		**4.0W**
Chip size		**9.0 × 4.2 mm²**
Element count		**36,000**
Technology		**1.0 μm bipolar:ft=25GHz**

Ref: H. Kimura et al, "A 10-b 300-MHz Interpolated-Parallel A/D Converter," JSSC April 1993, pp. 438-446.

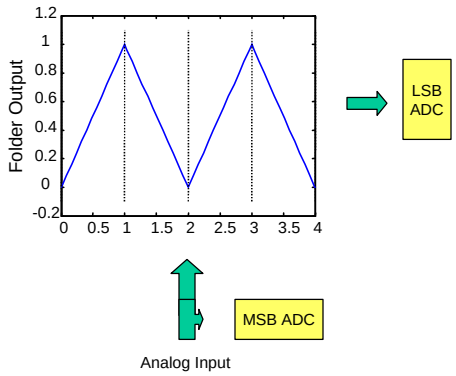
Folding Converter



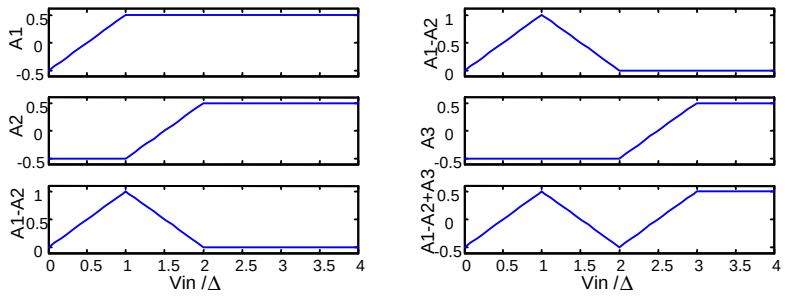
- Significantly fewer comparators than flash ~$2^{B/2+1}$
- Fast
- Nonidealities in folder limit resolution to ~10Bits

Folding

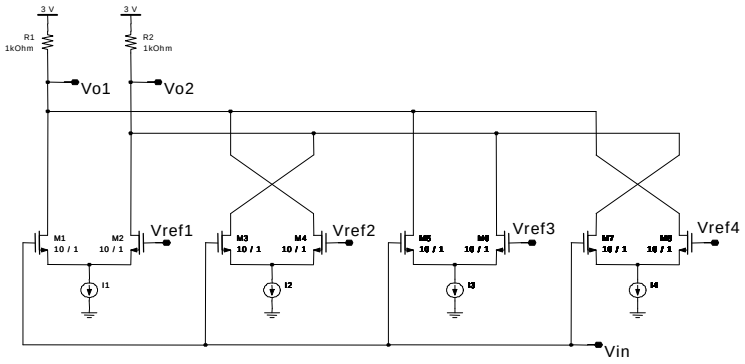
- Folder maps input to smaller range
- MSB ADC determines which fold input is in
- LSB ADC determines position within fold
- Logic circuit combines LSB and MSB results



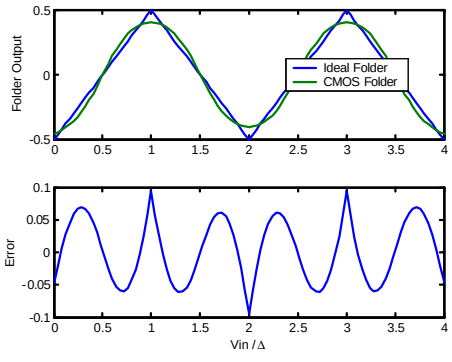
Generating Folds



Folding Circuit



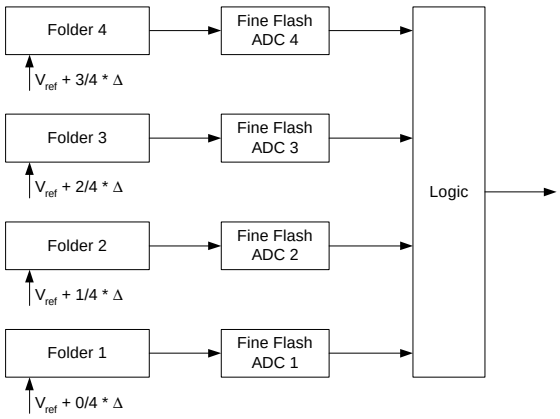
CMOS Folder Output



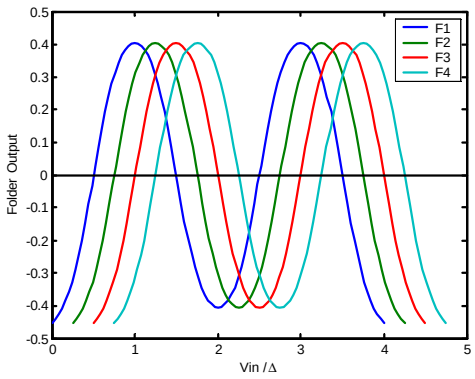
Accurate only at zero-crossings

Lowdown →
Most folding ADCs do not actually use the folds, but only the zero-crossings!

Parallel Folders



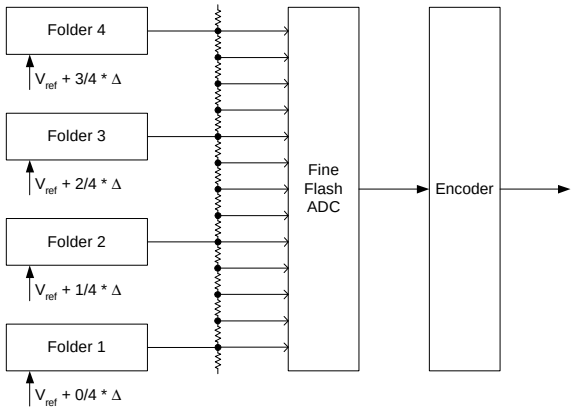
Parallel Folder Outputs



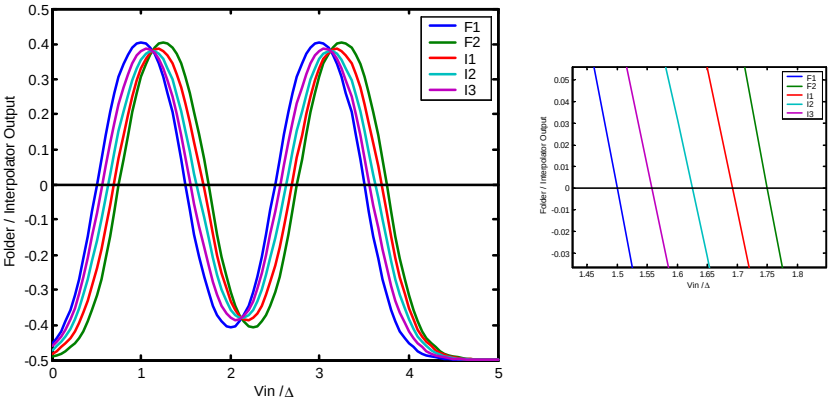
- 4 Folders
- 16 Zero crossings
- → only 4 LSB bits

- Better resolution
  - More folders
    → Large complexity
  - Interpolation

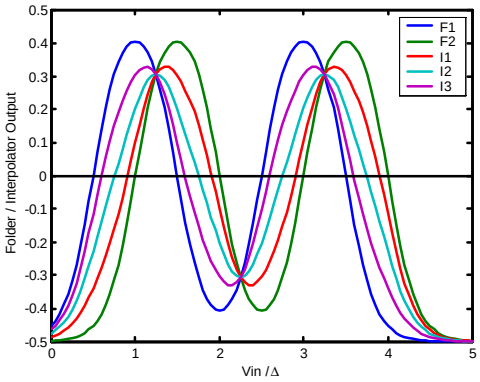
Folding & Interpolation

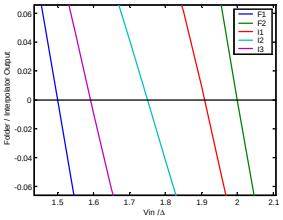


Folder / Interpolator Output



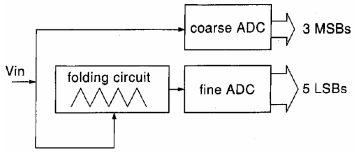
Folder / Interpolator Output

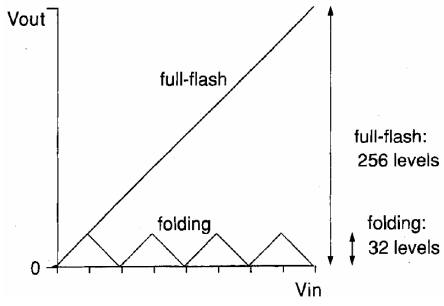




Interpolate only between closely spaced folds to avoid nonlinear distortion

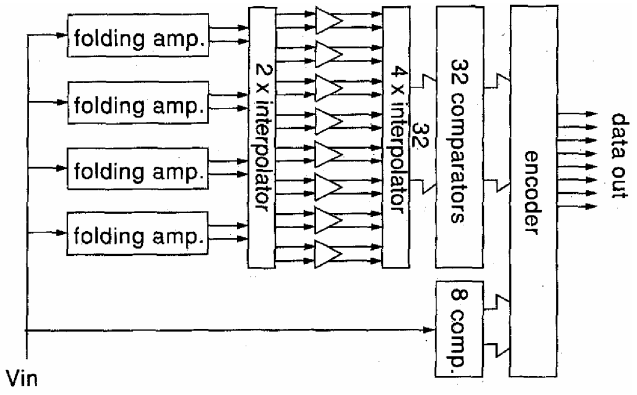
A 70-MS/s 110-mW 8-b CMOS Folding and Interpolating A/D Converter



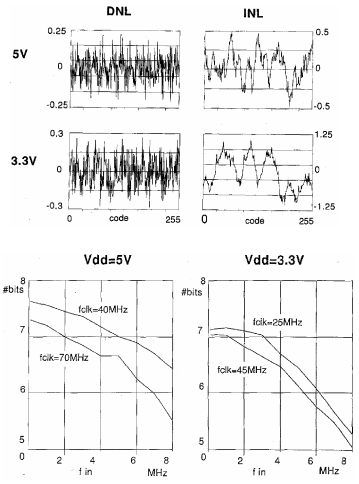


Ref: B. Nauta and G. Venes, JSSC Dec 1985, pp. 1302-8

A 70-MS/s 110-mW 8-b CMOS Folding and Interpolating A/D Converter



A 70-MS/s 110-mW 8-b CMOS Folding and Interpolating A/D Converter



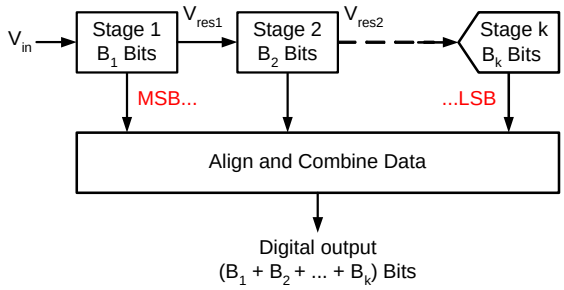
parameter		
resolution	8bit	
input capacitance	4.8 pF	
reference ladder resistance	720 Ω	
active area	0.7 mm^2	
technology	0.8μm, 1 poly , 2 metal, CMOS	
supply voltage	V_{dd}=5V	V_{dd}=3.3V
analog input	2Vpp	1.4Vpp
Integral nonlinearity	$\pm 0.5LSB$	$\pm 1.0LSB$
Differential nonlinearity	$\pm 0.2LSB$	$\pm 0.3LSB$
max. clock frequency	70MHz	45MHz
power dissipation	110mW	45mW

Pipelined ADCs

Pipelined A/D Converters

- Ideal Operation
- Errors and Correction
  - Redundancy
  - Digital Calibration
- Implementation
  - Practical Circuits
  - Stage Scaling

Block Diagram

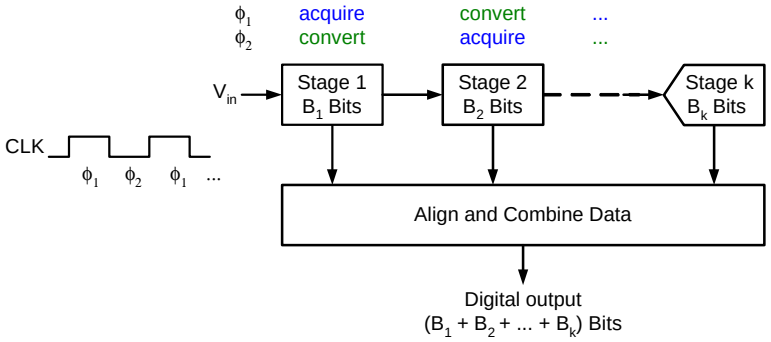


- Idea: Cascade several low resolution stages to obtain high overall resolution
- Each stage performs coarse A/D conversion and computes its quantization error, or "residue"

Characteristics

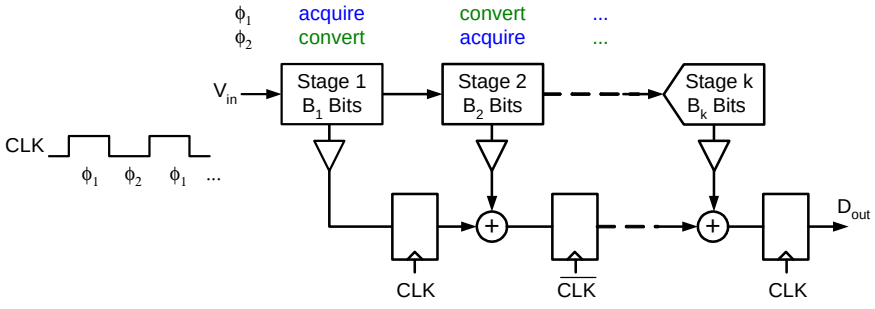
- Number of components (stages) grows linearly with resolution
- Pipelining
  - Trading latency for conversion speed
  - Latency may be an issue in e.g. control systems
  - Throughput limited by speed of one stage ® Fast
- Versatile: 8...16bits, 1...200MS/s
- Many analog circuit non-idealities can be corrected digitally

Concurrent Stage Operation



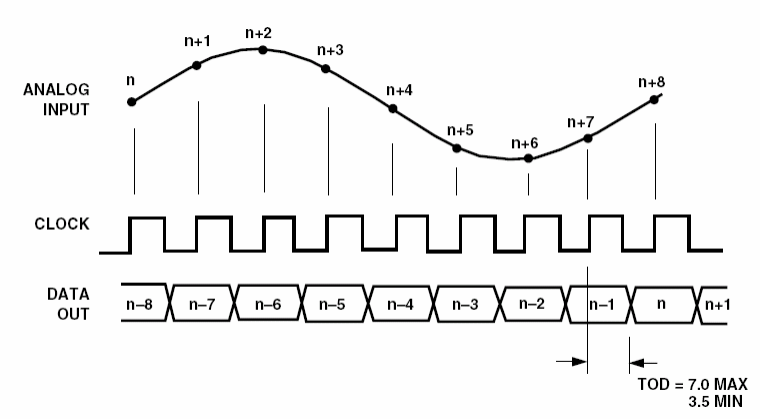
- Stages operate on the input signal like a shift register
- New output data every clock cycle, but each stage introduces ½ clock cycle latency

Data Alignment



- Digital shift register aligns sub-conversion results in time

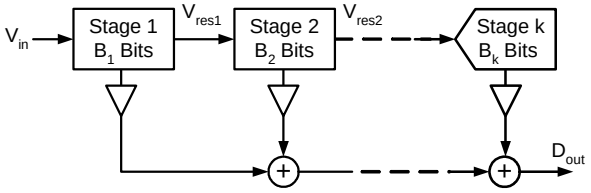
Latency



[Analog Devices, AD 9226 Data Sheet]

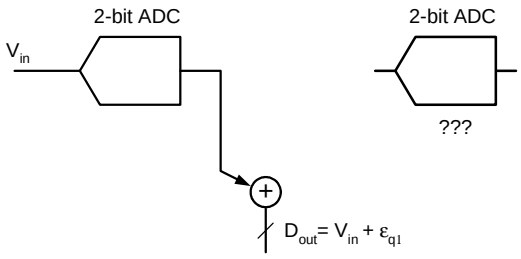
Pipelined ADC Analysis

- Ignore timing and use simple static model



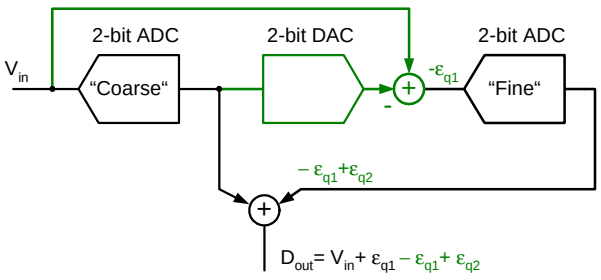
- Let's first look at "two-stage pipeline"
  - E.g.: Two cascaded 2-bit ADCs to get 4 bits of total resolution

Two Stage Example



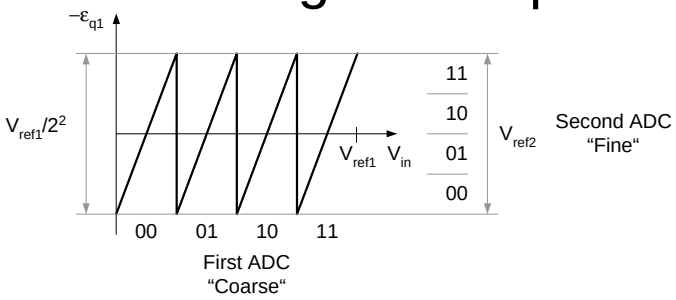
- Using only one ADC: Output contains large quantization error
- "Missing voltage" or "residue" ($-\varepsilon_{q1}$)
- Idea: Use second ADC to quantize and add $-\varepsilon_{q1}$

Two Stage Example



- Use DAC to compute missing voltage
- Add quantized representation of missing voltage
- Why does this help? How about ε_{q2} ?

Two Stage Example



- Fine ADC is re-used 2^2 times
- Fine ADC's full scale range needs to span only 1 LSB of coarse quantizer

$$e_{q2} = \frac{V_{ref\,2}}{2^2} = \frac{V_{ref\,1}}{2^2 \cdot 2^2}$$

Two Stage Transfer Function