EE247
Lecture 19

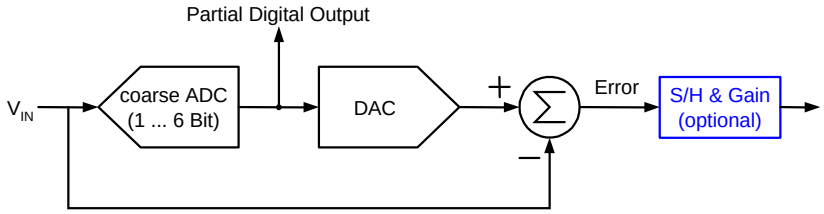
ADC Converters

- ADC architectures
- Comparator architectures
  - High gain amplifier with differential analog input & single-ended large swing output
  - Latched comparators; in response to a strobe, input stage disabled & digital output stored in a latch till next strobe
  - Sample-data comparators
    - Offset cancellation

ADC Architectures

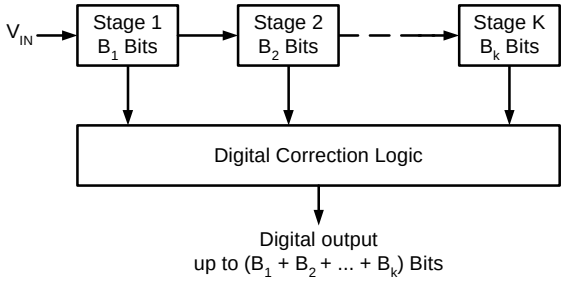
- Slope Converters
- Successive approximation
- Flash
- Folding
- Time-interleaved / parallel converter
- Residue type ADCs
  - Two-step
  - Pipeline
  - Algorithmic
  - ...
- Oversampled ADCs

Residue Type ADC



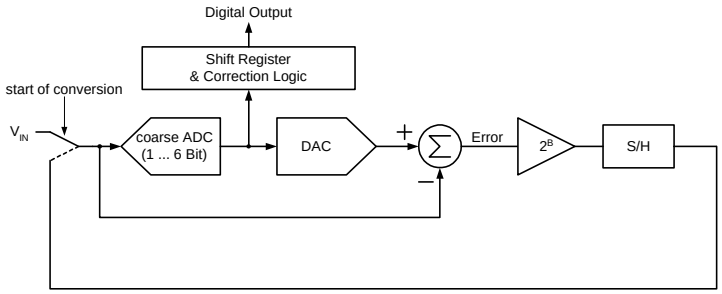
- Quantization error output ("residuum") enables cascading for higher resolution
- Great flexibility for stages: flash, oversampling ADC, …
- Optional S/H enables parallelism (pipelining)
- Fast: one clock per conversion (with S/H), latency

Pipelined ADC



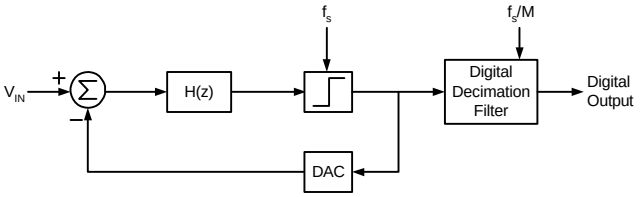
- Approaches speed of flash, but much lower complexity
- One clock per conversion, but K clocks latency
- Efficient digital calibration possible
- Versatile: from 16Bits / 1MS/s to 14Bits / 100MS/s

Algorithmic ADC



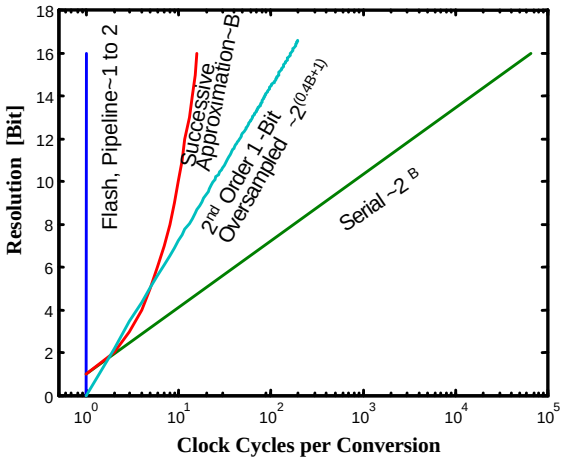
- Essentially same as pipeline, but a single stage is used for all partial conversions
- K clocks per conversion

Oversampled ADC

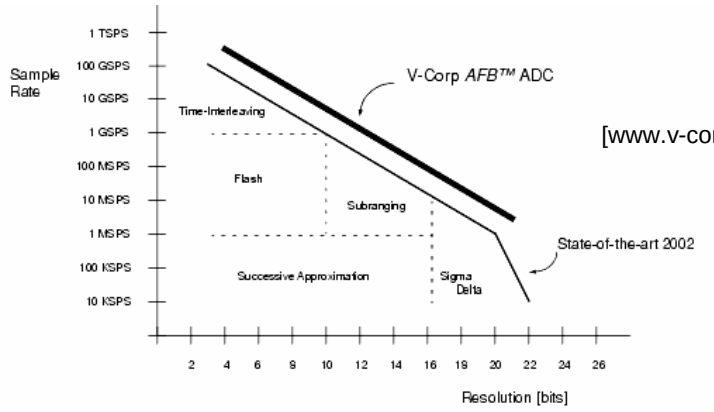


- Hard to comprehend … “easy” to build
- Input is oversampled (M times faster than output rate)
- Reduces Anti-Aliasing filter requirements and capacitor size
- Accuracy independent of component matching
- Very high resolution achievable (> 20 Bits)

Throughput Rate Comparison



Speed-Resolution Map



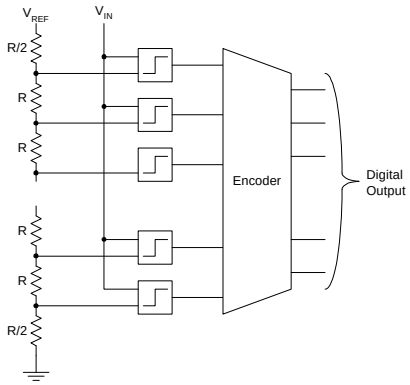
[www.v-corp.com]

High-Speed A/D Converters

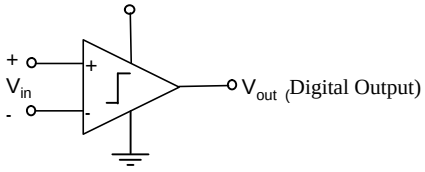
- Flash Converter
  - Comparator design considerations
  - Binary Encoder
- Interpolation
- Folding
- Pipelined ADCs

Flash Converter

- Very fast: only 1 clock cycle per conversion
- High complexity: 2^B-1 comparators
- High input capacitance



Voltage Comparators



Function: compare the instantaneous value of two analog signals

Important features:

- Maximum clock rate f_s → settling time, slew rate, small signal bandwidth
- Resolution→ gain, offset
- Overdrive recovery
- Input capacitance (and linearity!)
- Power dissipation
- Common-mode rejection
- Kickback noise
- …

Ref: Prof. B. Wooley, Course notes EE315 Stanford University

Voltage Comparator Architectures

Comparator architectures

- High gain amplifier with differential analog input & single-ended large swing output
  - Output swing compatible with driving digital logic circuits
  - Open-loop amplification→ no frequency compensation required
  - Precise gain not required
- Latched comparators; in response to a strobe, input stage disabled & digital output stored in a latch till next strobe
  - Two options for implementation :
    - High-gain amplifier + simple digital latch
    - Low-gain amplifier + a high-sensitivity latch
- Sample-data comparators
  - S/H input
  - Offset cancellation
  - Pipelined stages

Comparators w/ High-Gain Amplification

Amplify V_{in}(min) to V_{DD}

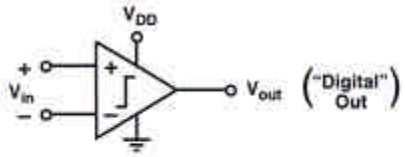
V_{in}(min) determined by ADC resolution

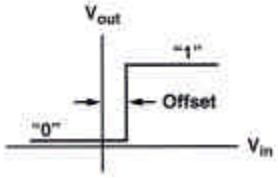
Example: 12-bit res. & full-scale input 2V→ 1LSB=0.5mV

→ For 2.5V output:

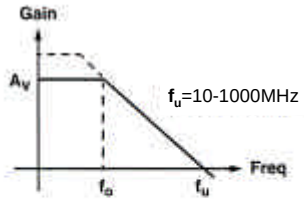
$$A_v = \frac{2.5V}{0.25mV} = 10{,}000$$

$$V_{os} < 1\,LSB$$





Comparators w/ High-Gain Amplification



f_u =unity gain frequency, f_0 $= -3dB$ frequency

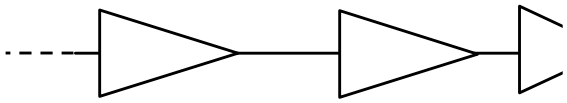
$$f_0 = \frac{f_u}{A_V} = \frac{1GHz}{10{,}000} = 100kHz$$

$$t_0 = \frac{1}{2p\,f_0} = 1.6m\,\text{sec}$$

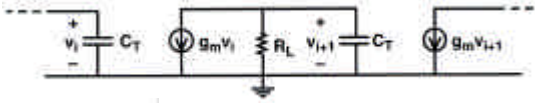
Too slow!

→ Cascade of lower gain stages to broadband response

Open Loop Cascade of Amplifiers



The stages identical → small-signal model for the cascades:



For 1-stage only:

$|A_V(0)| = g_m R_L$

ω_o = – 3dB frequency = $\dfrac{1}{R_L C_T}$

ω_u = – unity gain frequency = G×BW = $\dfrac{g_m}{C_T}$

$\therefore \omega_o = \dfrac{\omega_u}{|A_V(0)|}$

Open Loop Cascade of Amplifiers

For Cascade of N-stages:

$$A_T(j\omega) = [A_V(j\omega)]^N = \frac{|A_V(0)|^N}{\left(1 + j\frac{\omega}{\omega_o}\right)^N}$$

Define

ω_{oN} = –3dB frequency of the N-stage cascade

Then

$$|A_T(j\omega_{oN})| = \frac{|A_V(0)|^N}{\sqrt{2}}$$

and

$$\omega_{oN} = \omega_o\sqrt{2^{1/N} - 1} = \frac{\omega_u}{|A_V(0)|}\sqrt{2^{1/N} - 1}$$

∴ For a specified $|A_T(0)|$

$$|A_V(0)| = |A_T(0)|^{1/N}$$

$$\Rightarrow \omega_{oN} = \frac{\omega_u}{|A_T(0)|^{1/N}}\sqrt{2^{1/N} - 1}$$

Thus,

$$\frac{\omega_{oN}}{\omega_{o1}} = \left[\frac{\omega_u}{|A_T(0)|^{1/N}}\sqrt{2^{1/N} - 1}\right] \Big/ \left[\frac{\omega_u}{|A_T(0)|}\right]$$

$$= |A_T(0)|^{\left(\frac{N-1}{N}\right)}\sqrt{2^{1/N} - 1}$$

Open Loop Cascade of Amplifiers

For $|A_T(DC)|$=10,000

N	ω_{0N}/ω_{01}	$\|A_V(0)\|$
1	1	10,000
2	64	100
3	236	21.5
4	435	10
5	611	6.3
10	1067	2.5
20	1185	1.6

Example:

$N = 3,\ f_u = 1\text{GHz},\ A_T(0) = 10000$

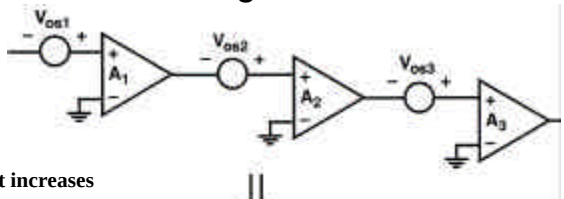
$$f_{0N} = \frac{1GHz}{(10{,}000)^{1/3}}\sqrt{2^{1/3}-1} = 24MHz$$

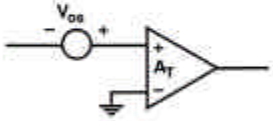
$$t_{0N} = \frac{1}{2p\, f_{0N}} = 7n\text{sec} \quad (1.6ms \text{ for 1-stage})$$

$$5t_{0N} = 35n\text{sec}$$

Cascade of 3-stage
→speed 236 higher compared to 1-stage (constant overall gain & f_u)

Open Loop Cascade of Amplifiers Offset Voltage





•Cascade of amplifiers
→Input-referred offset increases
•Choice of # of stages important
→Speed vs offset tradeoff

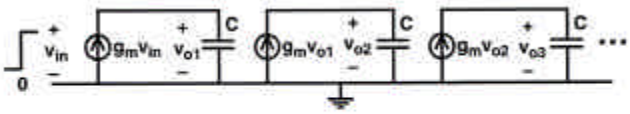
Example:
For 3-stage case with gain/stage ~22
→ Increase in offset ~ 4.5%

$$A_T = A_1 \cdot A_2 \cdot A_3$$

$$V_{os} = V_{os1} + \frac{V_{os2}}{A_1} + \frac{V_{os3}}{A_1 \cdot A_2}$$

Open Loop Cascade of Amplifiers Step Response

•**Assuming linear behavior**



$$v_{o1} = \frac{1}{C}\int_0^t g_m v_{in}\,dt = \frac{g_m}{C} v_{in} t$$

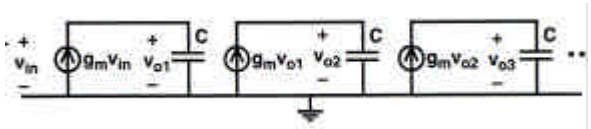
$$v_{o2} = \frac{1}{C}\int_0^t g_m v_{o1}\,dt = \frac{g_m}{C}\int_0^t \frac{g_m}{C} v_{in}\,dt = \frac{1}{2}\left(\frac{g_m}{C}\right)^2 v_{in} t^2$$

$$v_{o3} = \frac{1}{C}\int_0^t g_m v_{o2}\,dt = \frac{g_m}{C}\int_0^t \left[\frac{1}{2}\left(\frac{g_m}{C}\right)^2 v_{in} t^2\right] dt$$

$$= \frac{1}{3}\left(\frac{1}{2}\right)\left(\frac{g_m}{C}\right)^3 v_{in} t^3$$

Open Loop Cascade of Amplifiers Step Response

•**Assuming linear behavior**



N Stages

$$v_{oN} = \left(\frac{g_m}{C}\right)^N \left(\frac{t^N}{N!}\right) v_{in}$$

For the output to reach a specified v_{out} (i.e., $v_{oN} = v_{out}$) the delay is

$$\tau_D = \left(\frac{C}{g_m}\right)\left[(N!)\left(\frac{v_{out}}{v_{in}}\right)\right]^{1/N}$$

Open Loop Cascade of Amplifiers Delay/(C/g_m)

- **Minimum total delay broad function of N**
- **Relationship between # of stages that minimize delay (N_{op}) and gain (V_{out}/V_{in}) approximately:**

$$N_{op}=1.1x\ln(V_{out}/V_{in}) +0.79$$

for gain <1000

- **Or gain of 10dB (sqrt10) per stage results in near optimum delay**

Delay/(C/g_m)

N \ V_{out}/V_{in}	10	100	1000	10K
1	10	100	1000	10K
2	4.5	14.1	44.7	141
3	3.9	8.4	18.2	39.1
4	3.9	7.0	12.4	22.1
5	4.1	6.5	10.4	16.4
6	4.4	6.4	9.5	13.9
7	4.7	6.5	9.1	12.6
8	5.0	6.7	8.9	11.9
9	5.4	6.9	8.9	11.5
10	5.7	7.2	9.0	11.4
11	6.1	7.5	9.2	11.3
12	6.4	7.8	9.4	11.4
20	9.3	10.5	11.7	13.2

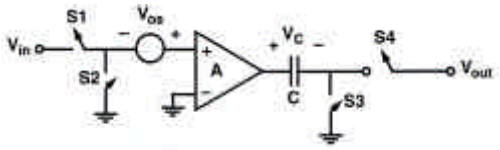
Ref: J.T. Wu, et al., "A 100-MHz pipelined CMOS comparator " *IEEE Journal of Solid-State Circuits,* vol. 23, pp. 1379 - 1385, December 1988.

Offset Cancellation

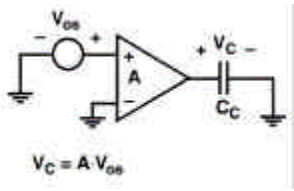
- **Disadvantage of using cascade of amplifiers:**
  - → **Increased overall input-referred offset**
- **Sampled-data cascade of amplifiers V_{os} can be cancelled**
  - → **Store on ac-coupling capacitors in series with amplifier stages**
- **Offset associated with a specific amplifier can be cancelled by storing it in series with either the input or the output of that stage**

Offset Cancellation
Output Series Cancellation

•Amp modeled as ideal + V_{os} (input referred)

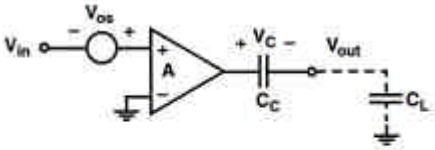


•Store offset:
- •S1, S4➔ open
- •S2, S3→ closed
  - → V_C=AxV_{OS}



Offset Cancellation
Output Series Cancellation

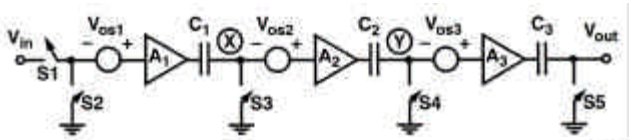
Amplify:
- •S1, S4➔ closed
- •S2, S3→ open
  - →V_C=AxV_{OS}



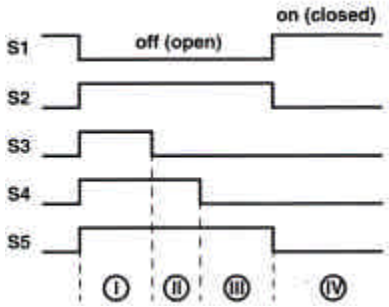
Circuit requirements:
- •Amp not saturate during offset storage
- •High-impedance (C) load → C_c not discharged
- •C_c >> C_L to avoid attenuation
- •C_c >> C_{switch} offset due to charge injection

$$V_{out} = A \cdot (V_{in} + V_{os}) - V_C$$
$$= A \cdot (V_{in} + V_{os}) - A \cdot V_{os}$$
$$= A \cdot V_{in}$$

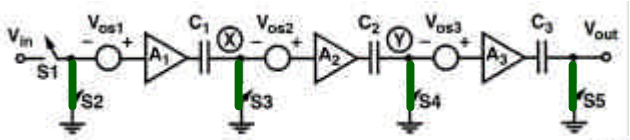
Offset Cancellation
Cascaded Output Series Cancellation



Note: Extra offset cancellation phase required
→ Overall speed compromised

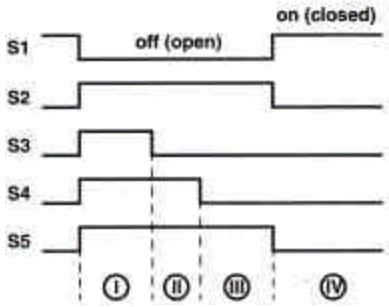


Offset Cancellation
Cascaded Output Series Cancellation

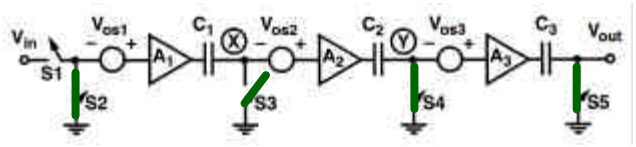


1- S1→ open, S2,3,4,5 closed

$V_{C1}=A_1xV_{os1}$
$V_{C2}=A_2xV_{os2}$
$V_{C3}=A_3xV_{os3}$



Offset Cancellation
Cascaded Output Series Cancellation



2- S3→ open

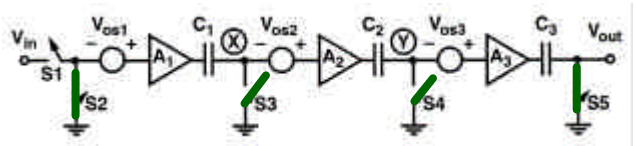
- •Feedthrough from S3 → offset on X
- •Switch offset , ε_2 stored on C1
- •Since S4 remains closed, offset associated with ε_2 → stored on C2

$V_X = \varepsilon_2$

$V_{C1} = A_1 x V_{os1} - \varepsilon_2$

$V_{C2} = A_2 x (V_{os2} + \varepsilon_2)$

Offset Cancellation
Cascaded Output Series Cancellation



3- S4→ open

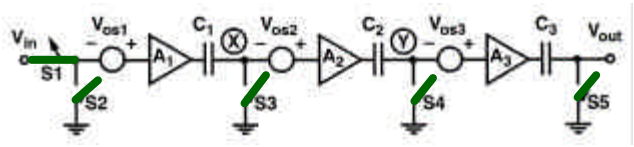
- •Feedthrough from S4 → offset on Y
- •Switch offset , ε_3 stored on C2
- •Since S5 remains closed, offset associated with ε_3 → stored on C3

$V_Y = \varepsilon_3$

$V_{C2} = A_2 x (V_{os2} + \varepsilon_2) - \varepsilon_3$

$V_{C3} = A_3 x (V_{os3} + \varepsilon_3)$

Offset Cancellation
Cascaded Output Series Cancellation



4- S2→ open, S1→ closed, S5→ open

- S1 closed & S2 open → since input connected to low impedance source charge injection not of major concern
- Switch offset , ε_4 introduced due to S5 opening
- ε_4 not cancelled
- As shown in the following analysis, ε_4 referred to the input will be attenuated by the overall gain

Offset Cancellation
Cascaded Output Series Cancellation

$$V_X = A_1(V_{in} + V_{os1}) - V_{C1}$$
$$= A_1(V_{in} + V_{os1}) - (A_1 V_{os1} - \varepsilon_2)$$
$$= A_1 V_{in} + \varepsilon_2$$

$$V_Y = A_2(V_X + V_{os2}) - V_{C2}$$
$$= A_2(A_1 V_{in} + \varepsilon_2 + V_{os2}) - [A_2(V_{os2} + \varepsilon_2) - \varepsilon_3)]$$
$$= A_1 A_2 V_{in} + \varepsilon_3$$

$$V_{out} = A_3(V_Y + V_{os3}) - V_{C3}$$
$$= A_3(A_1 A_2 V_{in} + \varepsilon_3 + V_{os3}) - [A_3(V_{os3} + \varepsilon_3) - \varepsilon_4)]$$
$$= A_1 A_2 A_3 V_{in} + \varepsilon_4$$

Offset Cancellation
Cascaded Output Series Cancellation

$$V_{out} = A_1 \cdot A_2 \cdot A_3\left(V_{in} + \frac{E_4}{A_1 \cdot A_2 \cdot A_3}\right)$$

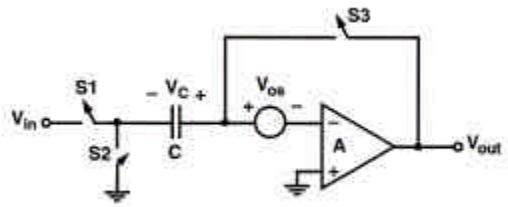
$$\text{Input-Referred Offset} = \left(\frac{E_4}{A_1 \cdot A_2 \cdot A_3}\right)$$

Example:
3-stage open-loop differential amplifier with offset cancellation + output amplifier (see ref.)

$A_{Total}(DC) = 2x10^6 = 120dB$
Input-referred offset $< 5\mu V$
Input-referred offset drift $< 0.05\mu V$

Ref: :R. Poujois and J. Borel, "A low drift fully integrated MOSFET operational amplifier," *IEEE Journal of Solid-State Circuits,* vol. 13, pp. 499 - 503, August 1978.

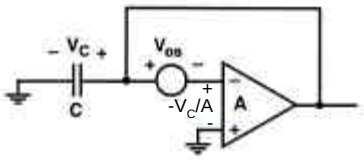
Offset Cancellation
Input Series Cancellation



Offset Cancellation
Input Series Cancellation

Store offset

S1 = 0 (off)
S2, S3 = 1 (conducting)



$$V_C = -A(V_C - V_{os})$$

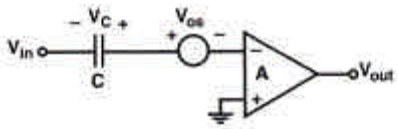
$$= \left(\frac{A}{A+1}\right)V_{os} - V_{os}$$

Note: Amplifier has to be compensated for unity gain stability

Offset Cancellation
Input Series Cancellation

Amplify

S2, S3 → open
S1→ closed



$$V_{out} = -A(V_{in} + V_C - V_{os}) = -A\left[V_{in} + V_{os}\left(\frac{A}{A+1} - 1\right)\right]$$

$$\therefore V_{out} = -A\left(V_{in} - \frac{V_{os}}{A+1}\right)$$

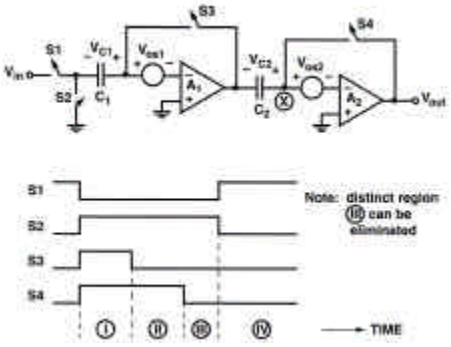
and

Input-Referred Offset = $\frac{V_{os}}{A+1}$

Offset Cancellation
Cascaded Input Series Cancellation

$$V_{out} = A_1 A_2 \left[V_{in} + \frac{V_{os2}}{A_1(A_2+1)} - \frac{\varepsilon_2}{A_1} \right]$$

$$\text{Input-Referred Offset} = \frac{V_{os2}}{A_1(A_2+1)} - \frac{\varepsilon_2}{A_1}$$



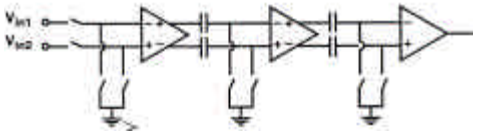
ε_2 →opening of S4 charge injection

→Amplifier A1 offset → fully cancelled
→Amplifier A2 offset → attenuated by 1/A1.A2
→Error associated with opening of S4 charge injection attenuated by 1/A1

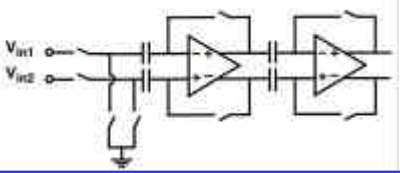
CMOS Comparators
Cascade of Gain Stages

Fully differential gain stages → 1st order cancellation of switch feedthrough & charge injection offsets

1-Output series offset cancellation

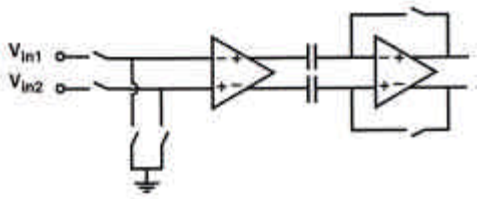


2- Input series offset cancellation



CMOS Comparators
Cascade of Gain Stages

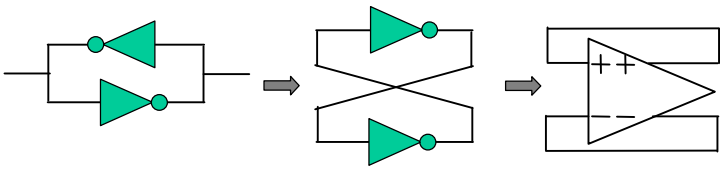
3-Combined input & output series offset cancellation



V_{os1} & V_{os2} are both stored on a single pair of coupling capacitors

CMOS Latched Comparators

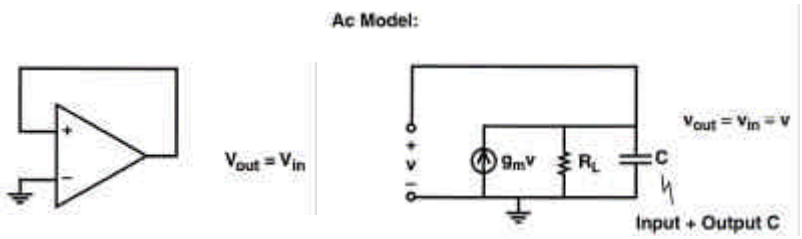
Comparator amplification need not be linear
→can use a latch → regeneration



→ Amplification + positive feedback

CMOS Latched Comparators

Latch can be modeled as a single-pole amp + positive feedback



CMOS Latched Comparators Delay

$$g_m v = \frac{v}{R_L} + C\frac{dv}{dt}$$

$$\frac{g_m}{C}\left(1 - \frac{1}{g_m R_L}\right)v = C\frac{dv}{dt}$$

$$\frac{g_m}{C}\left(1 - \frac{1}{g_m R_L}\right)\int_{t_1}^{t_2} dt = \int_{v_1}^{v_2}\frac{1}{v}dv$$

Latch Delay

$$\tau_D = t_2 - t_1 = \frac{C}{g_m}\left(\frac{1}{1 - \frac{1}{g_m R_L}}\right)\ln\left(\frac{v_2}{v_1}\right)$$

where $\frac{v_2}{v_1} = A_L$ = "LATCH GAIN"

For $g_m R_L >> 1$

$$\tau_D = \left(\frac{C}{g_m}\right)\ln(A_L)$$

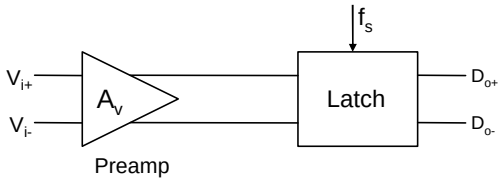
τ_D(3-state amp)= 18.2(C/g_m)

Normalized Latch Delay

A_L	$\frac{\tau_D}{(C/g_m)}$
10	2.3
100	4.6
1000	6.9
10K	9.2

Compared to a 3-stage open-loop cascade of amps for equal gain of 1000
→Latch faster by about x3
Only drawback → high latch offset (typically 10- 100mV)
→Use preamp w/gain =10-100 to reduce input-referred latch offset
→Or use offset cancellation

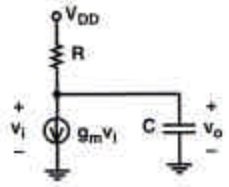
Latched Comparator



- Clock rate f_s
- Resolution
- Overload recovery
- Input capacitance (and linearity!)
- Power dissipation
- Common-mode rejection
- Kickback noise
- …

Comparators Overdrive Recovery

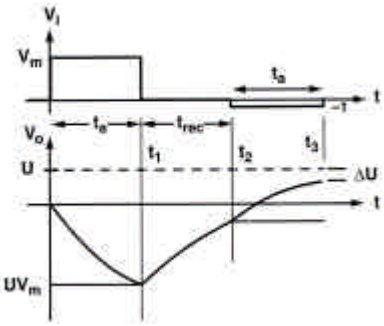
Linear model for a single-pole amplifier:



U→ amplification after time t_a

During reset amplifier settles exponentially to its zero input condition with τ_0=RC

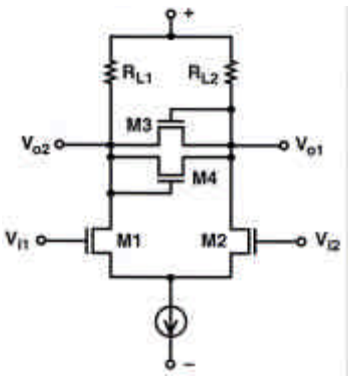
Assume Vm → maximum input normalized to 1/2lsb (=1)



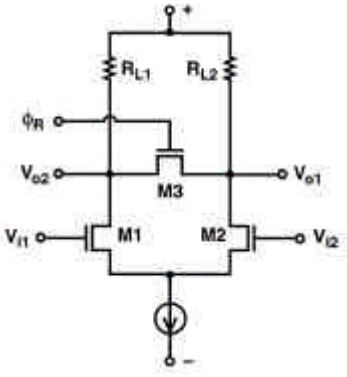
Example: Worst case input/output waveforms

→ Limit output voltage swing by
1. Passive clamp
2. Active restore
3. Low gain/stage

Comparators Overdrive Recovery Limiting Output

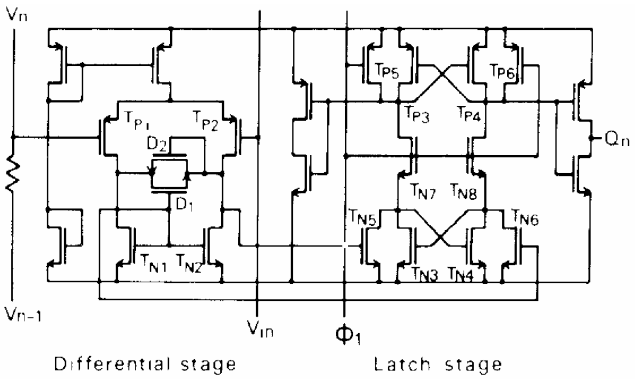


Clamp
Adds parasitic capacitance



Active Restore
After outputs are latched→ Activate ϕ_R & equalize output nodes

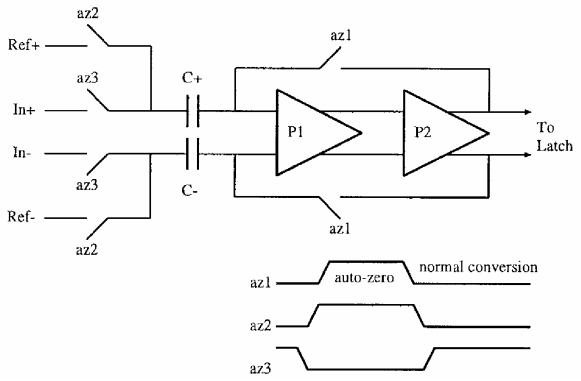
CMOS Comparator Example



- Flash ADC: 8bits, +-1/2LSB INL @ fs=15MHz (Vref=3.8V)
- No offset cancellation

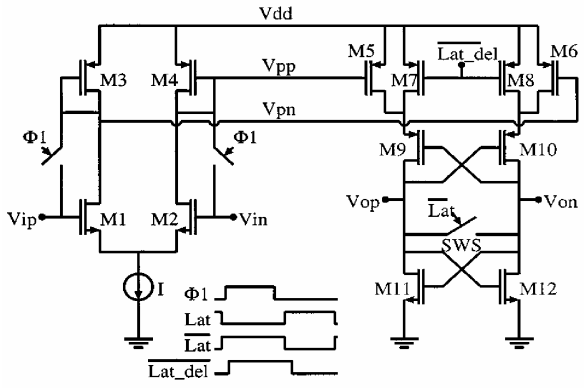
A. Yukawa, "A CMOS 8-Bit High-Speed A/D Converter IC," JSSC June 1985, pp. 775-9.

Comparator with Auto-Zero



I. Mehr and L. Singer, "A 500-Msample/s, 6-Bit Nyquist-Rate ADC for Disk-Drive Read-Channel Applications," JSSC July 1999, pp. 912-20.

Auto-Zero Implementation



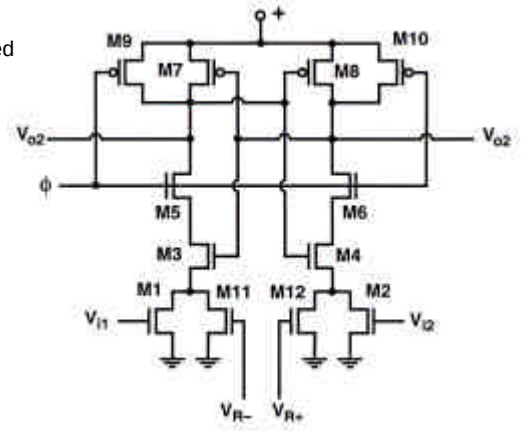
Ref:I. Mehr and L. Singer, "A 55-mW, 10-bit, 40-Msample/s Nyquist-Rate CMOS ADC," JSSC March 2000, pp. 318-25.

Comparator Example

- Variation on Yukawa latch used w/o preamp
- No dc power when ϕ high
- Good for low resolution ADCs
- M11 & M12 added to vary comparator threshold
- To 1st order, for W1=W2 & W11=W12

  $V_{th}^{latch} = W11/W1 \times V_R$

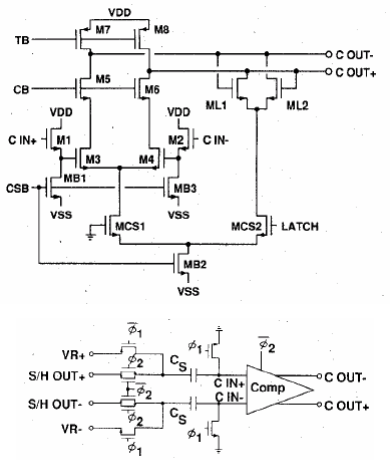
  where $V_R = V_{R+} - V_{R-}$



Ref: T. B. Cho and P. R. Gray, "A 10 b, 20 Msample/s, 35 mW pipeline A/D converter," *IEEE Journal of Solid-State Circuits,* vol. 30, pp. 166 - 172, March 1995.

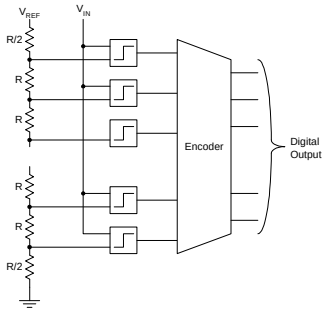
Comparator Example

- Used in a pipelined ADC with digital correction
  → no offset cancellation
- Note differential reference
- M7, M8 operate in triode region
- Preamp gain ~10
- Input buffers suppress kick-back



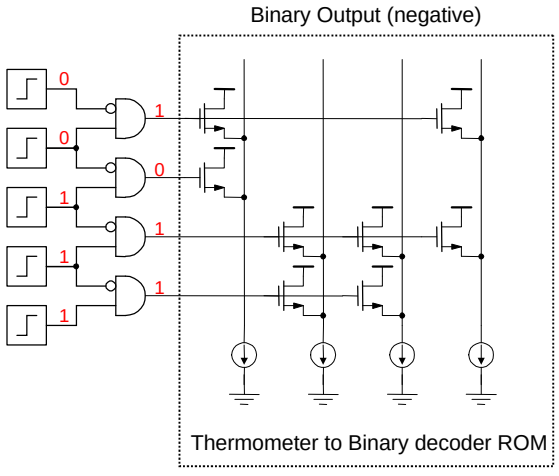
Ref: S. Lewis, et al., "A Pipelined 5-Msample/s 9-bit Analog-to-Digital Converter" IEEE JSSC ,NO. 6, Dec. 1987

Flash Converter Errors

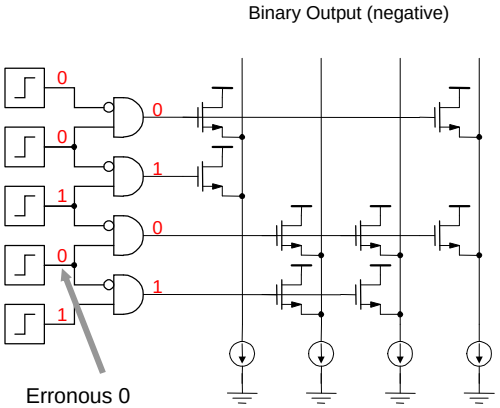


- Comparator input:
  - Offset
  - Nonlinear input capacitance
  - Kickback noise (disturbs reference)
  - Signal dependent sampling time
- Comparator output:
  - Sparkle codes (… 111101000 …)
  - Metastability

Typical Flash Output Decoder



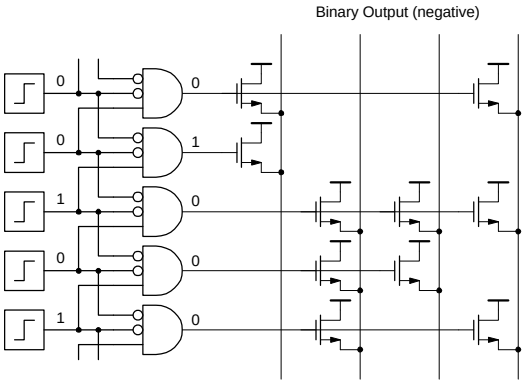
Sparkle Codes



Correct Output:
0110 … 1000

Actual Output:
1110

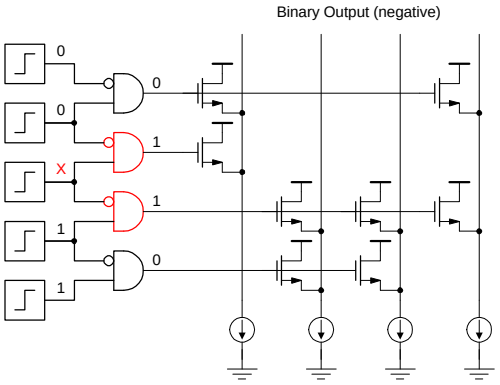
Sparkle Tolerant Encoder



Protects against a *single* sparkle.

Ref: C. Mangelsdorf et al, "A 400-MHz Flash Converter with Error Correction," JSSC February 1990, pp. 997-1002.

Meta Stability



Different gates interpret metastable output X differently

Correct Output: 0111 or 1000

Actual Output: 1111

Solutions:
- –Latches (high power)
- –Gray encoding

Ref: C. Portmann and T. Meng, "Power-Efficient Metastability Error Reduction in CMOS Flash A/D Converters," JSSC August 1996, pp. 1132-40.

Gray Encoding

Thermometer Code							Gray			Binary		
T_1	T_2	T_3	T_4	T_5	T_6	T_7	G_3	G_2	G_1	B_3	B_2	B_1
0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	1	0	0	1
1	1	0	0	0	0	0	0	1	1	0	1	0
1	1	1	0	0	0	0	0	1	0	0	1	1
1	1	1	1	0	0	0	1	1	0	1	0	0
1	1	1	1	1	0	0	1	1	1	1	0	1
1	1	1	1	1	1	0	1	0	1	1	1	0
1	1	1	1	1	1	1	1	0	0	1	1	1

$$G_1 = T_1\overline{T_3} + T_5\overline{T_7}$$
$$G_2 = T_2\overline{T_6}$$
$$G_3 = T_4$$

- Each T_i affects only one G_i
  → Avoids disagreement of interpretation by multiple gates
- Protects also against sparkles
- Follow Gray encoder by (latch and) binary encoder