EE247
Lecture 17

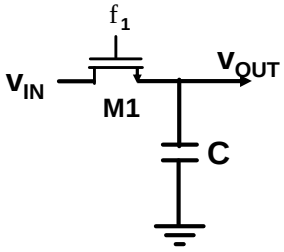
ADC Converters

- Sampling
  - Sampling switch induced distortion
    - Sampling switch conductance dependence on input voltage
  - Sampling switch charge injection
    - Complementary switch
    - Use of dummy device
    - Bottom-plate switching
  - Track & hold circuit
  - S/H circuit incorporating gain
- ESD protection impact on converter performance

Practical Sampling

- kT/C noise

$$C \geq 12 k_B T \left(\frac{2^B - 1}{V_{FS}} \right)^2$$



- Finite R_{sw} → limited bandwidth

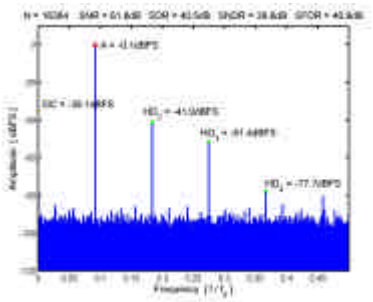
$$R << -\frac{1}{2 f_s C} \frac{1}{\ln\left(2^B - 1\right)}$$

- $g_{sw} = f(V_{in})$ → distortion

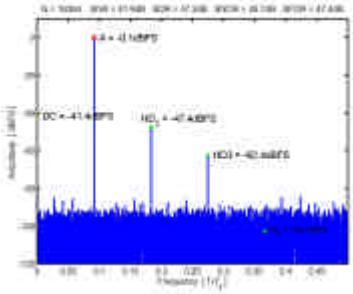
$$g_{ON} = g_o \left(1 - \frac{V_{in}}{V_{DD} - V_{th}} \right) \quad \text{for} \quad g_o = \mu C_{ox} \frac{W}{L} \left(V_{DD} - V_{th} \right)$$

- Switch charge injection
- Clock jitter

Sampling Distortion



10bit ADC & T/τ = 10
$V_{DD} - V_{th}$ = 2V V_{FS} = 1V

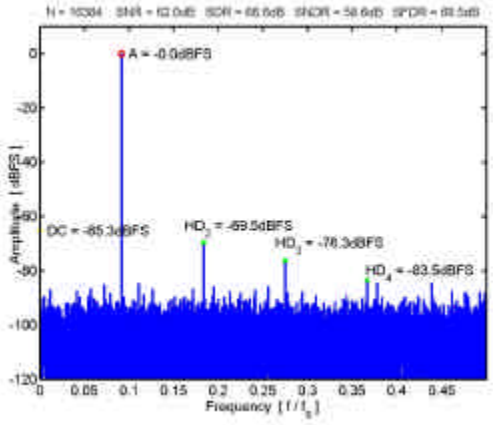


10bit ADC & T/τ = 10
$V_{DD} - V_{th}$ = 4V V_{FS} = 1V

- Effect of lower supply voltage on sampling distortion
  → HD3 increases by $(V_{DD1}/V_{DD2})^2$
  →HD2 increases by (V_{DD1}/V_{DD2})

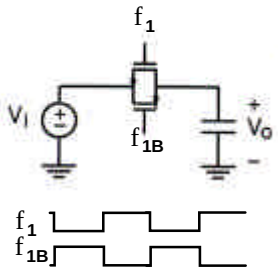
Sampling Distortion

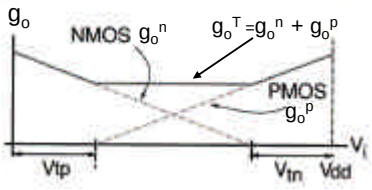
- SFDR is sensitive to sampling distortion to improve distortion
  - Larger VDD
  - Higher sampling bandwidth
- Solutions:
  - Overdesign→ Larger switches
    → Increased switch charge injection
    → Increased nonlinear S &D junction C
  - Maximize VDD/VFS
    →Decreased dynamic range if VDD const.
  - Complementary switch
  - Constant & max. V_{GS} ? f(V_{in})



10bit ADC T/τ = **20**
$V_{DD} - V_{th}$ = 2V V_{FS} = 1V

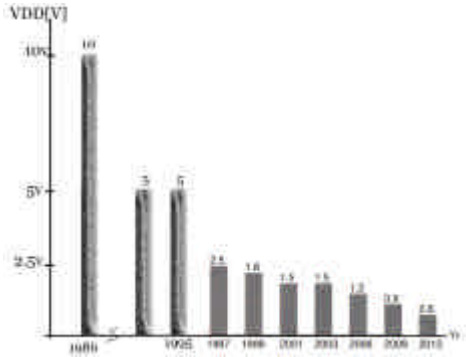
Complementary Switch





•Complementary n & p switch advantages:
- •Increases the overall conductance
- •Linearize the switch conductance for the range Vtp< Vin <Vdd-Vtn

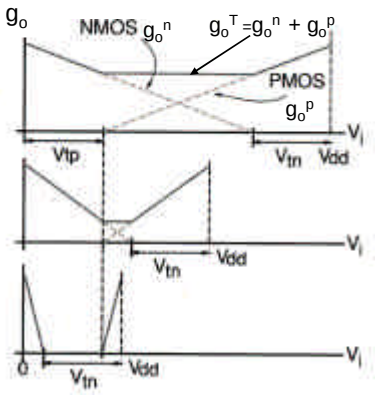
Complementary Switch Issues
Supply Voltage Evolution

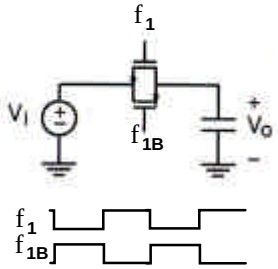


•Supply voltage scales down with technology scaling
•Threshold voltages do not scale accordingly

Ref: A. Abo et al, "A 1.5-V, 10-bit, 14.3-MS/s CMOS Pipeline Analog-to-Digital Converter," JSSC May 1999, pp. 599.

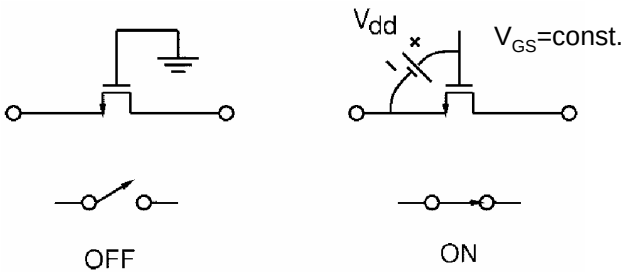
Complementary Switch
Effect of Supply Voltage Scaling





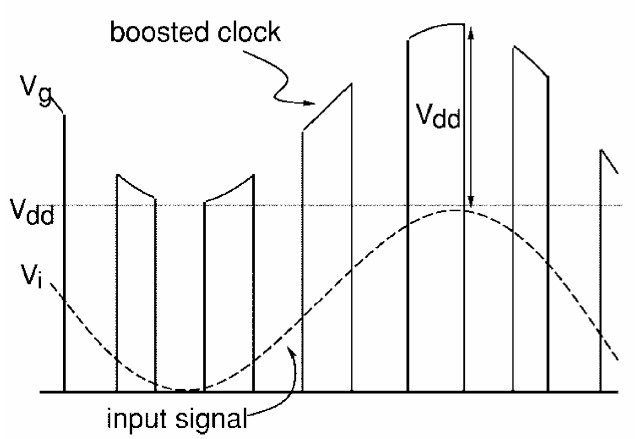
•As supply voltage scales down input voltage range for constant g_o shrinks
→ Complementary switch not effective when V_{DD} becomes comparable to V_{th}

Boosted & Constant V_{GS} Sampling

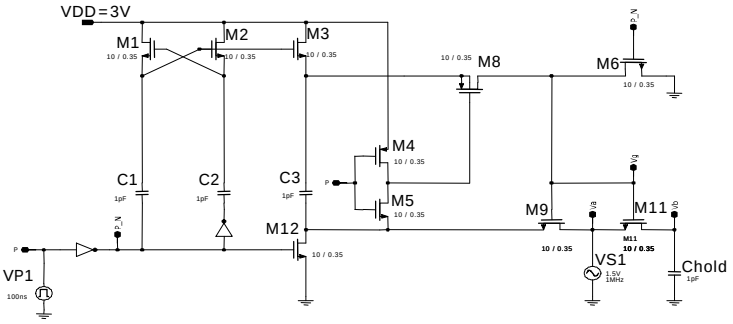


- Increase gate overdrive voltage as much as possible + keep V_{GS} constant
  - ➢Switch overdrive voltage is independent of signal level
  - ➢Error from finite R_{ON} is linear (to first order)
  - ➢Lower R_{on} achieved → lower time constant

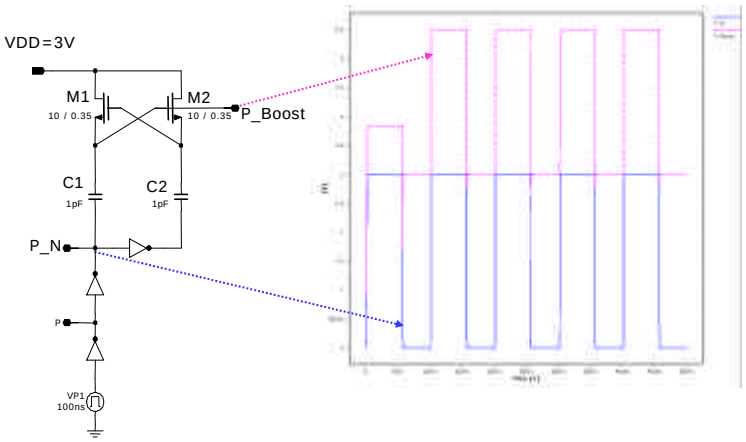
Constant V_{GS} Sampling



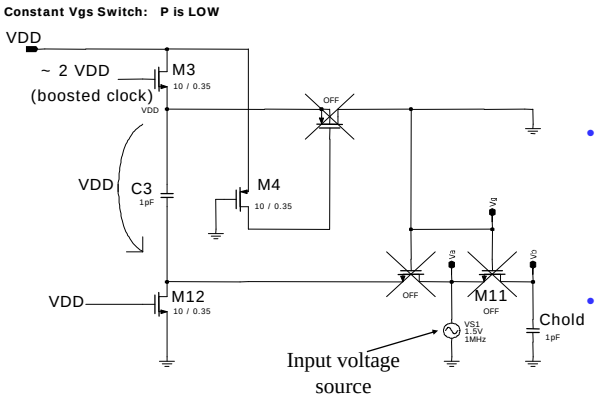
Constant V_{GS} Sampling Circuit



Clock Voltage Doubler



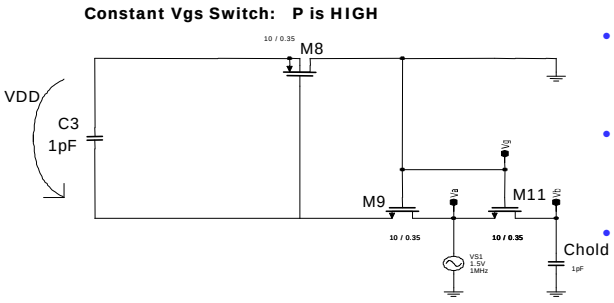
Constant V_{GS} Sampler: Φ LOW



- Sampling switch M11 is OFF

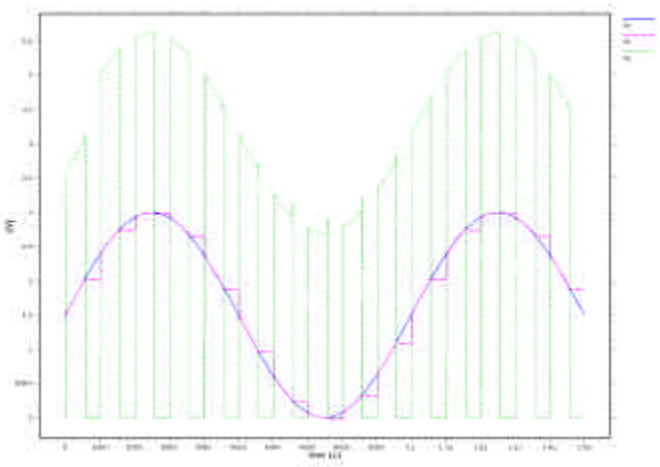
- C3 charged to VDD

Constant V_{GS} Sampler: Φ HIGH

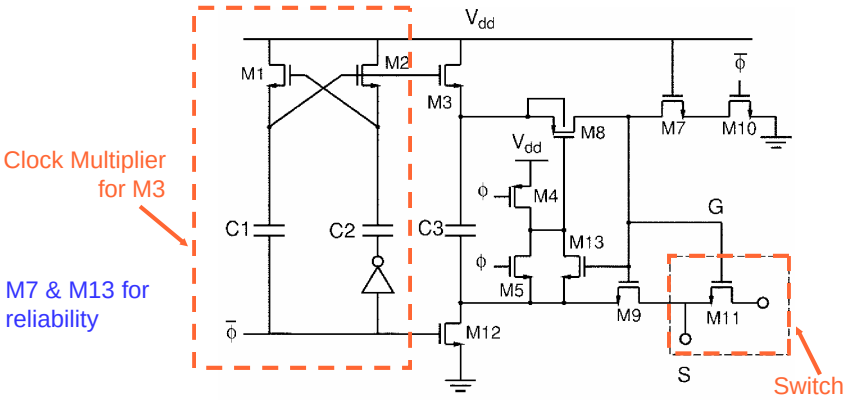


- C3 previously charged to VDD
- M8 & M9 are on: C3 across G-S of M11
- M11 on with constant VGS = VDD

Constant V_{GS} Sampling

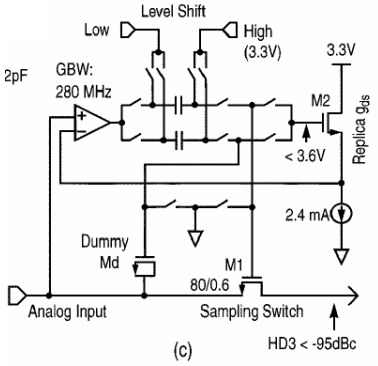


Complete Circuit



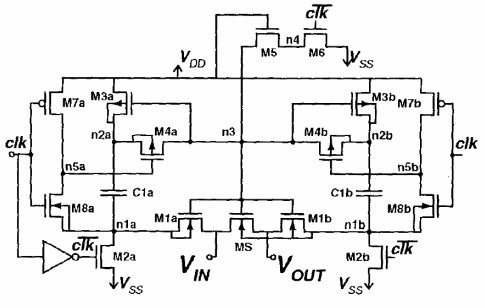
Ref: A. Abo et al, "A 1.5-V, 10-bit, 14.3-MS/s CMOS Pipeline Analog-to-Digital Converter," JSSC May 1999, pp. 599.

Advanced Clock Boosting



[H. Pan et al., "A 3.3-V 12-b 50-MS/s A/D converter in 0.6um CMOS with over 80-dB SFDR," *IEEE J. Solid-State Circuits*, pp. 1769-1780, Dec. 2000]

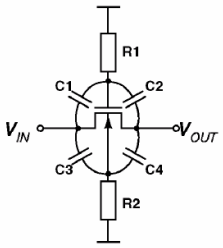
Advanced Clock Boosting



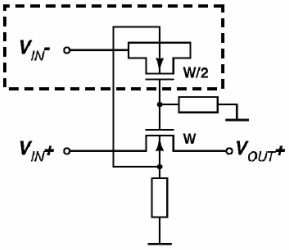
[M. Waltari et al., "A self-calibrated pipeline ADC with 200MHz IF-sampling frontend," ISSCC 2002, Dig. Techn. Papers, pp. 314.]

- Gate tracks *average* of input and output, reduces effect of I·R drop at high frequencies
- Bulk also tracks signal ⇒ reduced body effect (technology used allows connecting bulk to S)
- SFDR = 76.5dB at f_{in}=200MHz (measured)

Switch Off-Mode Feedthrough Cancellation



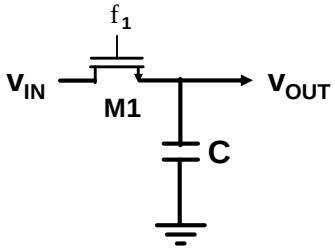
High-pass feedthrough paths past an open switch



Feedthrough cancellation with a dummy switch

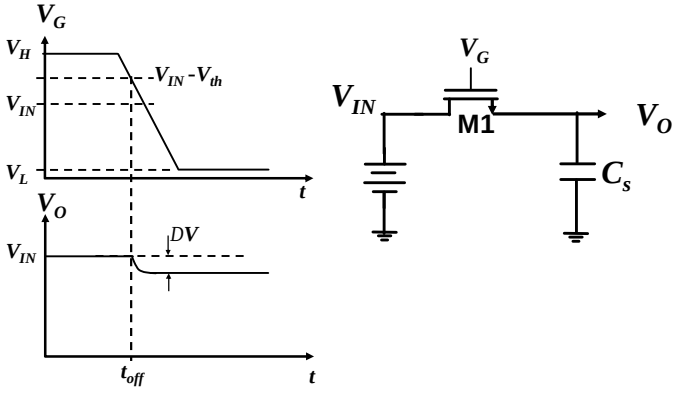
Ref: [M. Waltari et al., "A self-calibrated pipeline ADC with 200MHz IF-sampling frontend," ISSCC 2002, Dig. Techn. Papers, pp. 314.]

Practical Sampling



- $R_{sw} = f(V_{in})$ → distortion
- Switch charge injection

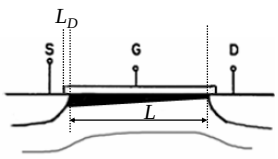
Sampling Switch Charge Injection



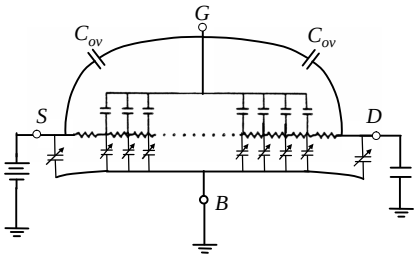
- First assume V_{IN} is a DC voltage
- When switch turns off → offset voltage induced on C_s
- Why?

Sampling
Switch Charge Injection

MOS xtor operating in triode region
Cross section view

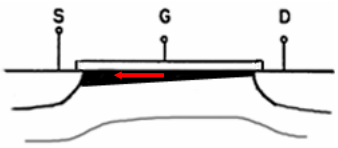


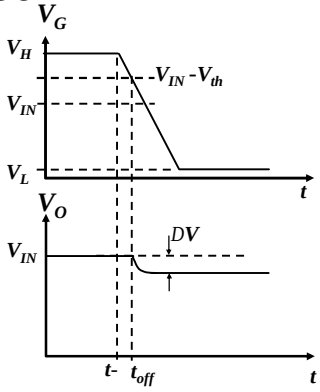
Distributed channel resistance & gate & junction capacitances



- Channel → distributed RC network
- Channel to substrate junction capacitance → distributed & variable
- Over-lap capacitance $C_{ov} = L_D x W x C_{ox}$ associated with GS & GD overlap

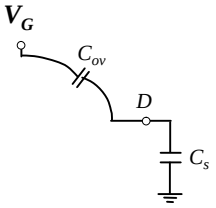
Switch Charge Injection
Slow Clock

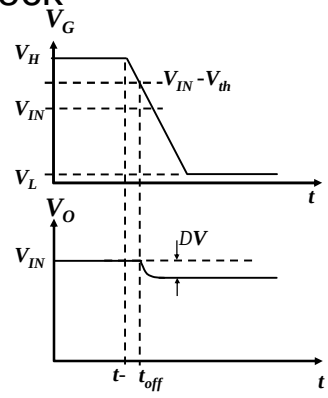




- Since clock fall time >> device speed
  → During the period (t- to t_{off}) current in channel discharges channel charge into source
- Only source of error → Charge transfer from C_{ov} into C_s

Switch Charge Injection
Slow Clock





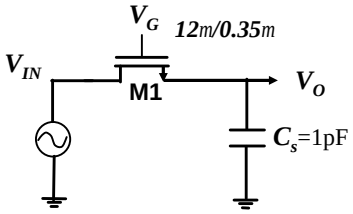
$$\Delta V = -\frac{C_{ov}}{C_{ov}+C_s}(V_i + V_{th} - V_L)$$

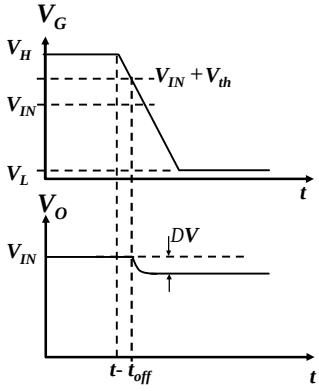
$$\approx -\frac{C_{ov}}{C_s}(V_i + V_{th} - V_L)$$

$$V_o = V_i(1+e) + V_{os}$$

$$where\ e = -\frac{C_{ov}}{C_s};\ V_{os} = -\frac{C_{ov}}{C_s}(V_{th} - V_L)$$

Switch Charge Injection
Slow Clock- Example



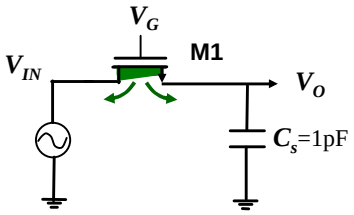


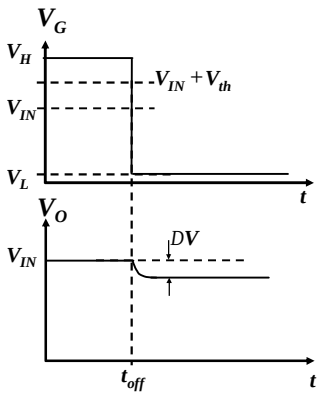
$$C_{ov} = 0.3fF/m\ \ C_{ox} = 5fF/m^2\ \ V_{th} = 0.5V$$

$$e = -\frac{C_{ov}}{C_s} = -\frac{12mx0.3fF/m}{1pF} = -.36\% \rightarrow 7-bit$$

$$V_{os} = -\frac{C_{ov}}{C_s}(V_{th} - V_L) = -1.8mV$$

Switch Charge Injection
Fast Clock





- Sudden gate voltage drop → no gate voltage to establish current in channel → channel charge has no choice but to escape out towards S & D

Switch Charge Injection
Fast Clock

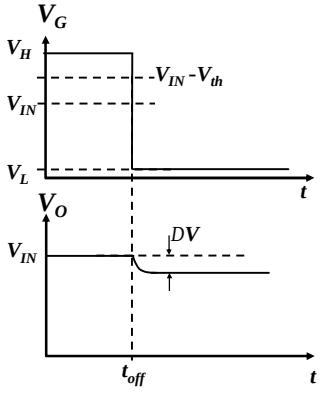
$$\Delta V_o = -\frac{C_{ov}}{C_{ov}+C_s}(V_H - V_L) - \frac{1}{2}\times\frac{Q_{ch}}{C_s}$$

$$\approx -\frac{C_{ov}}{C_{ov}+C_s}(V_H - V_L) - \frac{1}{2}\times\frac{WC_{ox}(L-2L_D)\left((V_H - V_i - V_{th})\right)}{C_s}$$

$$V_o = V_i(1+e) + V_{os}$$

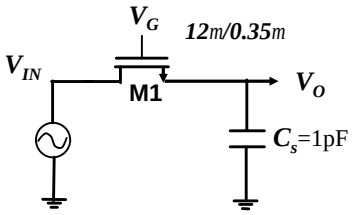
$$where\ e = -\frac{1}{2}\times\frac{WC_{ox}L}{C_s}$$

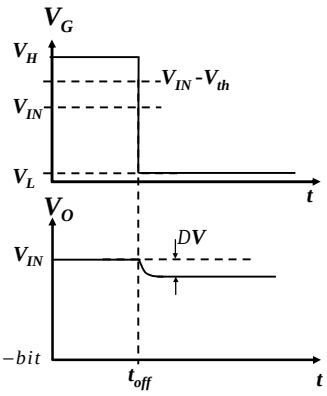
$$V_{os} = -\frac{C_{ov}}{C_s}(V_H - V_L) - \frac{1}{2}\times\frac{WC_{ox}L(V_H - V_{th})}{C_s}$$



- Assumption → channel charge divided between S & D 50% & 50%
- Source of error → channel charge transfer + charge transfer from C_{ov} into C_s

Switch Charge Injection
Fast Clock- Example



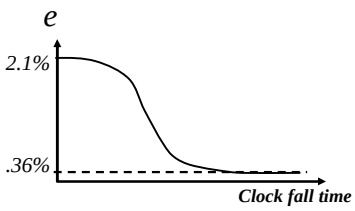


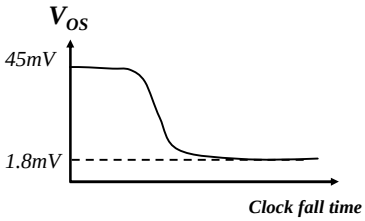
$C_{ov}=0.3fF/m \;\; C_{ox}=5fF/m^2 \;\; V_{th}=0.5V \; V_{DD}=3V$

$$e=-1/2\frac{WLC_{ox}}{C_s}=\frac{12mx0.35x5fF/m}{1pF}=-2.1\% \rightarrow 4.5-bit$$

$$V_{os}=-\frac{C_{ov}}{C_s}(V_H-V_L)-\frac{1}{2}\times\frac{WC_{ox}L(V_H-V_{th})}{C_s}=-9mV-26.3mV=-45.3mV$$

Switch Charge Injection





→ Both errors are a function of clock fall time, input voltage level, source impedance & sampling capacitance

Switch Charge Injection Error Reduction

- How do we reduce the error?
  →Reduce size switch?

$$t = R_{ON}C_s = \frac{C_s}{\mu C_{ox}\frac{W}{L}(V_{GS}-V_{th})}$$

$$\Delta V_o = -\frac{1}{2}\frac{Q_{ch}}{C_s}$$

$$FOM = t \times \Delta V_o \approx \frac{C_s}{\mu C_{ox}\frac{W}{L}(V_{GS}-V_{th})} \times \frac{1}{2} \times \frac{WC_{ox}L((V_H - V_i - V_{th}))}{C_s}$$

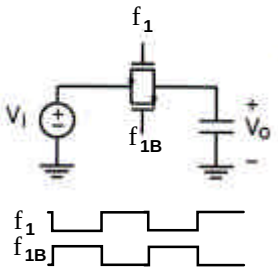
$$FOM \approx \frac{L^2}{\mu}$$

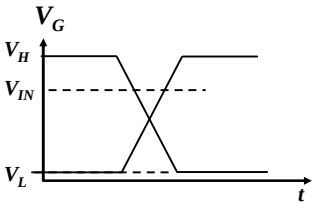
→Reducing switch size increases τ → increased distortion→ not a viable solution
→Small τ and ΔV → use minimum chanel length
→For a given technology τ x ΔV=conts.

Sampling Switch Charge Injection Summary

- Extra charge injected onto sampling capacitor @ switch device turn-off
  - Charge sharing with C_{ov}
  - Channel charge transfer
- Issues:
  - DC offset
  - Input dependant error voltage → distortion
- Solutions:
  - Complementary switch?
  - Addition of dummy switches?
  - Bottom-plate sampling?

Switch Charge Injection Complementary Switch





- In slow clock case if area of devices are equal → effect of overlap capacitor for n & p devices cancel to first order (matching n & p area)

Switch Charge Injection Complementary Switch

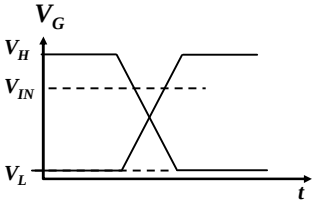
$$Q_{ch-n} = W_n C_{ox} L_n \left(V_H - V_i - |V_{th-n}|\right)$$

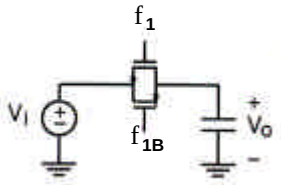
$$Q_{ch-p} = W_p C_{ox} L_p \left(V_i - VL - |V_{th-p}|\right)$$

$$\Delta V_o = \frac{1}{2}\left(\frac{Q_{ch-p}}{C_s} - \frac{Q_{ch-n}}{C_s}\right)$$

$$V_o = V_i(1+e) + V_{os}$$

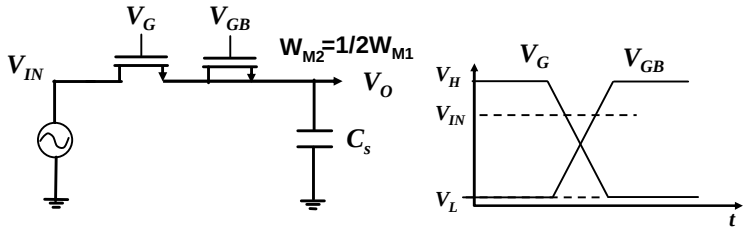
$$e = -\frac{1}{2} \times \frac{W_n C_{ox} L_n + W_p C_{ox} L_p}{C_s}$$





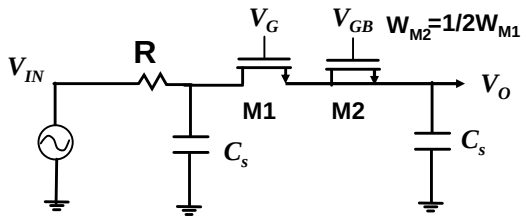
- In fast clock case
  - Offset cancelled for equal device area
  - Input voltage dependant error worse!

Switch Charge Injection Dummy Switch



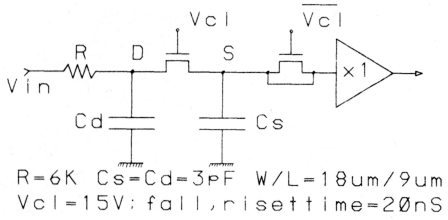
- Dummy switch same L and main switch but half W
- Main device clock goes low, dummy device goes high → dummy switch acquires same amount of channel charge main switch needs to lose
  - Effective only if exactly half of the charge transferred to M2 and good matching between clock fall/rise

Switch Charge Injection Dummy Switch



- To guarantee half of charge goes to each side→ create the same environment on both sides
  - Add C equal to sampling capacitor to the other side of the switch + add fixed resistor
- Degrades sampling bandwidth

Dummy Switch
Dummy Switch Effectiveness Test

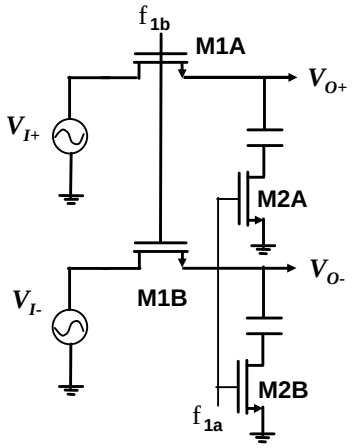


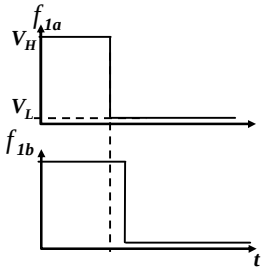
- Dummy switch → W=1/2W$_{main}$
- Note large Ls → good device area matching

Vin	UNCOMPENSATED SWITCH	COMPENSATED WITH DUMMY	BALANCED SWITCH
0v	-160mV	-45mV	6mV
5v	-105mV	-30mV	1mV
10v	-40mV	-11mV	0.5mV

Ref: L. A. BIENSTMAN et al, " An Eight-Channel 8 13it Microprocessor Compatible NMOS D/A Converter with Programmable Scaling", IEEE JSSC, VOL. SC-15, NO. 6, DECEMBER 1980

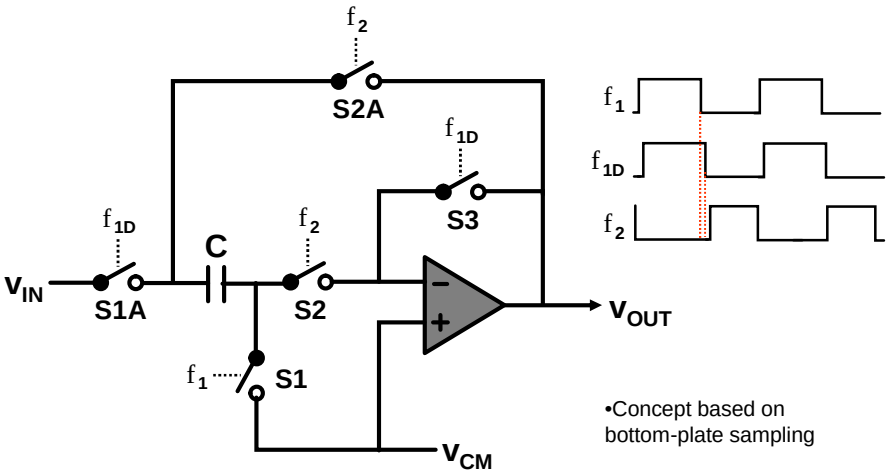
Switch Charge Injection
Bottom Plate Sampling





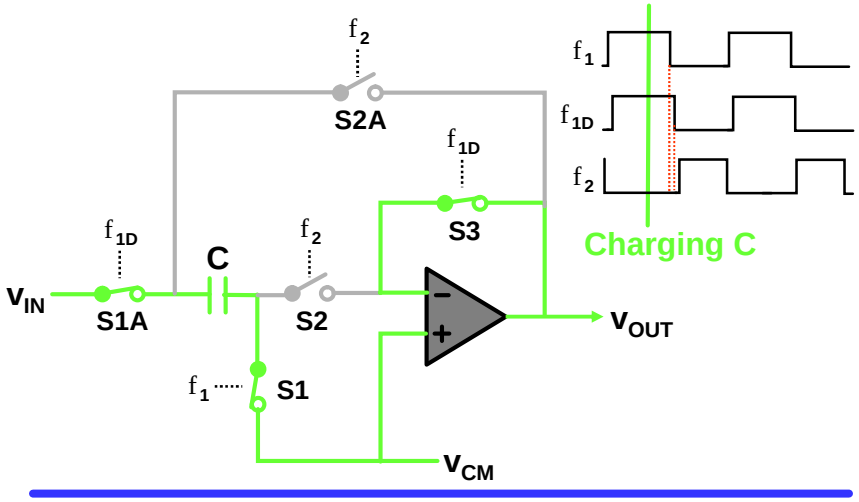
- Switches M2A@ B are opened slightly earlier compared to M1A&B
  → Injected charge by the opening or M2AB is constant & eliminated when used differentially
- Since bottom plate of C_s is open when M1A&B are opened→ no charge injected on C_s

Flip-Around T/H

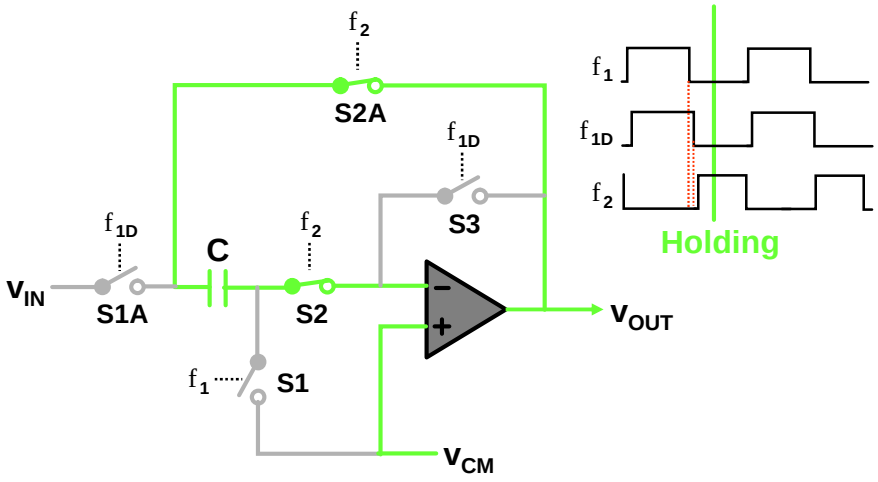


•Concept based on bottom-plate sampling

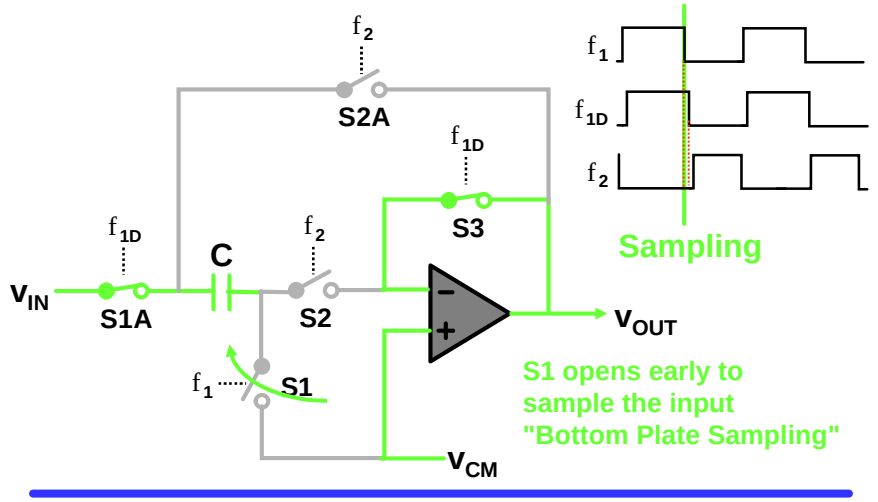
Flip-Around T/H



Flip-Around T/H



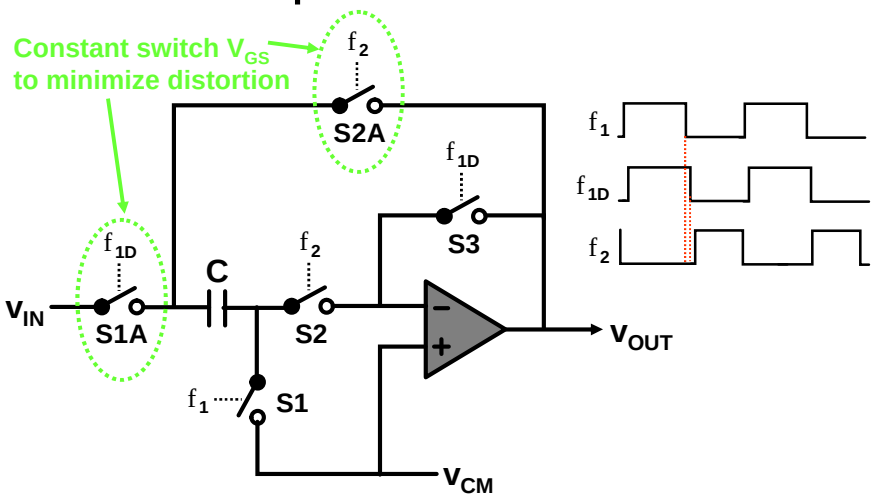
Flip-Around T/H - Timing



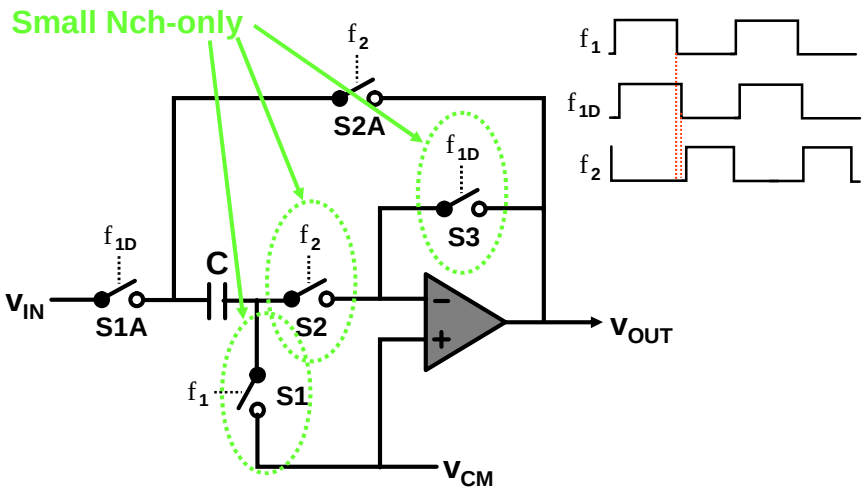
Charge Injection

- At the instant of sampling, some of the charge stored in sampling switch S1 is dumped onto C
- With "Bottom Plate Sampling", charge injection comes only from S1 and is to first-order independent of v_{IN}
  - Only a dc offset is added to the input signal
  - This dc offset can be removed with a differential architecture

Flip-Around T/H



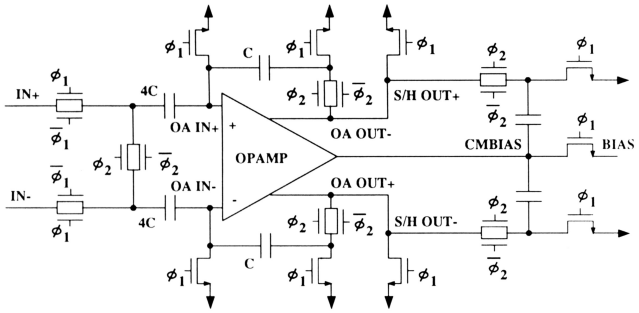
Flip-Around T/H



Flip-Around T/H

- S1 is an n-channel MOSFET
- Since it always switches the same voltage, it's on-resistance, R_{S1}, is signal-independent (to first order)
- Choosing $R_{S1} >> R_{S1A}$ minimizes the non-linear component of $R = R_{S1A} + R_{S1}$
  - S1A is a wide (much lower resistance than S1) constant V_{GS} switch
  - In practice size of S1A is limited by the (nonlinear) S/D capacitance that also adds distortion
  - If S1A's resistance is negligible, aperture delay depends only on S1 resistance
  - S1 resistance is independent of v_{IN}; hence, aperture delay is independent of v_{IN}

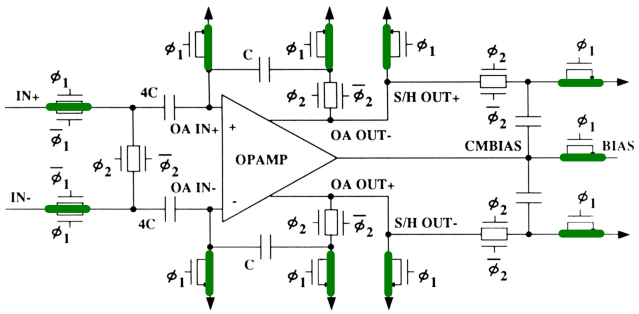
S/H Combined with Gain Stage



- Gain=4Cl/Ci=4

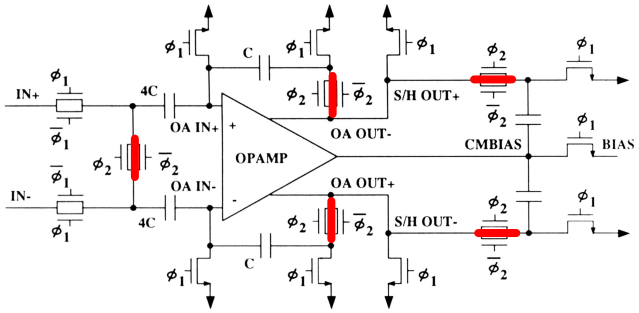
Ref: S. H. Lewis, et al., "A Pipelined 5-Msample/s 9-bit Analog-to-Digital Converter" IEEE JSSC, VOL. SC-22,NO. 6, DECEMBER 1987

S/H Combined with Gain Stage



Ref: S. H. Lewis, et al., "A Pipelined 5-Msample/s 9-bit Analog-to-Digital Converter" IEEE JSSC, VOL. SC-22,NO. 6, DECEMBER 1987

S/H Combined with Gain Stage



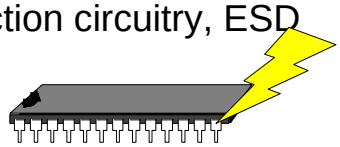
- *Gain=4C/C=4*

Ref: S. H. Lewis, et al., "A Pipelined 5-Msample/s 9-bit Analog-to-Digital Converter" IEEE JSSC, VOL. SC-22,NO. 6, DECEMBER 1987

ESD Protection
ADC Architectures

What is ESD?

- Electrostatic discharge
- Example: Charge built up on human body while walking on carpet...
- Charged objects near or touching IC pins can discharge through on-chip devices
- Without dedicated protection circuitry, ESD events are destructive



Model and Protection Circuit

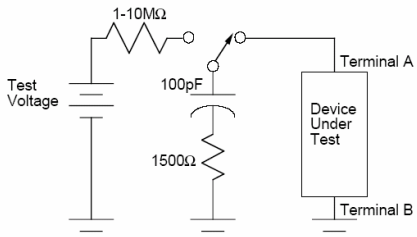
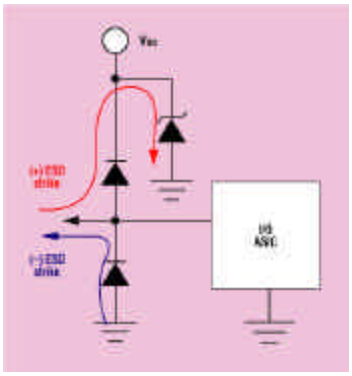


Figure 1. Human Body Model for ESD testing.

[http://www.idt.com/docs/AN_123.pdf]



[http://www.ce-mag.com/archive/03/ARG/dunnihoo.html]

Equivalent Circuit

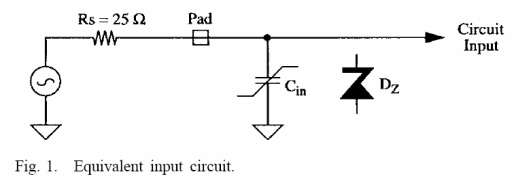
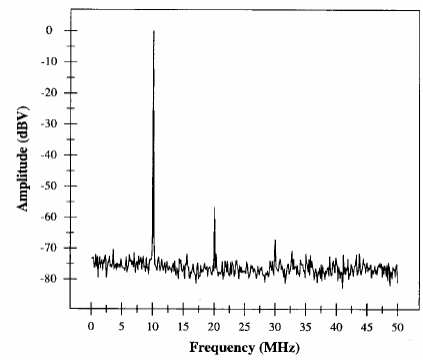


Fig. 1. Equivalent input circuit.

[I. E. Opris, "Bootstrapped pad protection structure," IEEE J.Solid-State Circuits, pp. 300, Feb. 1998.]

- Nonlinear capacitance causes distortion
- Distortion increases with frequency
  - Today's converters: High frequency, low distortion!

ESD Circuit Distortion

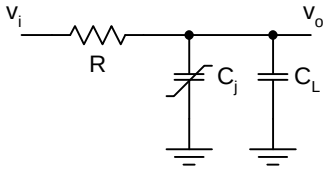


[I. E. Opris, "Bootstrapped pad protection structure," IEEE J.Solid-State Circuits, pp. 300, Feb. 1998.]

$C(V_{in})$= 2..4pF for V_{in}=2..0V

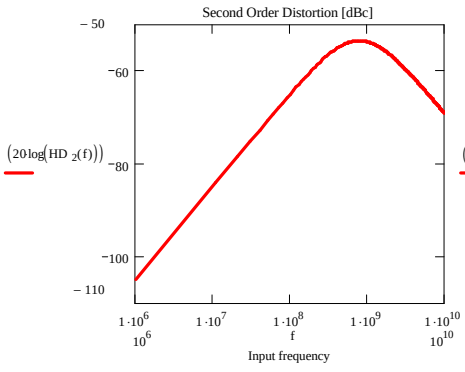
ESD Circuit Distortion

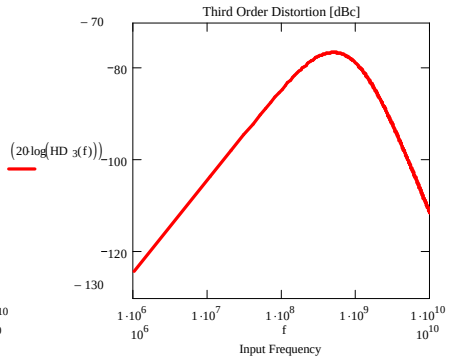
- Analysis: Volterra Series (see handout on the web)
- Example:



R=25Ω
C_{jo}=1pF
C_L=5pF
V_{ipeak}=0.5V

ESD Circuit Distortion





HD3(37.5MHz) = -92dB
HD3(100MHz) = -84dB

ESD Circuit Distortion

- Distortion from ESD circuits approaches state of-the-art ADC performance!
- If you are working on a new, record breaking ADC, better think about ESD now...
- Ref.: A. Wang, "Recent developments in ESD protection for RF IC," *Proc. DAC Conference*, Jan. 2003
- Solutions still pre-mature
- Lots of company IP