# EE247
# Lecture 16

D/A Converters
- D/A examples
  - Serial charge redistribution DAC
  - Practical aspects of current-switch DACs
  - Segmented current-switch DACs
- DAC self calibration techniques
  - Current copiers
  - Dynamic element matching

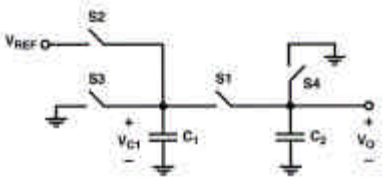
ADC Converters
- Sampling
  - Sampling switch induced distortion
  - Sampling switch charge injection



# Serial Charge Redistribution DAC

- Nominally $C_1=C_2$
- Operation sequence:
  - Discharge C1 & C2, S3& S4 closed
  - For each bit in succession beginning with LSB, $b_0$:
    - S1 open- if $b_i$=1 C1 precharge to $V_{REF}$ if $b_i$=0 to GND
    - S1 closed-S2 & S3 & S4 open- Charge sharing C1 & C2

    → ½ of precharge on C1 +½ of charge previously stored on C2→ C2

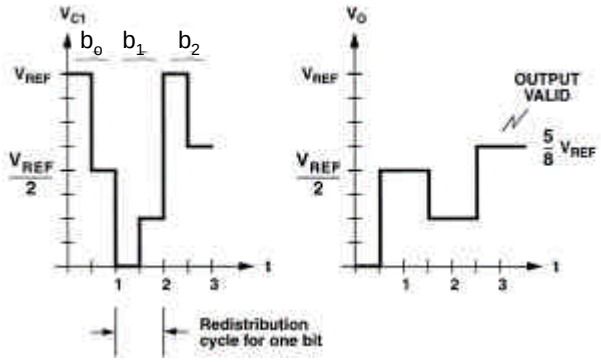



$$V_o(1) = \frac{b_N}{2}V_{REF}$$

$$V_o(2) = \frac{1}{2}\left(b_{N-1} + \frac{b_N}{2}\right)V_{REF}$$

$$V_o(N) = \left(\sum_{i=1}^{N}\frac{b_i}{2^i}\right)V_{REF}$$

# Serial Charge Redistribution DAC Example: Input Code 101

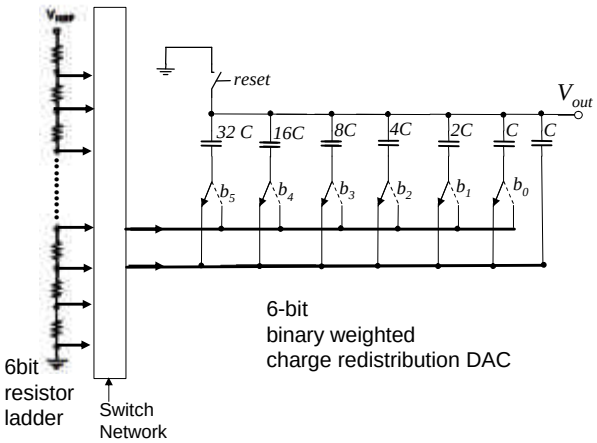



- Example input code 101→ output 5/8 $V_{REF}$
- Very small area
- N redistribution cycles for N-bits conversion



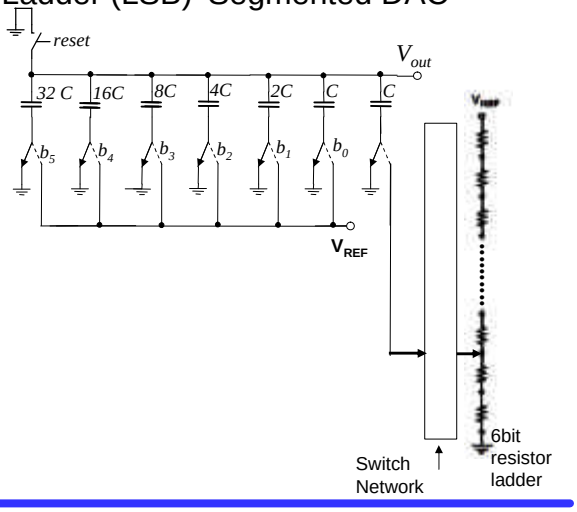
# Resistor Ladder (MSB) & Binary Weighted Charge Redistribution(LSB) Segmented DAC

- Example: 12bit DAC
  - 6-bit MSB DAC→ R string
  - 6-bit LSB DAC → binary weighted charge redistribution
- Complexity lower than full R string
  - Full R string→ 4096 resistors
  - Segmented → 64 R + 7 Cs (65 unit caps)



# Binary Weighted Charge Redistribution(MSB) & Resistor Ladder (LSB) Segmented DAC

- Homework 6:
- Compare sensitivity of these two segmented DACs to component mismatches

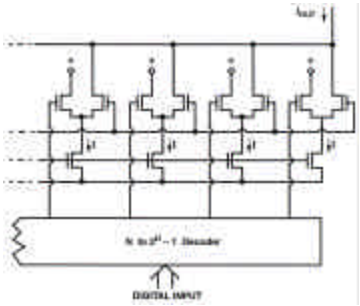





# Practical Aspects Current-Switched DACs

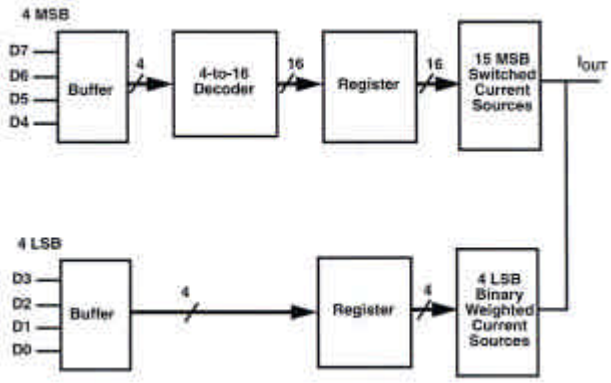
- Unit element DACs ensure monotonicity by turning on equal-weighted current sources in succession
- Typically current switching performed by differential pairs
- Based on the code only one of the diff. pair devices are on→ device mismatch not an issue
- Issue: While binary weighted DAC can use the incoming binary digital code directly, unit element requires
  - → N to ($2^N$-1) decoder

| Binary | Thermometer |
|---|---|
| 000 | 0000000 |
| 001 | 0000001 |
| 010 | 0000011 |
| 011 | 0000111 |
| 100 | 0001111 |
| 101 | 0011111 |
| 110 | 0111111 |
| 111 | 1111111 |



# Segmented Current-Switched DAC

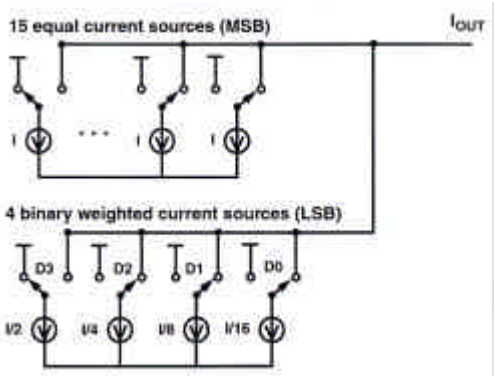
- 4-bit MSB Unit element DAC + 4-bit binary weighted DAC
- Note: 4-bit MSB DAC requires extra 4-to-16 bit decoder
- Digital code for both DACs stored in a register





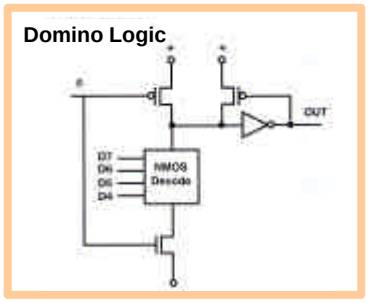

# Segmented Current-Switched DAC Cont'd

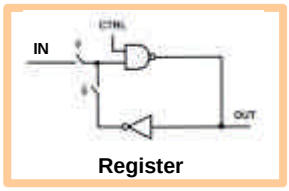
- 4-bit MSB Unit element DAC + 4-bit binary weighted DAC
- Note: 4-bit MSB DAC requires extra 4-to-16 bit decoder
- Digital code for both DACs stored in a register



# Segmented Current-Switched DAC Cont'd

- MSB Decoder
  - → Domino logic
  - → Example: D4,5,6,7=1 Out=1
- Register
  - → Latched NAND gate:
  - → CTRL=1 OUT=INB

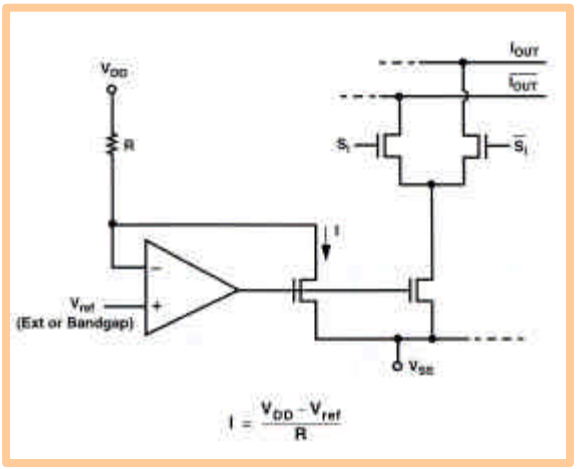




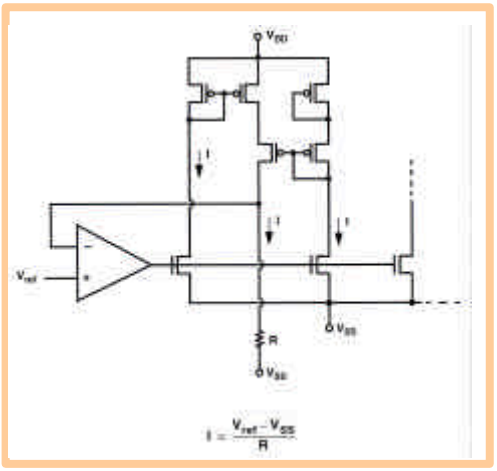

# Segmented Current-Switched DAC Reference Current Considerations

- $I_{ref}$ is referenced to $V_{DD}$
  - → Problem: Reference current varies with supply voltage



# Segmented Current-Switched DAC Reference Current Considerations

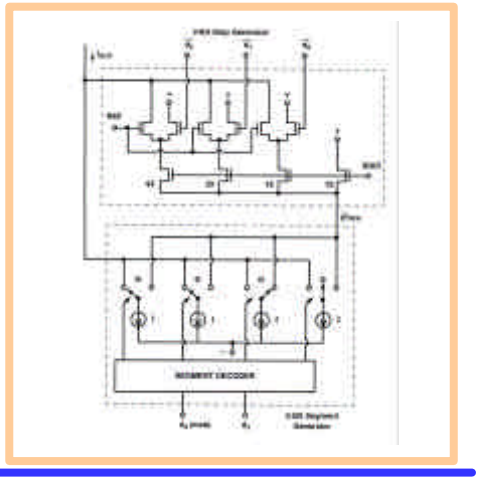
- $I_{ref}$ is referenced to $V_{ss}$→GND






# Segmented Current-Switched DAC Considerations

- Example: 2-bit MSB Unit element DAC + 3-bit binary weighted DAC
- To ensure monotonicity at the MSB→ LSB transition: First OFF MSB current source is routed to LSB current generator



IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 24, NO. 6, DECEMBER 1989



# A Self-Calibration Technique for Monolithic High-Resolution D/A Converters

D. WOUTER J. GROENEVELD, HANS J. SCHOUWENAARS, SENIOR MEMBER, IEEE, HENK A. H. TERMEER, AND CORNELIS A. A. BASTIAANSEN

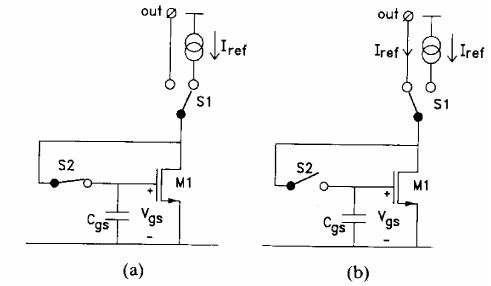
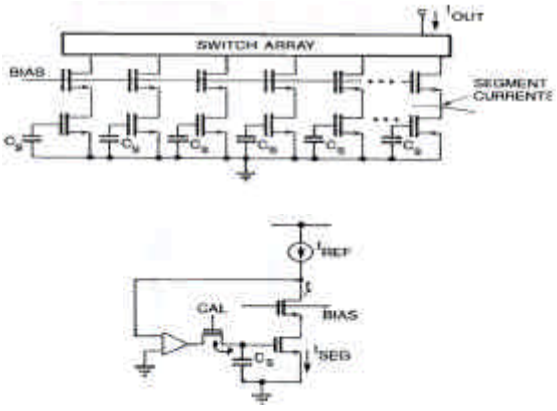
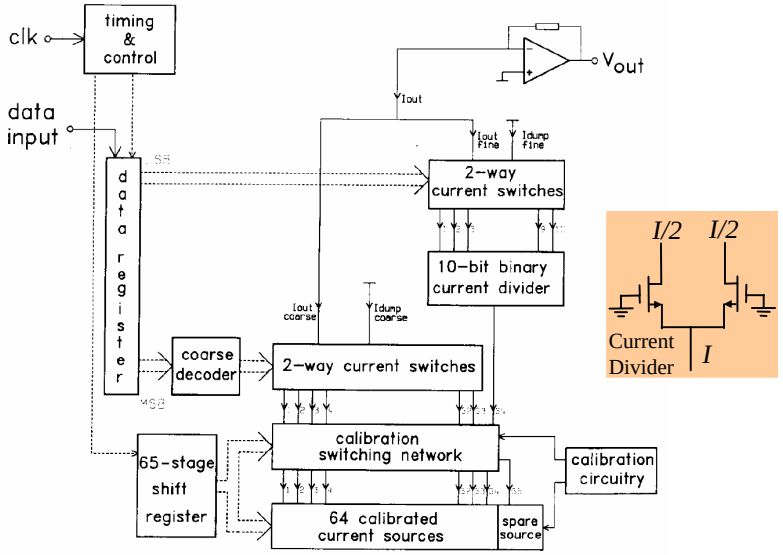



Fig. 2. Calibration principle. (a) Calibration. (b) Operation.

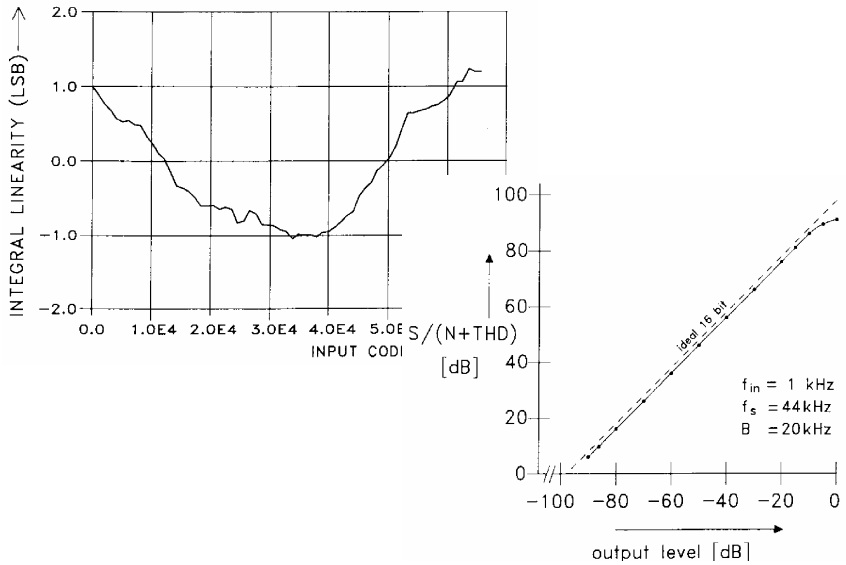


# Current Source Replica Self-Calibration




clk
timing & control
data input
data register
MSB
LSB
Vout
Iout
Iout fine
Idump fine
2-way current switches
10-bit binary current divider
Iout coarse
Idump coarse
coarse decoder
2-way current switches
calibration switching network
calibration circuitry
65-stage shift register
64 calibrated current sources
spare source
I/2
I/2
Current Divider
I



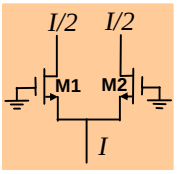

INTEGRAL LINEARITY (LSB)
2.0
1.0
0.0
-1.0
-2.0
0.0
1.0E4
2.0E4
3.0E4
4.0E4
5.0E
INPUT CODI
S/(N+THD) [dB]
100
80
60
40
20
0
-100
-80
-60
-40
-20
0
ideal 16 bit
fin = 1 kHz
fs = 44kHz
B = 20kHz
output level [dB]

# Current Divider

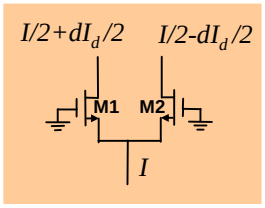
$$I_d = \frac{I_{d1} + I_{d2}}{2}$$

$$\frac{dI_d}{I_d} = \frac{I_{d1} - I_{d2}}{I_d}$$

$$\frac{dI_d}{I_d} = \frac{2}{V_{GS} - V_{th}} \times \left[ \left( \frac{d W/L}{W/L} \right) + dV_{th} \right]$$




Ideal Current Divider




Real Current Divider
M1& M2 mismatched

→Problem: Device mismatch could severely limit DAC accuracy



IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. SC-11, NO. 6, DECEMBER 1976 795

## Dynamic Element Matching for High-Accuracy Monolithic D/A Converters

RUDY J. VAN DE PLASSCHE

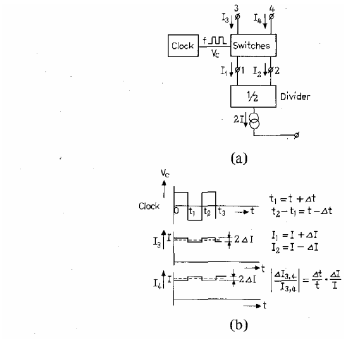



Fig. 2. (a) New current divider schematic diagram. (b) Time dependence of various currents in the new divider.

# Dynamic Element Matching

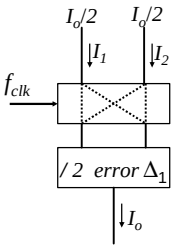
During $\Phi_1$

$$I_1^{(1)} = \tfrac{1}{2} I_o (1+\Delta_1)$$
$$I_2^{(1)} = \tfrac{1}{2} I_o (1-\Delta_1)$$

During $\Phi_2$

$$I_1^{(2)} = \tfrac{1}{2} I_o (1-\Delta_1)$$
$$I_2^{(2)} = \tfrac{1}{2} I_o (1+\Delta_1)$$

$$\langle I_2 \rangle = \frac{I_2^{(1)} + I_2^{(2)}}{2}$$
$$= \frac{I_o}{2} \frac{(1-\Delta_1)+(1+\Delta_1)}{2}$$
$$= \frac{I_o}{2}$$





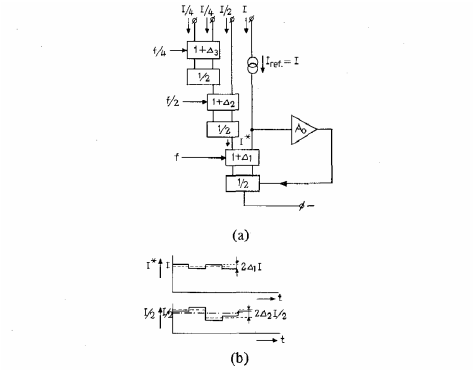
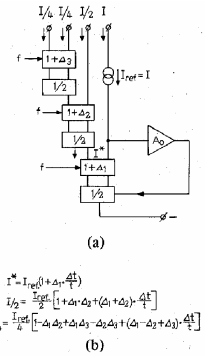




Fig. 4. (a) Binary weighted current network using different switching frequencies. (b) Time dependence of currents flowing in the first and second divider stage.




(a) Binary weighted current network with equal switching frequency. (b) Error analysis results.

# Dynamic Element Matching

During $\Phi_1$

$$I_1^{(1)} = \tfrac{1}{2} I_o (1+\Delta_1)$$
$$I_2^{(1)} = \tfrac{1}{2} I_o (1-\Delta_1)$$

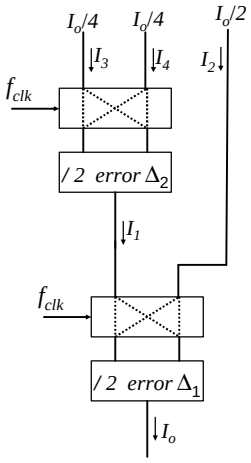
$$I_3^{(1)} = \tfrac{1}{2} I_1^{(1)} (1+\Delta_2)$$
$$= \tfrac{1}{4} I_o (1+\Delta_1)(1+\Delta_2)$$

During $\Phi_2$

$$I_1^{(2)} = \tfrac{1}{2} I_o (1-\Delta_1)$$
$$I_2^{(2)} = \tfrac{1}{2} I_o (1+\Delta_1)$$

$$I_3^{(2)} = \tfrac{1}{2} I_1^{(2)} (1-\Delta_2)$$
$$= \tfrac{1}{4} I_o (1-\Delta_1)(1-\Delta_2)$$

$$\langle I_3 \rangle = \frac{I_3^{(1)} + I_3^{(2)}}{2}$$
$$= \frac{I_o}{4} \frac{(1+\Delta_1)(1+\Delta_2) + (1-\Delta_1)(1-\Delta_2)}{2}$$
$$= \frac{I_o}{4} (1+\Delta_1\Delta_2)$$




E.g. $\Delta_1 = \Delta_2 = 1\%$ → matching error is $(1\%)^2 = 0.01\%$



# Summary
# D/A Converter

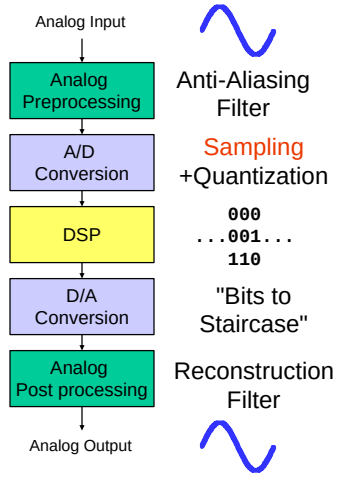
- D/A architecture
  - Unit element – complexity proportional to $2^B$- excellent DNL
  - Binary weighted- complexity proportional to B- poor DNL
  - Segmented- unit element MSB + binary weighted LSB→ complexity proportional $(2^{B1}-1) + B_2$ – DNL compromise between the two
- Static performance
  - Component matching
- Dynamic performance
  - Glitches
- DAC improvement techniques
  - Symmetrical switching rather than sequential switching
  - Current source self calibration
  - Dynamic element matching

# MOS Sampling Circuits



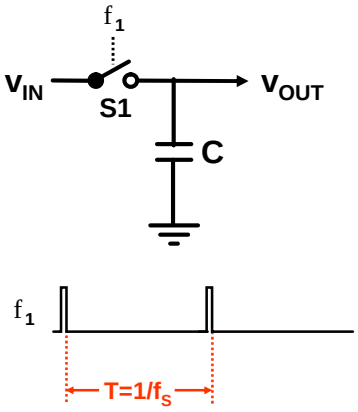
# Re-Cap

- How can we build circuits that "sample"



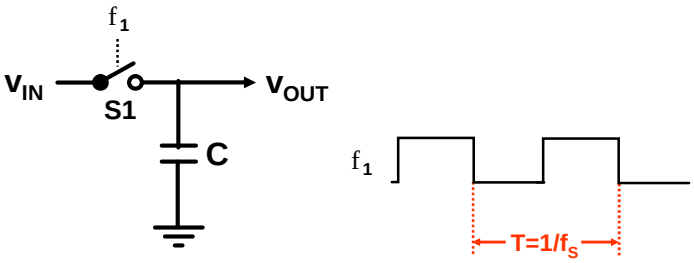
# Ideal Sampling

- In an ideal world, zero resistance sampling switches would close for the briefest instant to sample a continuous voltage $v_{IN}$ onto the capacitor C
- Not realizable!



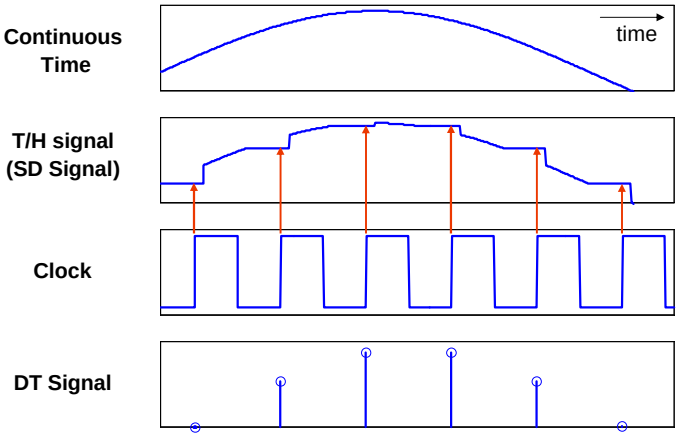



# Ideal T/H Sampling



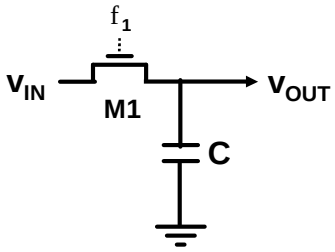

- $V_{out}$ tracks input when switch is closed
- Grab *exact* value of $V_{in}$ when switch opens
- "Track and Hold" (T/H)

# Ideal T/H Sampling






# Practical Sampling




- kT/C noise
- Finite $R_{sw}$ → limited bandwidth
- $R_{sw} = f(V_{in})$ → distortion
- Switch charge injection
- Clock jitter

# kT/C Noise

$$\frac{k_B T}{C} \le \frac{\Delta^2}{12}$$

$$C \ge 12 k_B T \left( \frac{2^B - 1}{V_{FS}} \right)^2$$

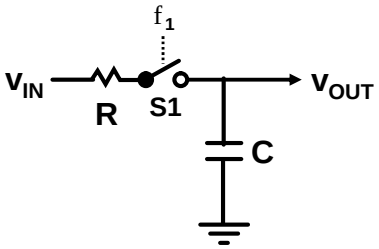
In high resolution ADCs kT/C noise usually dominates overall error (power dissipation considerations).

| B | $C_{min}$ ($V_{FS}$ = 1V) |
|---|---|
| 8 | 0.003 pF |
| 12 | 0.8 pF |
| 14 | 13 pF |
| 16 | 206 pF |
| 20 | 52,800 pF |



# Acquisition Bandwidth

- The resistance R of switch S1 turns the sampling network into a lowpass filter with risetime $= RC = t$
- Assuming $V_{in}$ is constant during the sampling period and C is initially discharged




$$v_{out}(t) = v_{in}\left(1 - e^{-t/t}\right)$$

## Switch On-Resistance

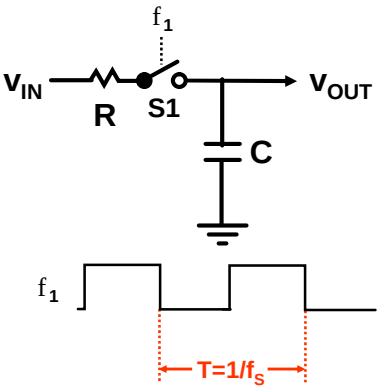
$$V_{in} - V_{out}\left(t = \frac{1}{2f_s}\right) << \Delta$$

$$V_{in} e^{-1/2 f_s t} << \Delta$$

Worst Case: $V_{in} = V_{FS}$

$$t << -\frac{T}{2}\frac{1}{\ln\left(2^B - 1\right)}$$

$$R << -\frac{1}{2 f_s C}\frac{1}{\ln\left(2^B - 1\right)}$$




Example:

B = 14, C = 13pF, $f_s$ = 100MHz

T/τ >> 19.4, R << 40Ω



# Switch On-Resistance

$$I_{D(triode)} = mC_{ox}\frac{W}{L}\left(V_{GS} - V_{TH} - \frac{V_{DS}}{2}\right)V_{DS}, \qquad g_{ON} \cong \left.\frac{dI_{D(triode)}}{dV_{DS}}\right|_{V_{DS}\to 0}$$

$$g_{ON} = mC_{ox}\frac{W}{L}\left(V_{GS} - V_{th}\right) = mC_{ox}\frac{W}{L}\left(V_{DD} - V_{th} - V_{in}\right)$$

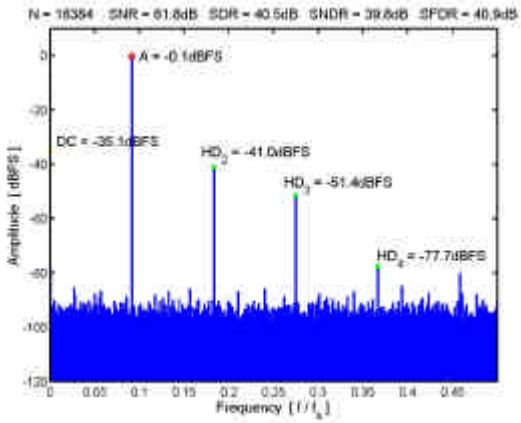
for $g_o = mC_{ox}\frac{W}{L}\left(V_{DD} - V_{th}\right)$

$$g_{ON} = g_o\left(1 - \frac{V_{in}}{V_{DD} - V_{th}}\right)$$

- Switch conductance varies with input voltage
- As the ratio of $V_{DD}/V_{th}$ gets smaller → conductance variation more pronounced
  → Technology scaling aggravates the situation

# Sampling Distortion

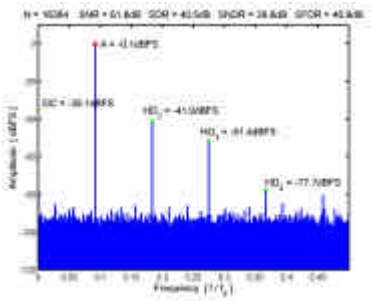
$$v_{out} = v_{in}\left(1 - e^{-\frac{T}{2t}\left(1-\frac{V_{in}}{V_{DD}-V_{th}}\right)}\right)$$



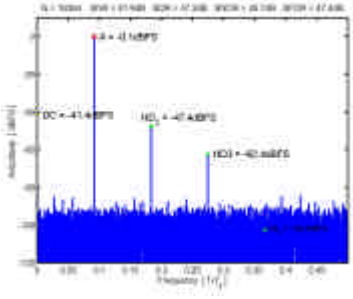

10bit ADC & T/τ = 10
$V_{DD} - V_{th}$ = 2V  $V_{FS}$ = 1V



# Sampling Distortion



10bit ADC & T/τ = 10
$V_{DD} - V_{th}$ = 2V  $V_{FS}$ = 1V



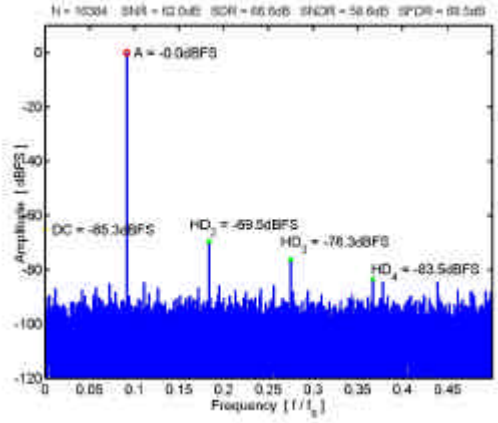
10bit ADC & T/τ = 10
$V_{DD} - V_{th}$ = 4V  $V_{FS}$ = 1V

- Effect of lower supply voltage on sampling distortion
  → HD3 increases by $(V_{DD1}/V_{DD2})^2$
  →HD2 increases by $(V_{DD1}/V_{DD2})$

# Sampling Distortion

- SFDR is very sensitive to sampling distortion
- → Decreasing τ by a factor of 2 improves HD3 by 25dB!

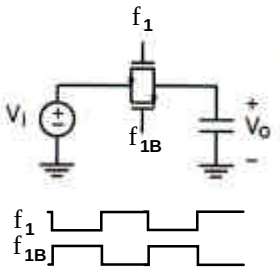
- Solutions:
  - Overdesign→ Larger switches
    → increased switch charge injection
  - Complementary switch
  - Maximize $V_{DD}/V_{FS}$
    → decreased dynamic range
  - Constant $V_{GS}$ ? $f(V_{in})$
    → …

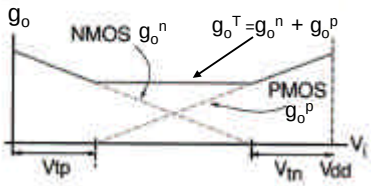



10bit ADC T/τ = **20**
$V_{DD} - V_{th}$ = 2V $V_{FS}$ = 1V



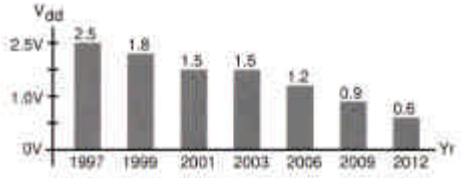
# Complementary Switch




•Complementary n & p switch advantages:
  •Increases the overall conductance
  •Linearize the switch conductance for the range Vtp< Vin <Vdd-Vtn

# Complementary Switch Issues

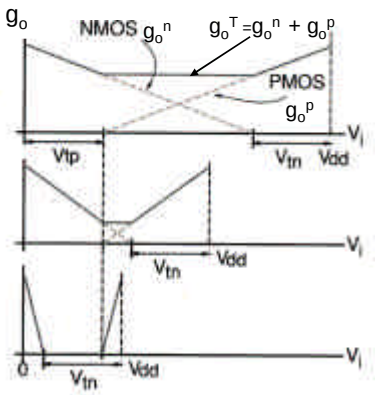


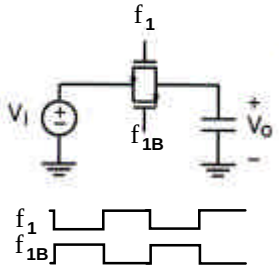

- Supply voltage scales down with technology scaling
- Threshold voltages do not scale accordingly

Ref: A. Abo et al, "A 1.5-V, 10-bit, 14.3-MS/s CMOS Pipeline Analog-to-Digital Converter," JSSC May 1999, pp. 599.



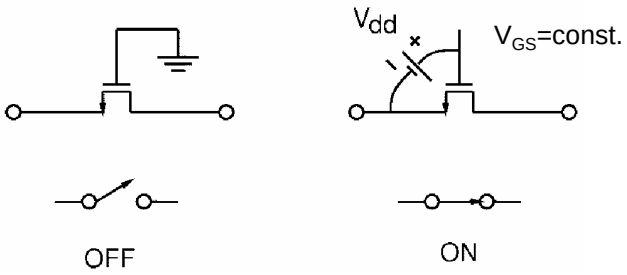
# Complementary Switch Effect of Supply Voltage Scaling




- As supply voltage scales down input voltage range for constant $g_o$ shrinks
  → Complementary switch not effective when $V_{DD}$ becomes comparable to $V_{th}$

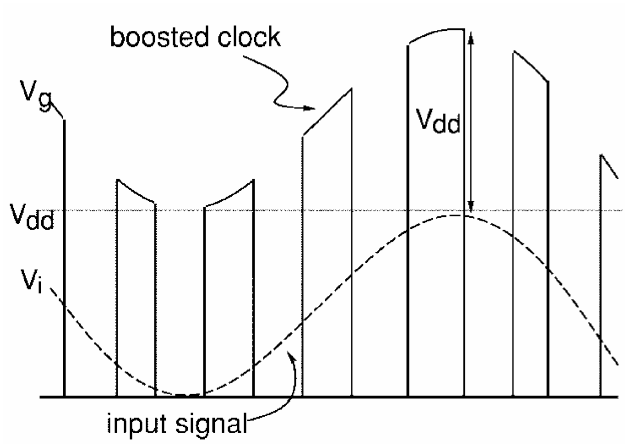
# Boosted & Constant $V_{GS}$ Sampling



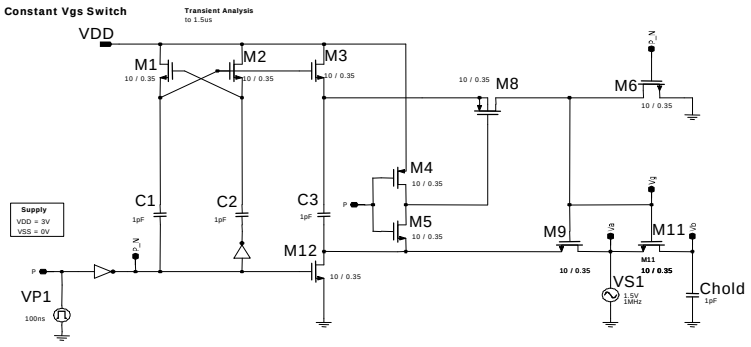

- Increase gate overdrive voltage as much as possible + keep $V_{GS}$ constant
  - Switch overdrive voltage is independent of signal level
  - Error from finite $R_{ON}$ is linear (to first order)
  - Lower $R_{on}$ achieved → lower time constant



# Constant $V_{GS}$ Sampling

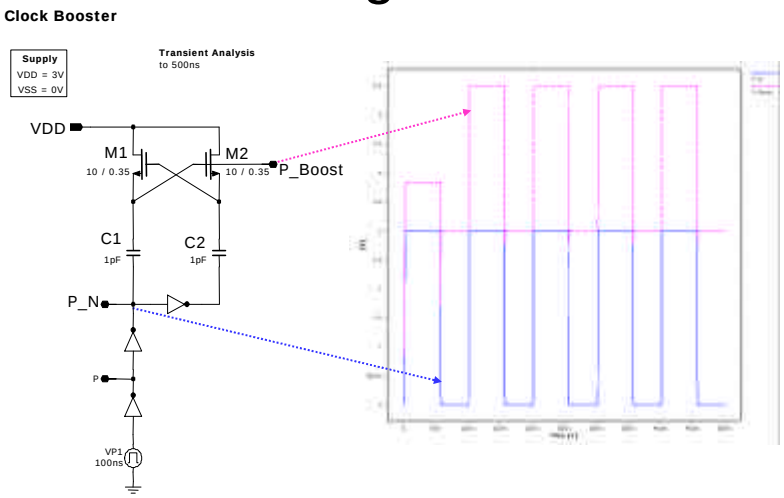


# Constant $V_{GS}$ Sampling Circuit

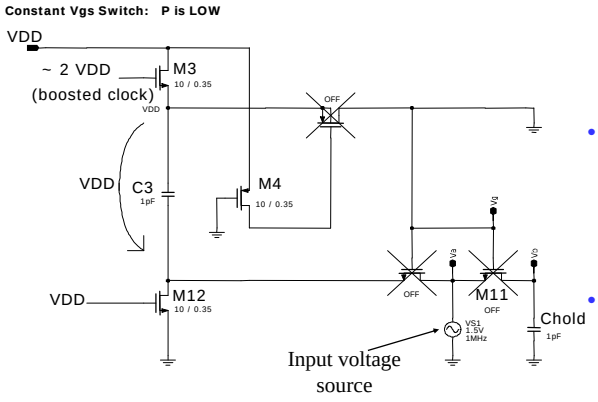





# Clock Voltage Doubler



# Constant $V_{GS}$ Sampler: $\Phi$ LOW

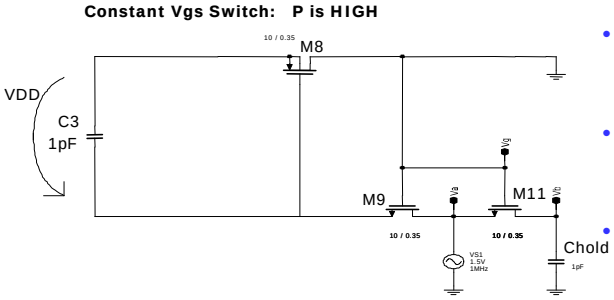



- Sampling switch M11 is OFF


- C3 charged to VDD

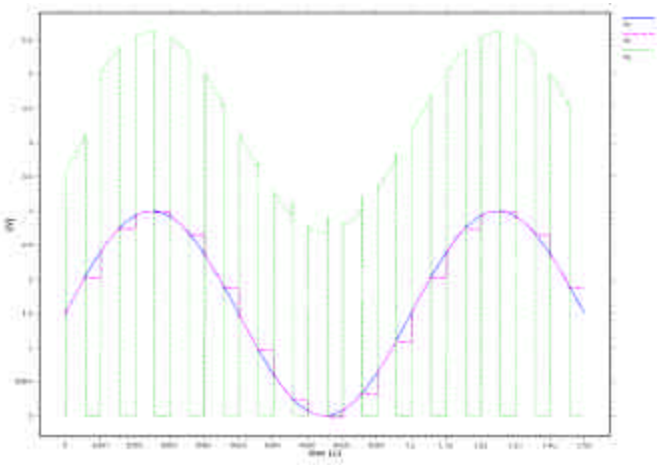


# Constant $V_{GS}$ Sampler: $\Phi$ HIGH



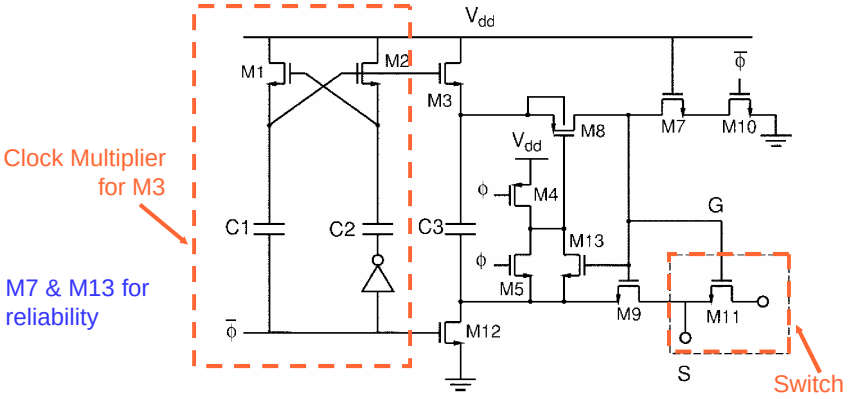

- C3 previously charged to VDD
- M8 & M9 are on: C3 across G-S of M11
- M11 on with constant VGS = VDD

# Constant $V_{GS}$ Sampling



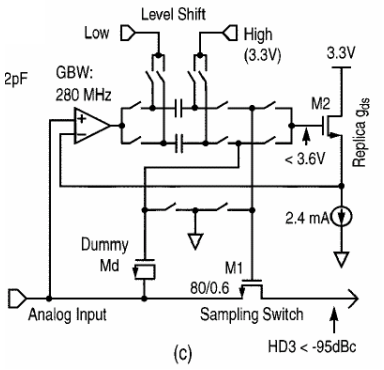


# Complete Circuit




Ref: A. Abo et al, "A 1.5-V, 10-bit, 14.3-MS/s CMOS Pipeline Analog-to-Digital Converter," JSSC May 1999, pp. 599.

# Advanced Clock Boosting

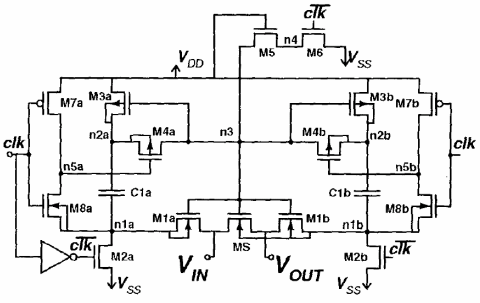



[H. Pan et al., "A 3.3-V 12-b 50-MS/s A/D converter in 0.6um CMOS with over 80-dB SFDR," *IEEE J. Solid-State Circuits*, pp. 1769-1780, Dec. 2000]

- An attempt to cancel body effect



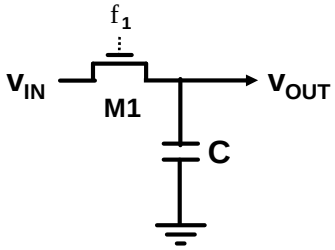
# Advanced Clock Boosting




[M. Waltari et al., "A self-calibrated pipeline ADC with 200MHz IF-sampling frontend," ISSCC 2002, Dig. Techn. Papers, pp. 314.]

- Gate tracks *average* of input and output, reduces effect of I·R drop at high frequencies
- Bulk also tracks signal ⇒ reduced body effect
- SFDR = 76.5dB at $f_{in}$=200MHz (measured)

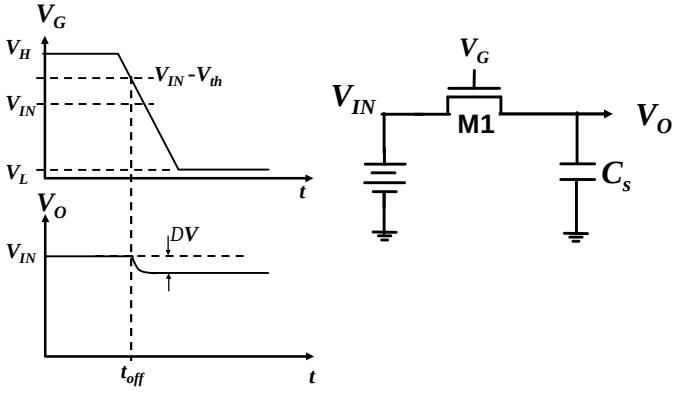
# Practical Sampling




- $R_{sw} = f(V_{in})$ → distortion
- Switch charge injection



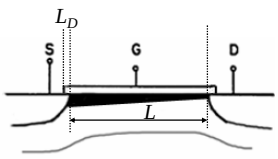
# Sampling Switch Charge Injection



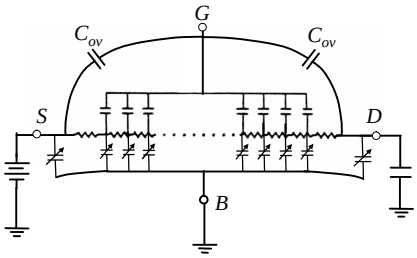

- First assume $V_{IN}$ is a DC voltage
- When switch turns off → offset voltage induced on $C_s$
- Why?

# Sampling
# Switch Charge Injection

MOS xtor operating in triode region
Cross section view



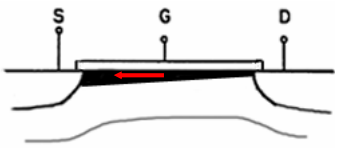

Distributed channel resistance & gate & junction capacitances

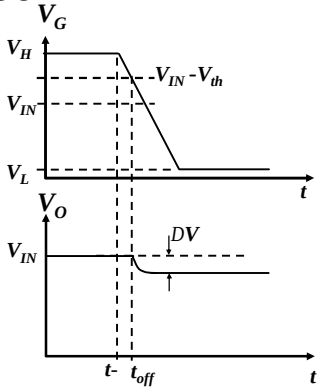



- Channel → distributed RC network
- Channel to substrate junction capacitance → distributed & variable
- Over-lap capacitance $C_{ov} = L_D x W x C_{ox}$ associated with GS & GD overlap



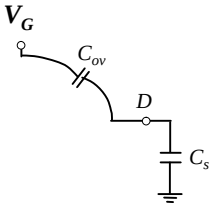
# Switch Charge Injection
# Slow Clock

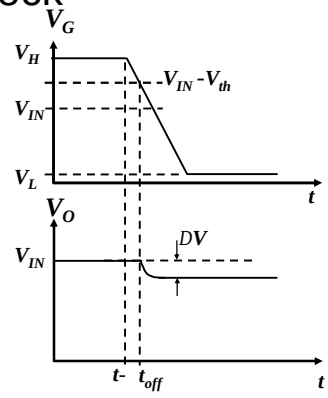



- Since clock fall time >> device speed
  → During the period ($t$- to $t_{off}$) current in channel discharges channel charge into source
- Only source of error → Charge transfer from $C_{ov}$ into $C_s$

# Switch Charge Injection
# Slow Clock




$$\Delta V = -\frac{C_{ov}}{C_{ov}+C_s}(V_i + V_{th} - V_L)$$

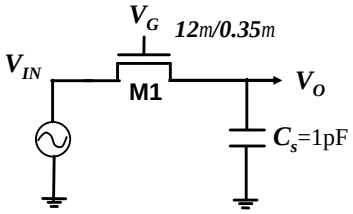
$$\approx -\frac{C_{ov}}{C_s}(V_i + V_{th} - V_L)$$

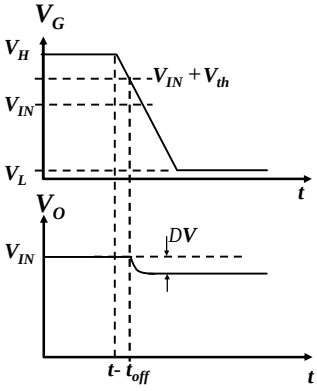
$$V_o = V_i(1+e) + V_{os}$$

$$where\ e = -\frac{C_{ov}}{C_s};\ V_{os} = -\frac{C_{ov}}{C_s}(V_{th} - V_L)$$



# Switch Charge Injection
# Slow Clock- Example



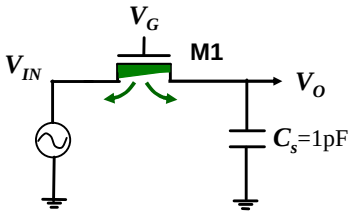



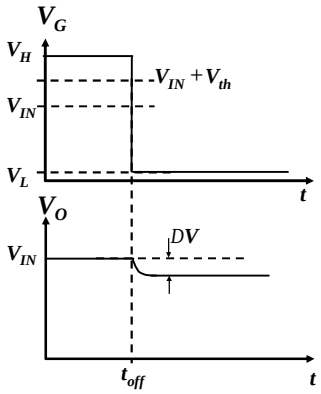

$$C_{ov} = 0.3fF/m\ \ C_{ox} = 5fF/m^2\ \ V_{th} = 0.5V$$

$$e = -\frac{C_{ov}}{C_s} = -\frac{12mx0.3fF/m}{1pF} = -.36\% \rightarrow 7-bit$$

$$V_{os} = -\frac{C_{ov}}{C_s}(V_{th} - V_L) = -1.8mV$$

# Switch Charge Injection
# Fast Clock




- Sudden gate voltage drop → no gate voltage to establish current in channel → channel charge has no choice but to escape out towards S & D



# Switch Charge Injection
# Fast Clock

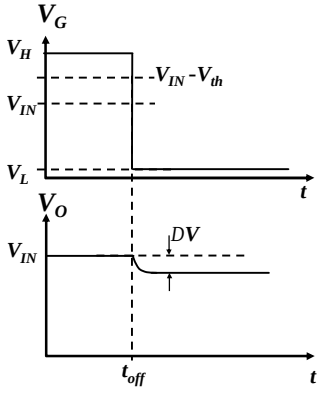
$$\Delta V_o = -\frac{C_{ov}}{C_{ov}+C_s}(V_H - V_L) - \frac{1}{2}\times\frac{Q_{ch}}{C_s}$$

$$\approx -\frac{C_{ov}}{C_{ov}+C_s}(V_H - V_L) - \frac{1}{2}\times\frac{WC_{ox}(L-2L_D)((V_H - V_i - V_{th}))}{C_s}$$

$$V_o = V_i(1+e)+V_{os}$$

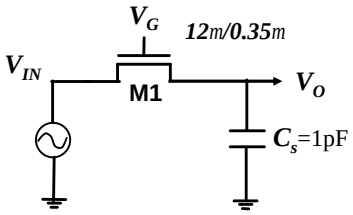
$$where\ e = -\frac{1}{2}\times\frac{WC_{ox}L}{C_s}$$

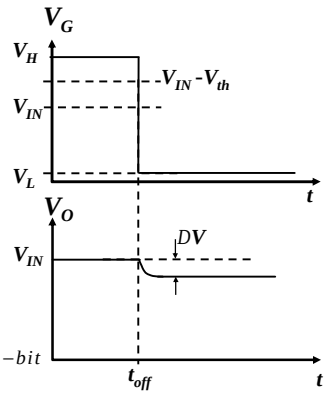
$$V_{os} = -\frac{C_{ov}}{C_s}(V_H - V_L) - \frac{1}{2}\times\frac{WC_{ox}L(V_H - V_{th})}{C_s}$$




- Assumption → channel charge divided between S & D 50% & 50%
- Source of error → channel charge transfer + charge transfer from $C_{ov}$ into $C_s$

# Switch Charge Injection
# Fast Clock- Example



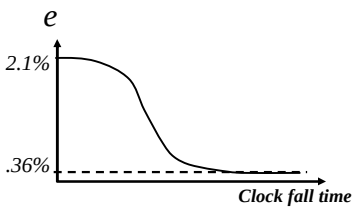

$C_{ov}=0.3fF/m \;\; C_{ox}=5fF/m^2 \;\; V_{th}=0.5V \; V_{DD}=3V$

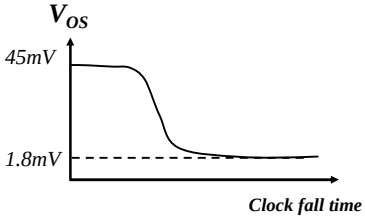
$$e=-1/2\frac{WLC_{ox}}{C_s}=\frac{12mx0.35x5fF/m}{1pF}=-2.1\% \rightarrow 4.5-bit$$

$$V_{os}=-\frac{C_{ov}}{C_s}(V_H-V_L)-\frac{1}{2}\times\frac{WC_{ox}L(V_H-V_{th})}{C_s}=-9mV-26.3mV=-45.3mV$$



# Switch Charge Injection




→ Both errors are a function of clock fall time, input voltage level, source impedance & sampling capacitance

# Switch Charge Injection Error Reduction

- How do we reduce the error?
  →Reduce size switch?

$$t = R_{ON}C_s = \frac{C_s}{\mu C_{ox}\frac{W}{L}(V_{GS}-V_{th})}$$

$$\Delta V_o = -\frac{1}{2}\frac{Q_{ch}}{C_s}$$

$$FOM = t \times \Delta V_o \approx \frac{C_s}{\mu C_{ox}\frac{W}{L}(V_{GS}-V_{th})} \times \frac{1}{2} \times \frac{WC_{ox}L((V_H - V_i - V_{th}))}{C_s}$$

$$FOM \approx \frac{L^2}{\mu}$$

→Reducing switch size increases τ → increased distortion→ not a viable solution
→Small τ and ΔV → use minimum chanel length
→For a given technology t x ΔV →conts.



# Sampling Switch Charge Injection Summary

- Extra charge injected onto sampling capacitor @ switch device turn-off
  - Charge sharing with $C_{ov}$
  - Channel charge
- Issues:
  - DC offset
  - Input dependant error voltage → distortion
- Solutions:
  - Complementary switch?
  - Addition of dummy switches?
  - Bottom-plate sampling?