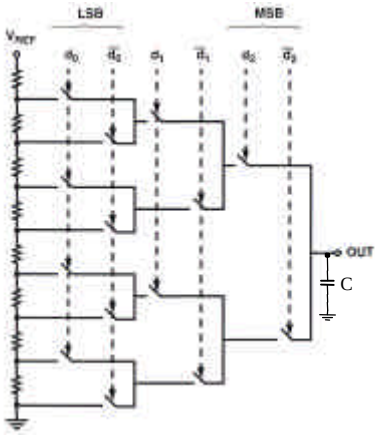
EE247
Lecture 15

D/A Converters
- D/A architecture examples
  - Unit element
  - Binary weighted
- Static performance
  - Component matching
  - Architectures
    - Unit element
    - Binary weighted
    - Segmented
  - Dynamic element matching
- Dynamic performance
  - Glitches
- DAC Examples

R-String DAC

- Advantages:
  - Simple, fast for <8-10bits
  - Inherently monotonic
  - Compatible with purely digital technologies
- Disadvantages:
  - 2^B resistors & 2^B switches for B bits → High element count & larger area for B>10bits
  - High settling time for B > 10: $\tau_{max} = 0.25 \times 2^B RC$

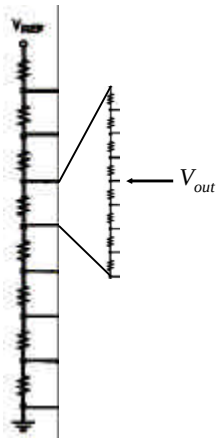


*Ref: M. Pelgrom, "A 10-b 50-MHz CMOS D/A Converter with 75-W Buffer," JSSC, Dec. 1990, pp. 1347.

R-String DAC Including Interpolation

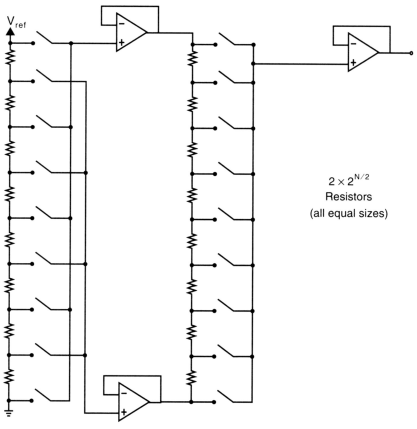
Resistor string DAC
Resistor string interpolator increases resolution w/o drastic increase in complexity
e.g. 6bit DAC→ 3+3

Considerations:
Interpolation string loading of main R string
Large R values → less loading but lower speed
Can use buffers



R-String DAC Including Interpolation

Use buffers
→ Issues: offset & speed

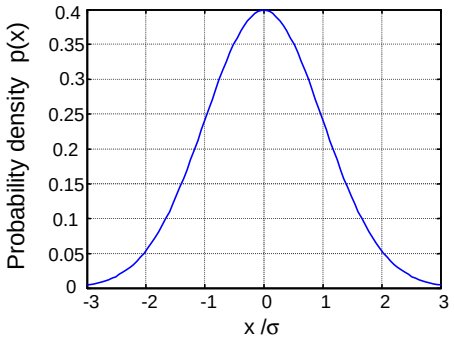


Static DAC INL / DNL Errors

- Component matching
- Systematic errors
  - Contact resistance
  - Edge effects in capacitor arrays
  - Process gradient
  - Finite current source output resistance
- Random errors
  - Lithography
  - Often Gaussian distribution (central limit theorem)

*Ref: C. Conroy et al, "Statistical Design Techniques for D/A Converters," JSSC Aug. 1989, pp. 1118-28.

Gaussian Distribution



$$p(x) = \frac{1}{\sqrt{2\pi}\,s} e^{-\frac{(x-m)^2}{2s^2}}$$

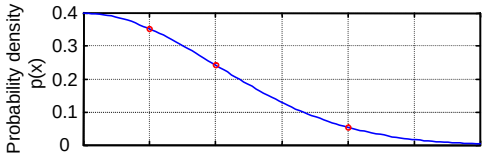
$$where\ standard\ \ deviation: s = \sqrt{E(X^2) - m^2}$$

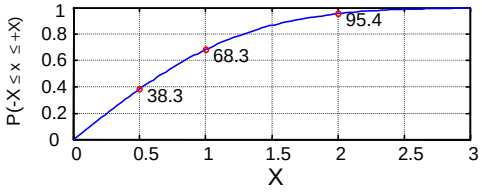
Yield

$$P(-X \le x \le +X) =$$

$$= \frac{1}{\sqrt{2p}} \int_{-X}^{+X} e^{-\frac{x^2}{2}} dx$$

$$= erf\left(\frac{X}{\sqrt{2}}\right)$$





Yield

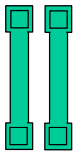
X/s	P(-X £ x £ X) [%]	X/s	P(-X £ x £ X) [%]
0.2000	15.8519	2.2000	97.2193
0.4000	31.0843	2.4000	98.3605
0.6000	45.1494	2.6000	99.0678
0.8000	57.6289	2.8000	99.4890
1.0000	68.2689	3.0000	99.7300
1.2000	76.9861	3.2000	99.8626
1.4000	83.8487	3.4000	99.9326
1.6000	89.0401	3.6000	99.9682
1.8000	92.8139	3.8000	99.9855
2.0000	95.4500	4.0000	99.9937

Example

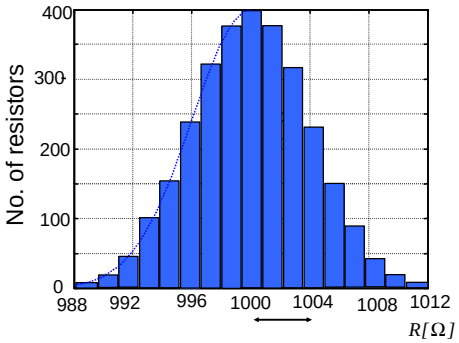
- Measurements show that the offset voltage of a batch of operational amplifiers follows a Gaussian distribution with $\sigma = 2mV$ and $\mu = 0$.
- Fraction of opamps with $|V_{os}| < X = 6mV$:
  - $X/\sigma = 3$ → 99.73 % yield (we'd still test before shipping!)
- Fraction of opamps with $|V_{os}| < X = 400\mu V$:
  - $X/\sigma = 0.2$ → 15.85 % yield

Component Mismatch

Example: Two side-by-side Resistors

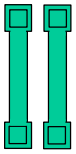


Large # of devices measured
& curved → typically if sample size large shape is Gaussian

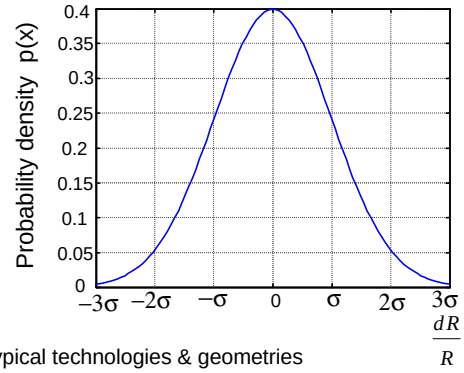


E.g. Let us assume in this example 1000 Rs measured & 68.5% within +-4OHM or +-0.4% of average
→ 1σ for resistors→ 0.4%

Component Mismatch



Two side-by-side Resistors



$$R = \frac{R_1 + R_2}{2}$$

$$dR = R_1 - R_2$$

$$s^2_{\frac{dR}{R}} \propto \frac{1}{Area}$$

For typical technologies & geometries

1σ for resistors→ 0.02 το 5%

In the case of resistors σ is a function of area

DNL Unit Element DAC

E.g. Resistor string DAC:

$$\Delta = R_{nom}\, I_{ref}$$

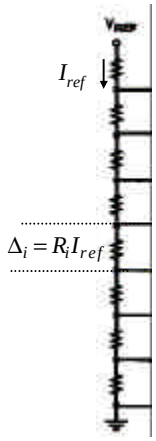
$$\Delta_i = R_i I_{ref}$$

$$DNL_i = \frac{\Delta_{nom} - \Delta}{\Delta}$$

$$= \frac{R_i - R_{nom}}{R_{nom}} = \frac{dR_{nom}}{R_{nom}} \approx \frac{dR_{nom}}{R_i}$$

$$s_{DNL} = s_{\frac{dR_i}{R_i}}$$

DNL of unit element DAC is independent of resolution!



DNL Unit Element DAC

E.g. Resistor string DAC:

$$\sigma_{DNL} = \sigma_{\frac{dR_i}{R_i}}$$

DNL of unit element DAC is independent of resolution!

Example:

If $\sigma_{dR/R}$ = 0.4%, what DNL spec goes into the datasheet so that 99.9% of all converters meet the spec?

Answer:

From table: for 99.9%

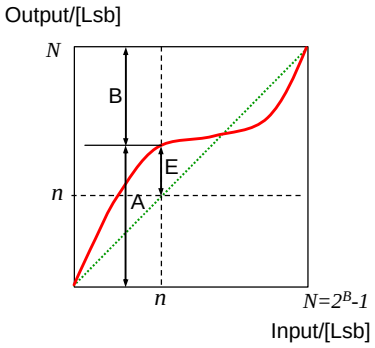
→ X/σ = 3.3

$\sigma_{DNL} = \sigma_{dR/R}$ = 0.4%

3.3 σ_{DNL} = 1.3%

→DNL= +/- 0.013 LSB

DAC INL Analysis



	Ideal	Variance
A	n	$n\sigma_\varepsilon^2$
B	N-n	$(N-n)\sigma_\varepsilon^2$

$E = A\text{-}n \quad r = n/N$

$= A\text{-}r(A+B)$

$= A\,(1\text{-}r)\,\text{-}B.r$

→ *Variance of E:*

$\sigma_E^2 = (1\text{-}r)^2 .\sigma_A^2 + r^2 .\sigma_B^2$

$= N.r\,.(1\text{-}r).\sigma_\varepsilon^2$

→Maximum @ $r = 0.5$, $n = N/2$

→Max INL @ midscale

DAC INL

$$s_E^2 = n\left(1 - \frac{n}{N}\right) \times s_e^2$$

$$To\ find\ max.\ variance: \quad \frac{ds_E^2}{dn} = 0$$

$$\rightarrow n = N/2$$

- Error is maximum at mid-scale (N/2):

$$s_{INL} = \frac{1}{2}\sqrt{2^B - 1}\, s_e$$
$$with \quad N = 2^B - 1$$

- INL depends on DAC resolution and element matching σ_ε
- While $s_{DNL} = s_e$

Ref: Kuboki et al, TCAS, 6/1982

Untrimmed DAC INL

$$s_{INL} \cong \frac{1}{2}\sqrt{2^B - 1}\, s_e$$

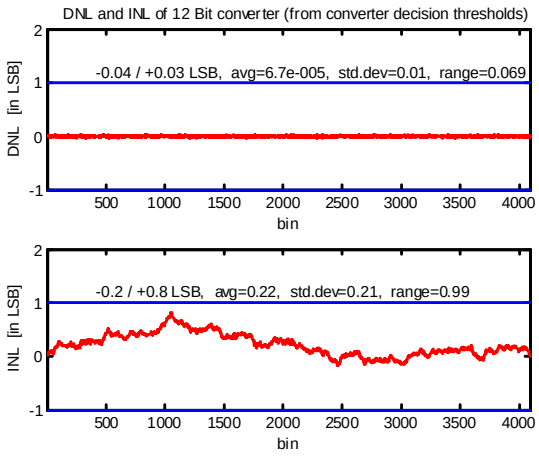
$$B \cong 2 + 2\log_2\left[\frac{s_{INL}}{s_e}\right]$$

Example:

σ_{INL} = 0.1 LSB

σ_ε = 1%	B = 8.6
σ_ε = 0.5%	B = 10.6
σ_ε = 0.2%	B = 13.3
σ_ε = 0.1%	B = 15.3

Simulation Example

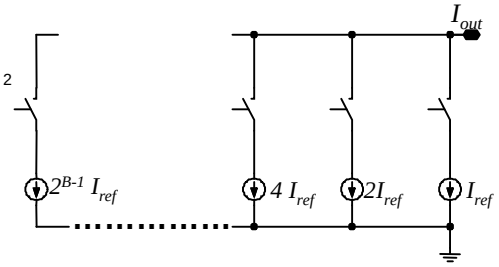


σ_ε = 1%
B = 12

σ_{INL} = 0.3 LSB (midscale)

Binary Weighted DAC

- INL same as for unit element DAC
- DNL depends on transition
  - Example:
    0 to 1 → $s_{DNL}^2 = s_{(dI/I)}^2$
    1 to 2 → $s_{DNL}^2 = 3s_{(dI/I)}^2$
- Consider MSB transition:
  0111 … → 1000 …

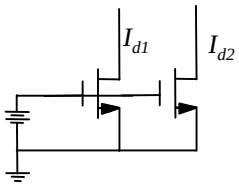


MOS Device Matching

$$I_d = \frac{I_{d1} + I_{d2}}{2}$$

$$\frac{dI_d}{I_d} = \frac{I_{d1} - I_{d2}}{I_d}$$

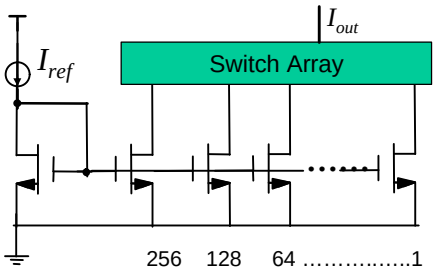
$$\frac{dI_d}{I_d} = \left[\left(\frac{d\,W/L}{W/L}\right) + \left(\frac{dV_{th}}{V_{GS} - V_{th}}\right)\right]$$



•Current matching depends on:
- -Device ratio matching
  - → larger area less mismatch effect
- -Threshold voltage matching
  - → Larger gate-overdrive less threshold voltage mismatch effect

Current-Switched DACs in CMOS

$$\frac{dI_d}{I_d} = \left[\left(\frac{d\,W/L}{W/L}\right) + \left(\frac{dV_{th}}{V_{GS} - V_{th}}\right)\right]$$

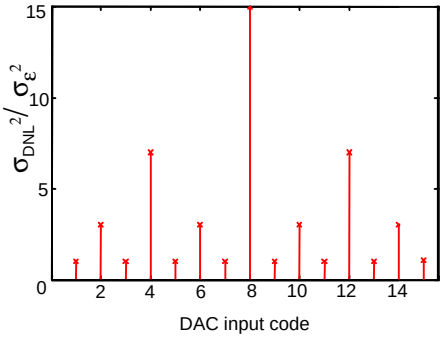


Example: 8bit Binary Weighted

•Advantages:
- Can be very fast
- Small area for <9-10bits

•Disadvantages:
- Matching depends on V_{th} matching & device W/L matching

DNL of Binary Weighted DAC



- Worst-case transition occurs at mid-scale:

$$s_{DNL}^2 = \underbrace{\left(2^{B-1}-1\right)s_e^2}_{0111\ldots} + \underbrace{\left(2^{B-1}\right)s_e^2}_{1000\ldots}$$

$$\cong 2^B s_e^2$$

$$s_{DNL_{max}} = 2^{B/2} s_e$$

$$s_{INLmax} \cong \frac{1}{2}\sqrt{2^B - 1}\, s_e \cong \frac{1}{2} s_{DNL_{max}}$$

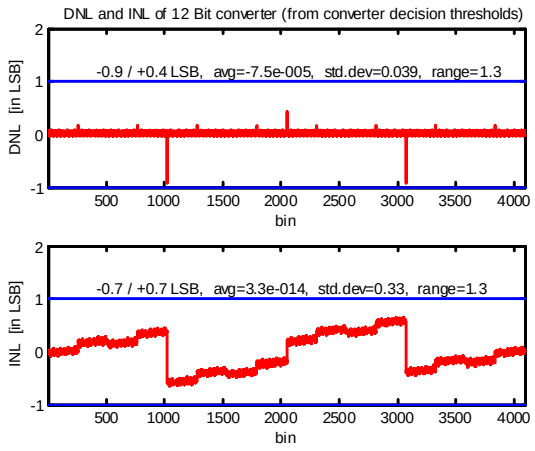
- Example:

B = 12, s_ε = 1%

→ s_{DNL} = 0.64 LSB

→ s_{INL} = 0.32 LSB

Simulation Example

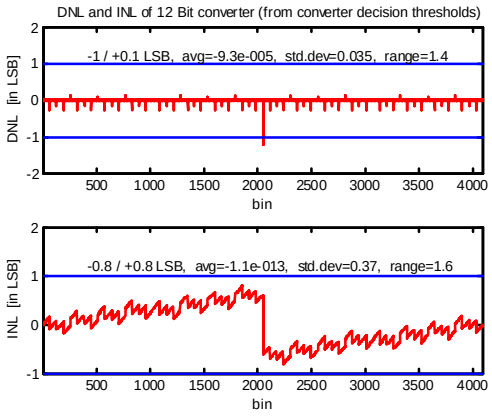


σ_ε = 1%
B = 12

σ_{DNL} = 0.6 LSB (midscale)

MSB transitions clearly visible

"Another" Random Run …



Now (by chance) worst DNL is mid-scale.

Statistical result!

Unit Element vs Binary Weighted

Unit Element DAC

$$s_{DNL} = s_e$$

$$s_{INL} \cong 2^{B/2-1} s_e$$

Binary Weighted DAC

$$s_{DNL} \cong 2^{B/2} s_e = 2 s_{INL}$$

$$s_{INL} \cong 2^{B/2-1} s_e$$

Number of switched elements:

$$S = 2^B \qquad S = B$$

Significant difference in performance and complexity!

Unit Element vs Binary Weighted Example: B=10

Unit Element DAC	Binary Weighted DAC
$s_{DNL} = s_e$	$s_{DNL} \cong 2^{B/2} s_e = 32 s_e$
$s_{INL} \cong 2^{B/2-1} s_e = 16 s_e$	$s_{INL} \cong 2^{B/2-1} s_e = 16 s_e$

Number of switched elements:

$S = 2^B = 1024$	$S = B = 10$

Significant difference in performance and complexity!

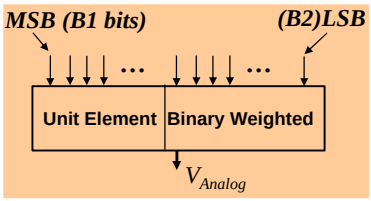
DAC INL/DNL Summary

- DAC architecture has significant impact on DNL
- INL is independent of DAC architecture and requires element matching commensurate with overall DAC precision
- Results are for uncorrelated random element variations
- Systematic errors and correlations are usually also important

Ref: Kuboki, S.; Kato, K.; Miyakawa, N.; Matsubara, K. Nonlinearity analysis of resistor string A/D converters. IEEE Transactions on Circuits and Systems, vol.CAS-29, (no.6), June 1982. p.383-9.

Segmented DAC

- Objective:
  compromise between unit element and binary weighted DAC



- Approach:
  B_1 MSB bits → unit elements
  $B_2 = B\text{-}B_1$ LSB bits → binary weighted
- INL: unaffected
- DNL: worst case occurs when LSB DAC turns off and one more MSB DAC element turns on: same as binary weighted DAC with B_2+1 bits
- Number of switched elements: $(2^{B1}-1) + B_2$

Comparison

Example:

B = 12, $B_1 = 5$, $B_2 = 7$

$\underbrace{B_1 = 6}_{\text{MSB}}$, $\underbrace{B_2 = 6}_{\text{LSB}}$

$\sigma_\varepsilon = 1\%$

$$s_{DNL} \cong 2^{(B_2+1)/2} s_e = 2 s_{INL}$$

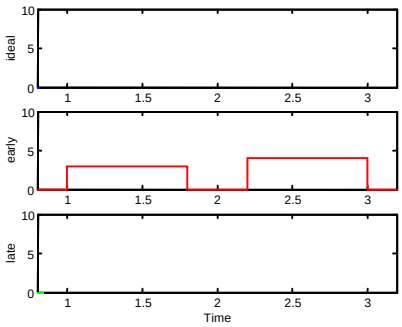
$$s_{INL} \cong 2^{B_2/2-1} s_e$$

$$S = 2^{B1} - 1 + B_2$$

DAC Architecture	$\sigma_{INL[LSB]}$	$\sigma_{DNL[LSB]}$	# s.e.
Unit element (10+0)	0.32	0.01	4095
Binary weighted(0+10)	0.32	0.64	12
Segmented 5+7	0.32	0.16	31+7
Segmented 6+6	0.32	0.113	63+6

Dynamic DAC Error: Glitch

- Consider binary weighted DAC transition 011 → 100
- DAC output depends on timing
- Plot shows situation where
  - LSB/MSBs on time
  - LSB early, MSB late
  - LSB late, MSB early



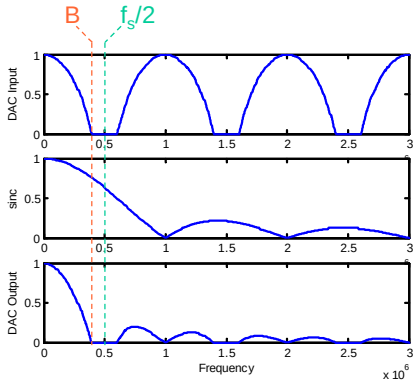
Glitch Energy

- Glitch energy (worst case): $\sim dt \times 2^{B-1}$
- LSB energy: $\sim T$
- Need $dt \times 2^{B-1} << T$ or $dt << 2^{-B+1} T$
- Examples:

f_s [MHz]	B	dt [ps]
1	12	<< 488
20	16	<< 1.5
1000	10	<< 2

DAC Reconstruction Filter

- Need for and requirements depend on application
- Tasks:
  - Correct for sinc distortion
  - Remove “aliases” (stair-case approximation)



Reconstruction Filter Options

- Digital and SC filter possible only in combination with oversampling (signal bandwidth B << $f_s/2$)
- Digital filter can prewarp spectrum to compensate in-band sinc attenuation (from ZOH)

Sample DAC Implementations

- Untrimmed segmented
  - T. Miki et al, “An 80-MHz 8-bit CMOS D/A Converter,” JSSC December 1986, pp. 983.
  - A. Van den Bosch et al, “A 1-GSample/s Nyquist Current-Steering CMOS D/A Converter,” JSSC March 2001, pp. 315.
- Current copiers:
  - D. W. J. Groeneveld et al, “A Self-Calibration Techique for Monolithic High-Resolution D/A Converters,” JSSC December 1989, pp. 1517.
- Dynamic element matching:
  - R. J. van de Plassche, “Dynamic Element Matching for High-Accuracy Monolithic D/A Converters,” JSSC December 1976, pp. 795.

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An 80-MHz 8-bit CMOS D/A Converter

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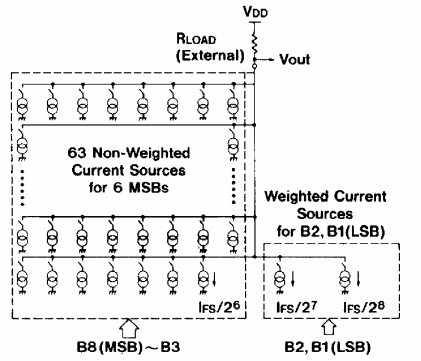


Fig. 1. Basic architecture of the DAC.

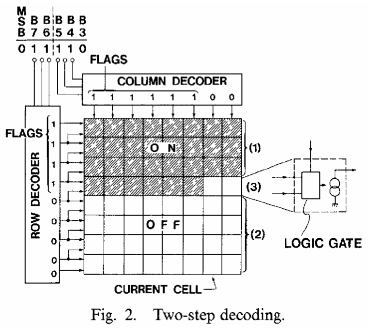
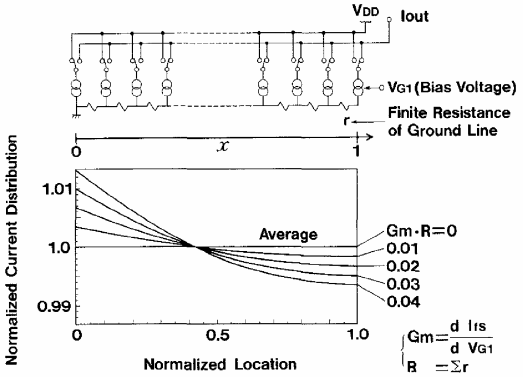


Fig. 2. Two-step decoding.



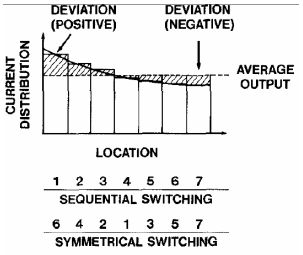
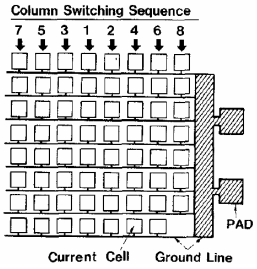
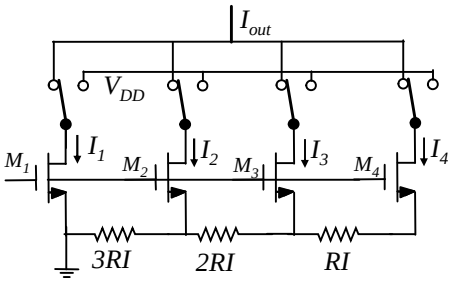


Fig. 9. Symmetrical switching.



Current-Switched DACs in CMOS

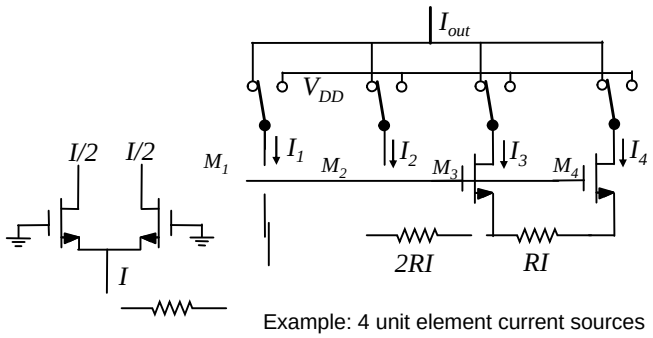
$$I_1 = k\left(V_{GS_{M_1}} - V_{th}\right)^2$$
$$V_{GS_{M_2}} = V_{GS_{M_1}} - 3RI$$
$$V_{GS_{M_3}} = V_{GS_{M_1}} - 5RI$$
$$V_{GS_{M_4}} = V_{GS_{M_1}} - 6RI$$
$$I_2 = k\left(V_{GS_{M_2}} - V_{th}\right)^2 = I_1\left(1 - \frac{3RI}{V_{GS_{M_1}} - V_{th}}\right)^2$$
$$g_{m_{M_1}} = \frac{2I_1}{V_{GS_{M_1}} - V_{th}}$$
$$\rightarrow I_2 = I_1\left(1 - \frac{3Rg_{m_{M_1}}}{2}\right)^2 \approx I_1\left(1 - 3Rg_{m_{M_1}}\right)$$
$$\rightarrow I_3 = I_1\left(1 - \frac{3Rg_{m_{M_1}}}{2}\right)^2 \approx I_1\left(1 - 5Rg_{m_{M_1}}\right)$$
$$\rightarrow I_4 = I_1\left(1 - \frac{3Rg_{m_{M_1}}}{2}\right)^2 \approx I_1\left(1 - 6Rg_{m_{M_1}}\right)$$



Example: 4 unit element current sources

•Assumption: *RI* is small compared to transistor gate overdrive
→ Desirable to have *gm* small

Current-Switched DACs in CMOS

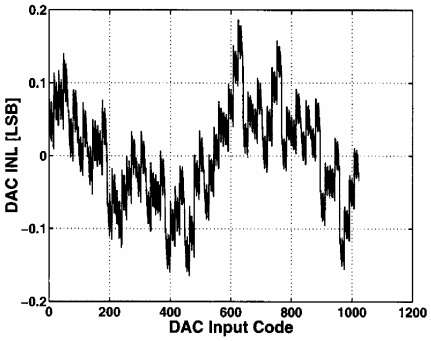


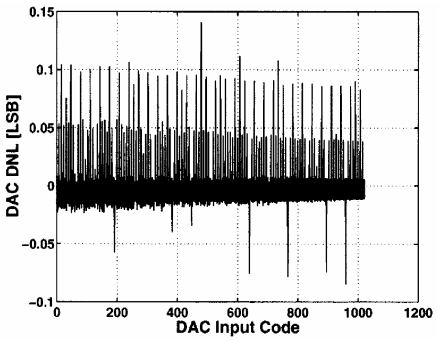
Example: 4 unit element current sources

•Assumption: *RI* is small compared to xtor gate overdrive
→ Desirable to have *gm* small

A 10-bit 1-GSample/s Nyquist Current-Steering CMOS D/A Converter

Anne Van den Bosch, *Student Member, IEEE*, Marc A. F. Borremans, *Student Member, IEEE*, Michel S. J. Steyaert, *Senior Member, IEEE*, and Willy Sansen, *Fellow, IEEE*





IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 24, NO. 6, DECEMBER 1989

A Self-Calibration Technique for Monolithic High-Resolution D/A Converters

D. WOUTER J. GROENEVELD, HANS J. SCHOUWENAARS, SENIOR MEMBER, IEEE, HENK A. H. TERMEER, AND CORNELIS A. A. BASTIAANSEN

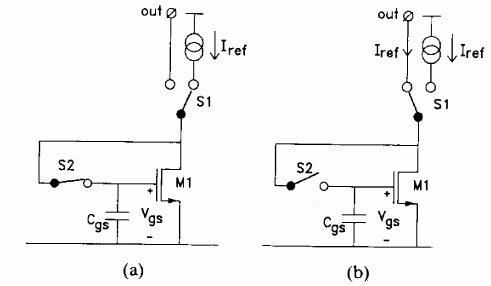
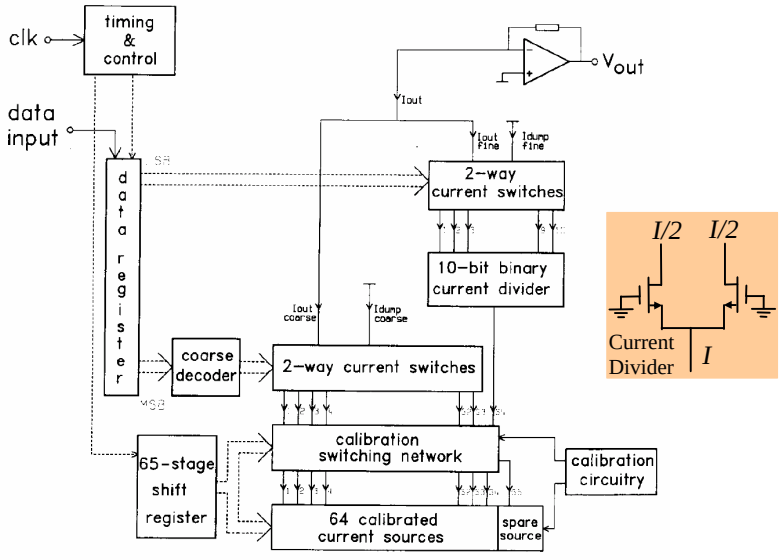
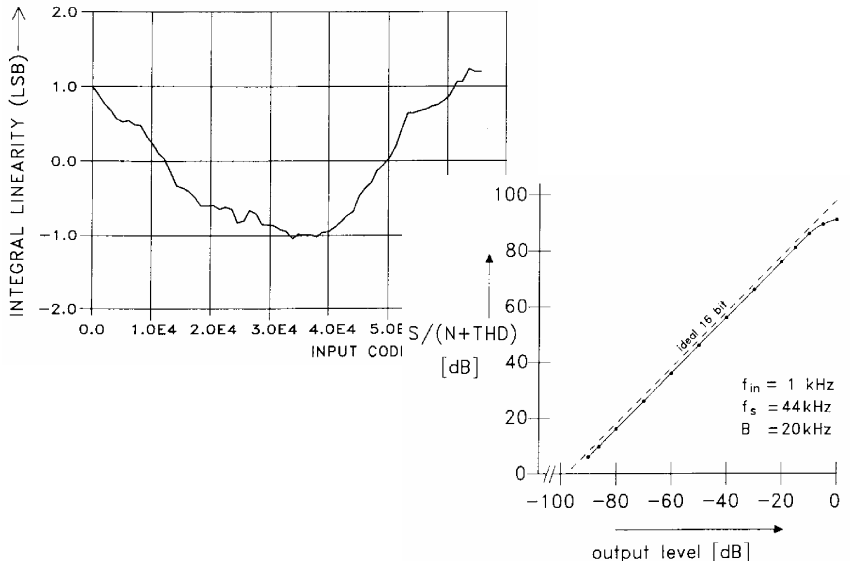


Fig. 2. Calibration principle. (a) Calibration. (b) Operation.





IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. SC-11, NO. 6, DECEMBER 1976 795

Dynamic Element Matching for High-Accuracy Monolithic D/A Converters

RUDY J. VAN DE PLASSCHE

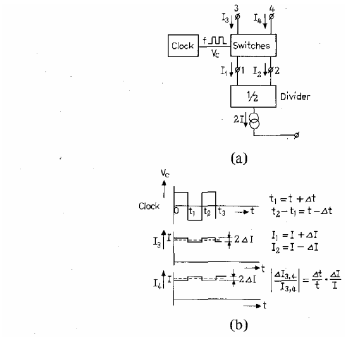
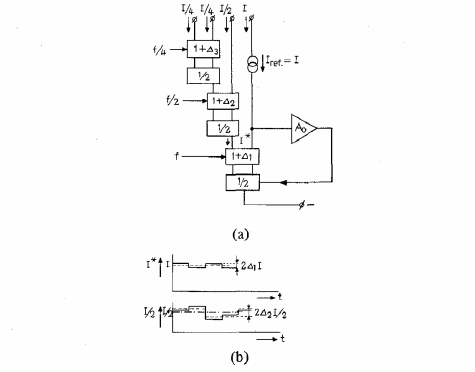


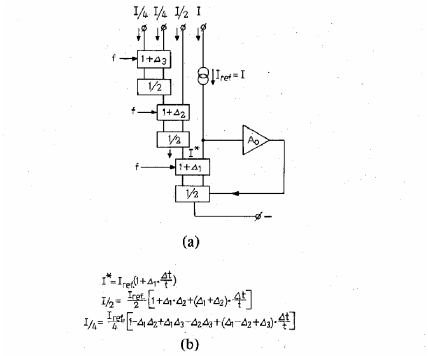
Fig. 2. (a) New current divider schematic diagram. (b) Time dependence of various currents in the new divider.



(a)

(b)

Fig. 4. (a) Binary weighted current network using different switching frequencies. (b) Time dependence of currents flowing in the first and second divider stage.



(a)

(b)

(a) Binary weighted current network with equal switching frequency. (b) Error analysis results.

Dynamic Element Matching

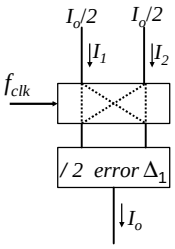
During Φ_1

$$I_1^{(1)} = \tfrac{1}{2} I_o (1+\Delta_1)$$
$$I_2^{(1)} = \tfrac{1}{2} I_o (1-\Delta_1)$$

During Φ_2

$$I_1^{(2)} = \tfrac{1}{2} I_o (1-\Delta_1)$$
$$I_2^{(2)} = \tfrac{1}{2} I_o (1+\Delta_1)$$

$$\langle I_2 \rangle = \frac{I_2^{(1)} + I_2^{(2)}}{2}$$
$$= \frac{I_o}{2} \frac{(1-\Delta_1)+(1+\Delta_1)}{2}$$
$$= \frac{I_o}{2}$$



Dynamic Element Matching

During Φ_1

$$I_1^{(1)} = \tfrac{1}{2} I_o (1+\Delta_1)$$
$$I_2^{(1)} = \tfrac{1}{2} I_o (1-\Delta_1)$$

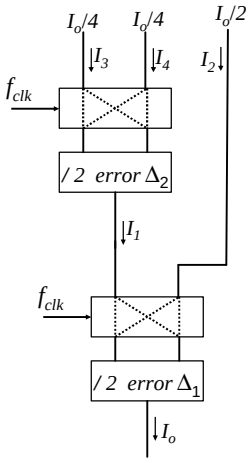
$$I_3^{(1)} = \tfrac{1}{2} I_1^{(1)} (1+\Delta_2)$$
$$= \tfrac{1}{4} I_o (1+\Delta_1)(1+\Delta_2)$$

During Φ_2

$$I_1^{(2)} = \tfrac{1}{2} I_o (1-\Delta_1)$$
$$I_2^{(2)} = \tfrac{1}{2} I_o (1+\Delta_1)$$

$$I_3^{(2)} = \tfrac{1}{2} I_1^{(2)} (1-\Delta_2)$$
$$= \tfrac{1}{4} I_o (1-\Delta_1)(1-\Delta_2)$$

$$\langle I_3 \rangle = \frac{I_3^{(1)} + I_3^{(2)}}{2}$$
$$= \frac{I_o}{4} \frac{(1+\Delta_1)(1+\Delta_2) + (1-\Delta_1)(1-\Delta_2)}{2}$$
$$= \frac{I_o}{4}(1+\Delta_1\Delta_2)$$

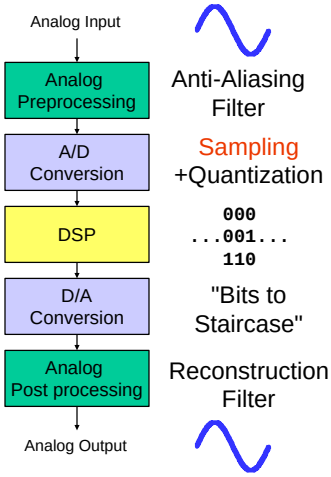


E.g. $\Delta_1 = \Delta_2 = 1\%$ → matching error is $(1\%)^2 = 0.01\%$

MOS Sampling Circuits

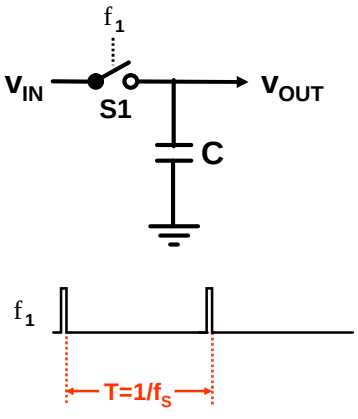
Re-Cap

- How can we build circuits that "sample"

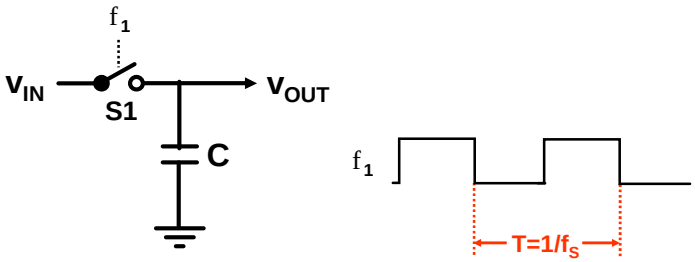


Ideal Sampling

- In an ideal world, zero resistance sampling switches would close for the briefest instant to sample a continuous voltage v_{IN} onto the capacitor C
- Not realizable!

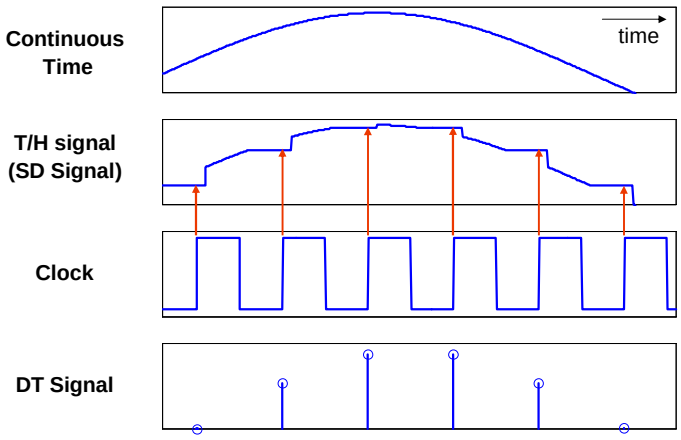


Ideal T/H Sampling

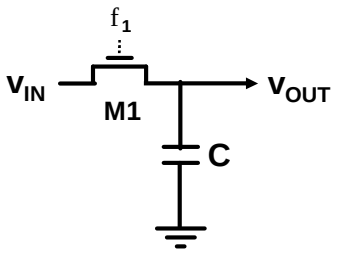


- V_{out} tracks input when switch is closed
- Grab *exact* value of V_{in} when switch opens
- "Track and Hold" (T/H)

Ideal T/H Sampling



Practical Sampling



- kT/C noise
- Finite R_{sw} → limited bandwidth
- $R_{sw} = f(V_{in})$ → distortion
- Switch charge injection (EE240)
- Clock jitter

kT/C Noise

$$\frac{k_B T}{C} \leq \frac{\Delta^2}{12}$$

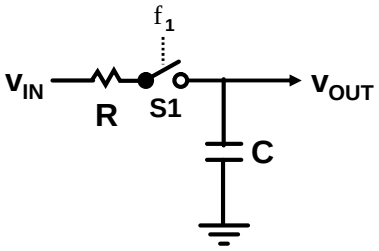
$$C \geq 12 k_B T \left(\frac{2^B - 1}{V_{FS}} \right)^2$$

In high resolution ADCs kT/C noise usually dominates overall error (power dissipation considerations).

B	C_{min} (V_{FS} = 1V)
8	0.003 pF
12	0.8 pF
14	13 pF
16	206 pF
20	52,800 pF

Acquisition Bandwidth

- The resistance R of switch S1 turns the sampling network into a lowpass filter with risetime $= RC = t$
- Assuming V_{in} is constant during the sampling period and C is initially discharged



$$v_{out}(t) = v_{in}\left(1 - e^{-t/t}\right)$$

Switch On-Resistance

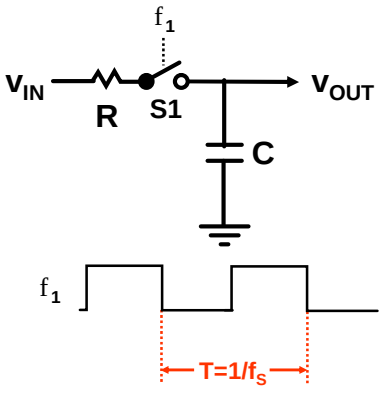
$$V_{in} - V_{out}\left(t = \frac{1}{2 f_s}\right) << \Delta$$

$$V_{in} e^{-1/2 f_s t} << \Delta$$

Worst Case: $V_{in} = V_{FS}$

$$t << -\frac{T}{2}\frac{1}{\ln\left(2^B - 1\right)}$$

$$R << -\frac{1}{2 f_s C}\frac{1}{\ln\left(2^B - 1\right)}$$



Example:

B = 14, C = 13pF, f_s = 100MHz

T/τ >> 19.4, R << 40Ω

Switch On-Resistance

$$I_{D(triode)} = mC_{ox}\frac{W}{L}\left(V_{GS} - V_{TH} - \frac{V_{DS}}{2}\right)V_{DS}, \qquad \frac{1}{R_{ON}} \cong \left.\frac{dI_{D(triode)}}{dV_{DS}}\right|_{V_{DS}\to 0}$$

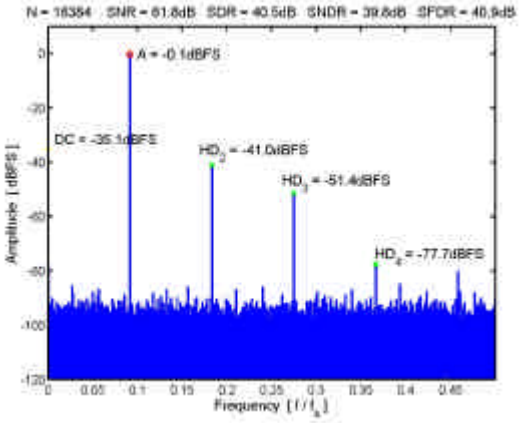
$$R_{ON} = \frac{1}{mC_{ox}\frac{W}{L}(V_{GS} - V_{th})} = \frac{1}{mC_{ox}\frac{W}{L}(V_{DD} - V_{th} - V_{in})}$$

for $$R_o = \frac{1}{mC_{ox}\frac{W}{L}(V_{DD} - V_{th})}$$

$$R_{ON} = \frac{R_o}{1 - \frac{V_{in}}{V_{DD} - V_{th}}}$$

Sampling Distortion

$$v_{out} = v_{in}\left(1 - e^{-\frac{T}{2t}\left(1 - \frac{V_{in}}{V_{DD} - V_{th}}\right)}\right)$$

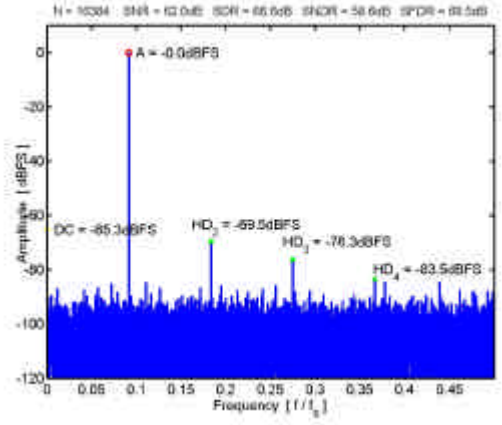


10bit ADC & T/τ = 10

$V_{DD} - V_{th} = 2V$ $V_{FS} = 1V$

Sampling Distortion

- SFDR is very sensitive to sampling distortion
- Solutions:
  - Overdesign→ Larger switches
    → increased switch charge injection
  - Complementary switch
  - Maximize V_{DD}/V_{FS}
    → decreased dynamic range
  - Constant V_{GS} ? f(V_{in})
    → …



10bit ADC T/τ = **20**
$V_{DD} - V_{th}$ = 2V V_{FS} = 1V