EE247
Lecture 13

- Data Converters
  - Summary last lecture
  - Spectral testing
  - Practical aspects of converter testing
    - Signal source
    - Clock generator
    - Evaluation board considerations
    - Evaluation set-up
    - Debugging

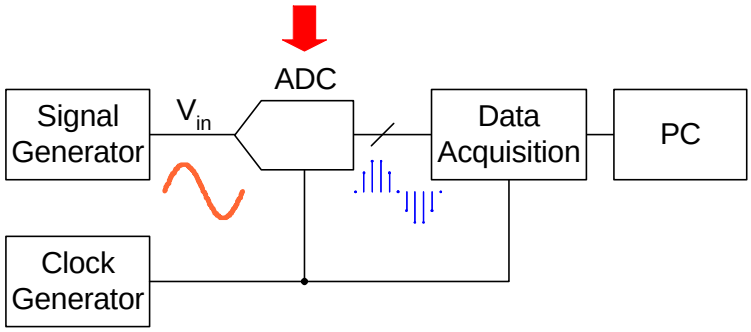
Converter Testing

- DAC:
  - "trivial", apply codes and use a good voltmeter to measure output
- ADC
  - Need to find "decision levels", i.e. input voltages at all code boundaries
    - One way: Adjust voltage source to find exact code trip points "code boundary servo"
    - More versatile: Histogram testing

      →Apply a signal with known distribution (ramp or sinusoid) and analyze digital code distribution at ADC output
  - Spectral testing
    - Reveals ADC errors associated with dynamic behaviour i.e. ADC performance as a function of frequency

DFT Test

Device Under Test (DUT)



Discrete Fourier Transform

DFT of a block of N samples

$$\{x(k)\} = \{x(0), x(1), x(2),\ldots,x(N-1)\}$$

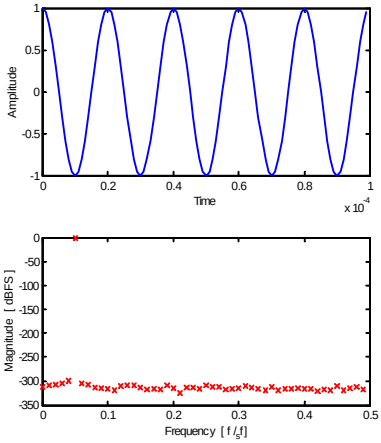
→ set of N frequency bins

$$\{A_m\} = \{A_0,A_1,A_2,\ldots,A_{N-1}\}$$

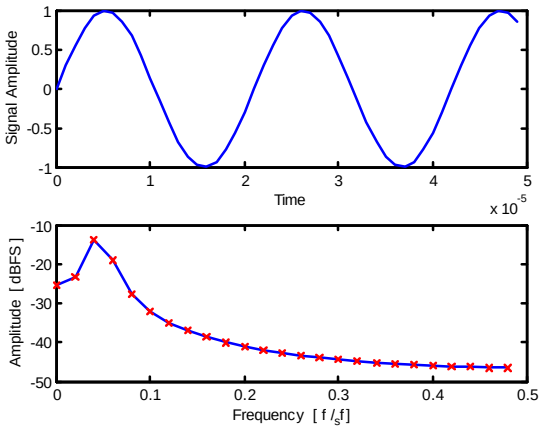
- DFT of N samples spaced $T=1/f_s$ seconds:
  - N frequency bins
  - Bin m represents frequencies at $m * f_s/N$ [Hz]
- DFT frequency resolution:
  - Proportional to 1/(NT) in [Hz/bin]
  - NT is proportional to total time spent gathering samples

DFT Example

```
fs  = 1e6;
fx  = 50e3;
Afs = 1;
N   = 100;

% time vector
t = linspace(0, (N-1)/fs, N);
% signal
y = Afs * cos(2*pi*fx*t);
% spectrum
s = 20 * log10(abs(fft(y)/N/Afs*2));
% drop redundant half
s = s(1:N/2);
% frequency vector (normalized to fs)
f = (0:length(s)-1) / N;
```



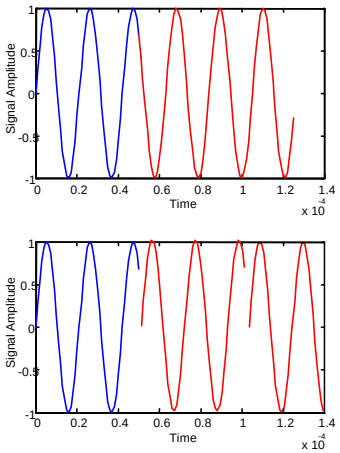
"Another" Example …



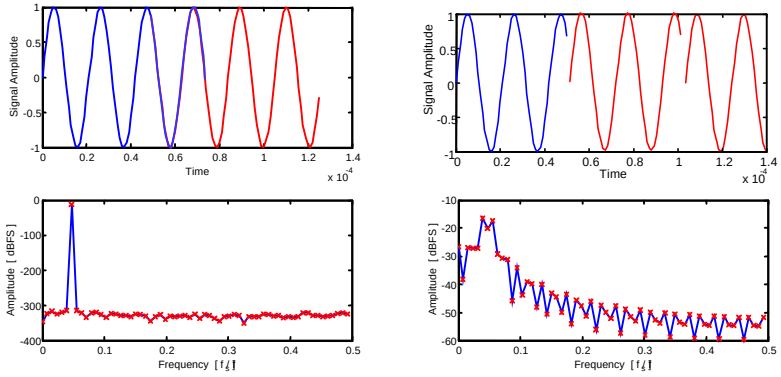
This does not look like the spectrum of a sinusoid …

DFT Periodicity

- The DFT implicitly assumes that time sample blocks repeat every N samples
- With a non-integral number of periods periods within our observation window, the input yields a huge amplitude/phase discontinuity at the block boundary
- This energy spreads into all frequency bins as “spectral leakage”
- Spectral leakage can be eliminated by either
  - An integral number of sinusoids in each block
  - Windowing

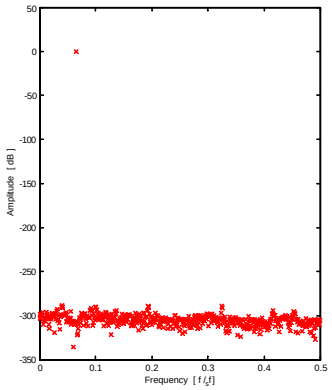


Spectra



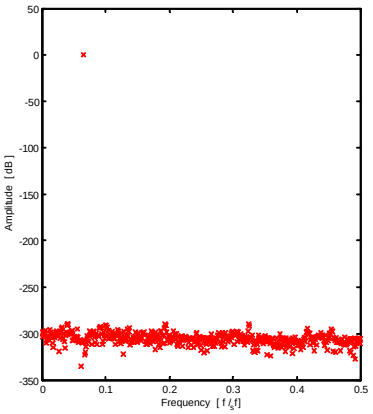
Integral Number of Periods

```
fs = 1e6;

% number of full cycles in test
cycles = 67;

% power of 2 speeds up analysis
% but make N/cycles non-integer!
N = 2^10;

% signal frequency
fx = fs*cycles/N
```



Integral Number of Periods

- Fundamental falls into a single DFT bin
- Noise (here numerical quantization) occupies all other bins
- "Integral number of periods" constrains signal frequency f_x
- Alternative: windowing →

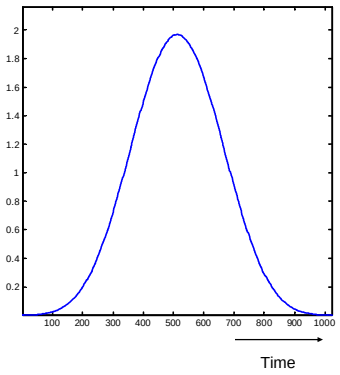


Windowing

- Spectral leakage can also be virtually eliminated by "windowing" time samples prior to the DFT
  - Windows taper smoothly down to zero at the beginning and the end of the observation window
  - Time samples are multiplied by window coefficients on a sample-by-sample basis
- Windowing sinewaves places the window spectrum at the sinewave frequency
  → Convolution in frequency domain

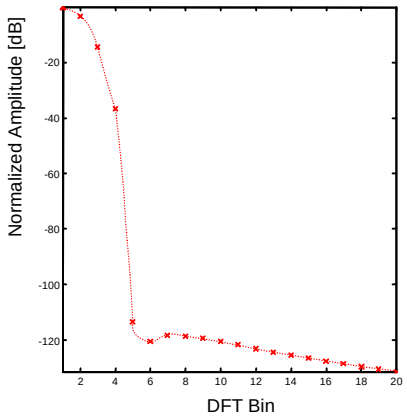
Window

- Time samples are multiplied by window coefficients on a sample-by-sample basis
- Multiplication in the time domain corresponds to convolution in the frequency domain
- Example: Nuttall window



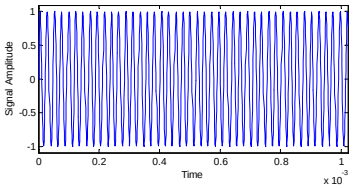
DFT of Nuttall Window

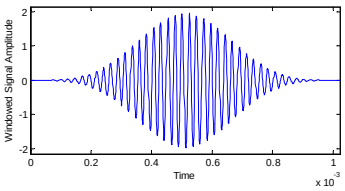
- Only first 20 bins shown
- Response essentially zero for bins > 5
- Lots of windows to choose from (go by name of inventor- Blackman, Harris…)
- Various windows trade-off attenuation versus width (smearing of sinusoids)



Windowed Data

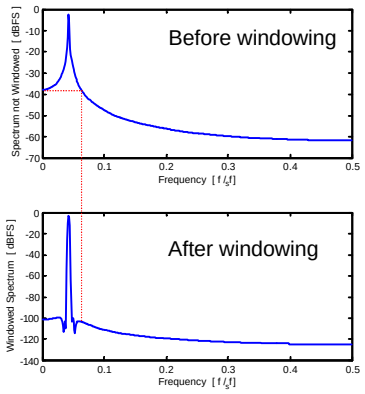
- The plot on the right shows the signal before and after windowing
- Windowing removes the discontinuity at block boundaries





DFT of Windowed Signal

- Spectra of signal before and after windowing
- Window gives ~ 100dB attenuation of sidelobes (use longer window for higher attenuation)
- Signal energy "smeared" over several (approximately 10) bins



Integral Cycles versus Windowing

- Integral number of cycles
  - Signal energy for a single sinusoid falls into single DFT bin
  - Requires careful choice of f_x
  - Ideal for simulations
  - Measurements→ need to lock f_x to f_s (PLL)
- Windowing
  - No restrictions on f_x →no need to have the signal locked to f_s → ideal for measurements
  - Signal energy (and harmonics) distributed over several DFT bins
  - Requires more data points for a fixed accuracy

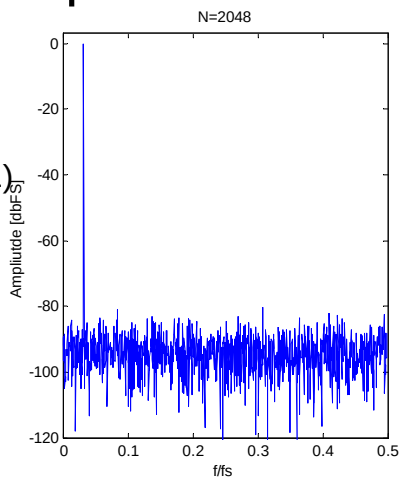
Spectral ADC Testing

- ADC with B bits
- ±1 full scale input

```
B = 10;
delta = 2/(2^B-1);
th = -1+delta/2:delta:1-delta/2;
x = sin(…);
y = adc(x, th) * delta - 1;
s = abs(fft(y)/N*2);s = s(1:N/2);
f = (0:length(s)-1) / N;
```


ADC Output Spectrum

- Signal amplitude:
  - Bin: `N * fx/fs + 1` (Matlab arrays start at 1)
  - A = 0dBFS
- SNR?

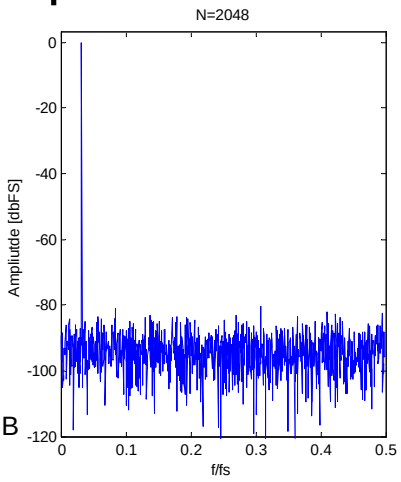


ADC Output Spectrum

- Noise bins: all except signal bin

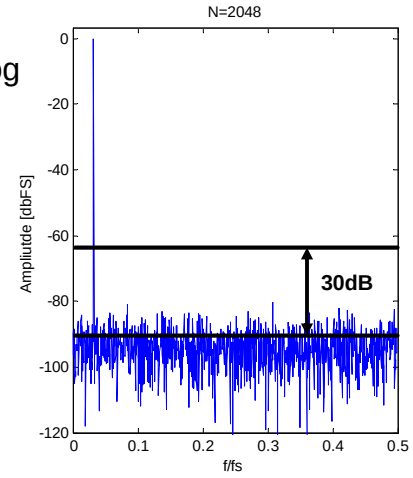
```
bx = N*fx/fs + 1;
As = 20*log10(s(bx))
s(bx) = 0;
An = 10*log10(sum(s.^2))
SNR = As - An
```

- SNR = 62dB (10 bits)
- Computed SQNR = 6.02xN+1.76dB



Why is noise floor not 62dB ?

- DFT bins act like an analog spectrum analyzer with bandwidth of f_s/N, rather than $f_s/2$
- The DFT noise floor is $10\log_{10}(N/2)$dB below the actual noise floor (assuming white noise)
- For N=2048: 30dB



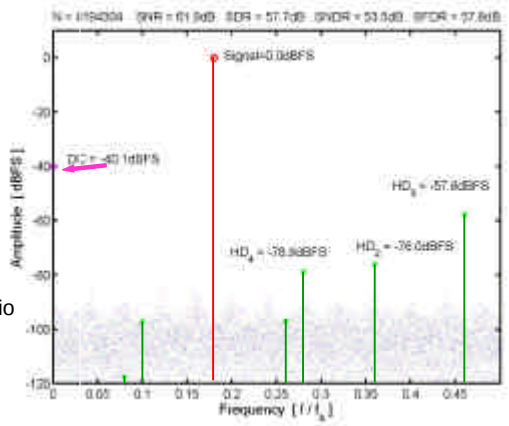
DFT Plot Annotation

1. Specify how many DFT points (N) are used, or
2. Shift DFT noise floor by $10\log_{10}(N/2)$dB, or
3. Normalize to "noise power in 1Hz bandwidth"

Spectral Performance Metrics

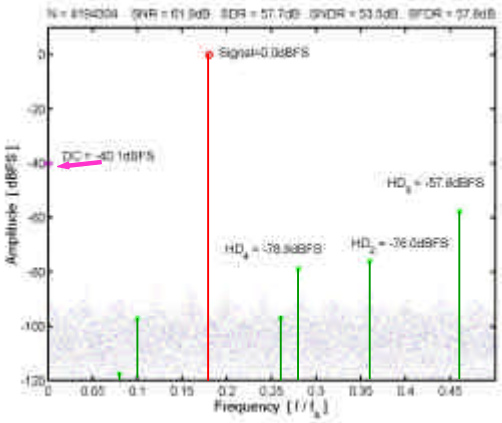
- Signal S
- DC
- Distortion D
- Noise N

- Signal-to-noise ratio
  SNR = S / N
- Signal-to-distortion ratio
  SDR = S / D
- Signal-to-noise+distortion ratio
  SNDR = S / (N+D)
- Spurious-free dynamic range
  SFDR

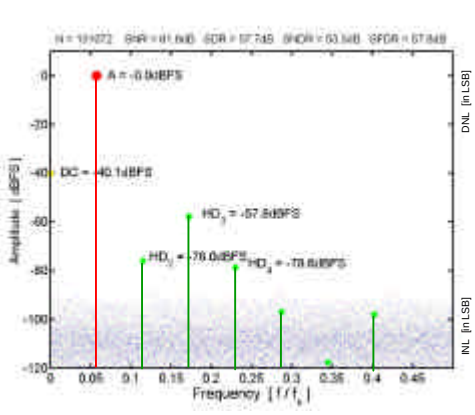


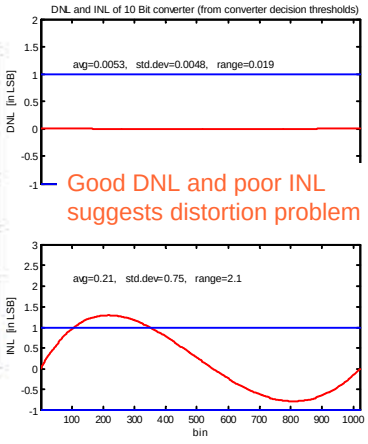
Harmonic Components

- At multiples of f_x
- Aliasing:
  - $f_{signal} = f_x = 0.18\ f_s$
  - $f_2 = 2\ f_0 = 0.36\ f_s$
  - $f_3 = 3\ f_0 = 0.54\ f_s$
    → $0.46\ f_s$
  - $f_4 = 4\ f_0 = 0.72\ f_s$
    → $0.28\ f_s$
  - $f_5 = 5\ f_0 = 0.90\ f_s$
    → $0.10\ f_s$
  - $f_6 = 6\ f_0 = 1.08\ f_s$
    → $0.08\ f_s$



Spectrum versus INL, DNL





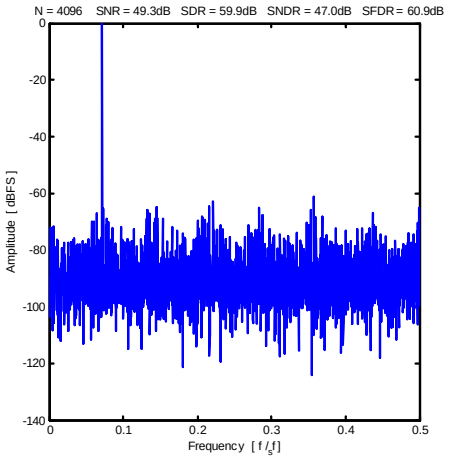
Good DNL and poor INL suggests distortion problem

Relationship INL-SFDR/SNDR

- Depends on "shape" of INL
- Rule of Thumb: SFDR ≅ 20log(2^B/INL)
  - E.g. 1LSB INL, 10b→ SFDR≅60dB
- Beware, this is of course only true under the same conditions at which the INL was taken, i.e. typically low input frequency

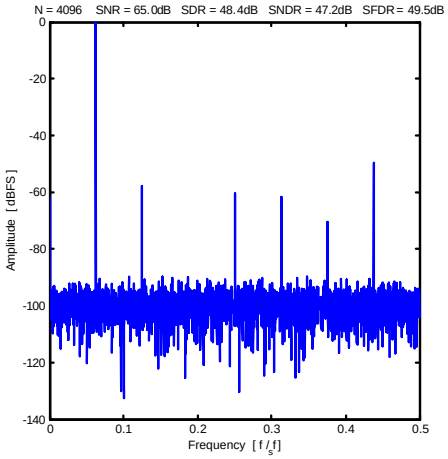
ADC Noise Example

- At right is the spectrum of a 10-Bit converter
- SNDR = 47dB – something's amiss
- Distortion?
  SDR = 59.9dB – no
- Must be a noise problem, but is it thermal or quantization noise?



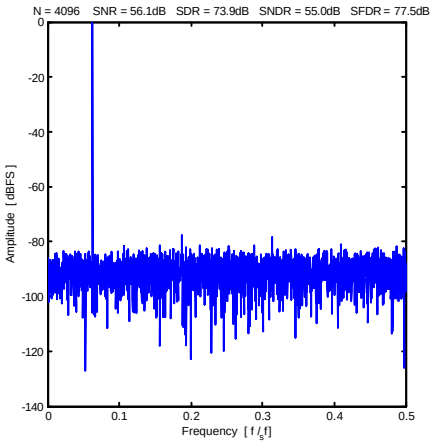
Noise Investigation

- At right is the spectrum of the same 10-Bit converter for $f_x = f_s / 16$
- Since f_x divides f_s, the quantization noise is periodic!
- It falls into the same bins the harmonics would normally occupy
- Hence
  - SNR → thermal noise
  - SDR → quantization noise (apparently the culprit)



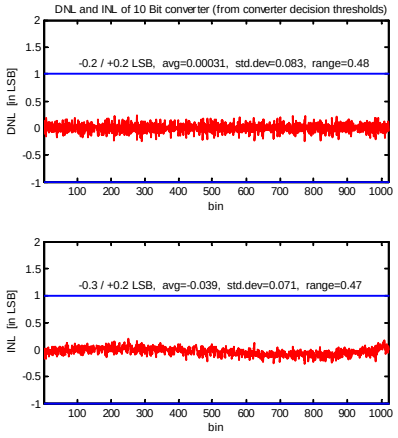
Noise Investigation

- After re-design … ($f_x = f_s / 16$)
- The quantization noise is not a major error: SDR = 74dB
- SNR = 56.1dB
  This corresponds to Gaussian noise with variance $\Delta/2$ at the converter input … a reasonable design choice



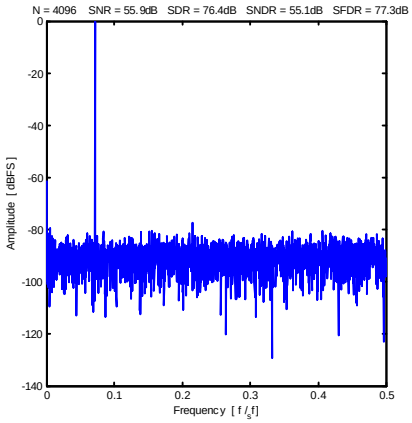
Noise Investigation

- The DNL and INL confirm the good result
- But the INL shows some “bowing” … let’s see if our test masked a distortion problem



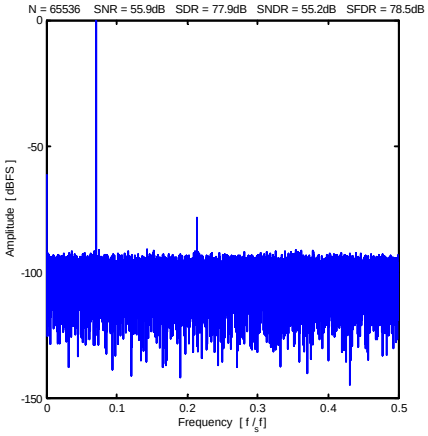
Noise Investigation

- For that we revert to simulating with f_s/f_x non-integer
- A 3rd harmonic is barely visible
- How can we “lift” it out of the noise?

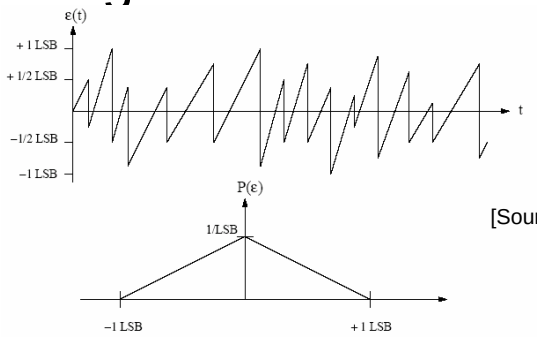


Noise Investigation

- Increasing N, the number of samples (and hence the measurement or simulation time) distributes the noise over more bins
- More bins → less noise power per bin (total noise stays constant)
- SFDR = 78dB for 10Bit is acceptable in many applications



SNR Degradation due to DNL



[Source: Ion Opris]

- For ideal quantizer we assumed uniform quatization error over +/- Δ/2
- Let's now add uniform DNL over +/- 0.5LSB and repeat math...

SNR Degradation due to DNL

- Integrate triangular pdf:

$$\overline{e^2} = 2\int_0^{+\Delta}(1-e)\frac{e^2}{\Delta}de = \frac{\Delta^2}{6} \quad \Rightarrow SNR = 6.02\cdot N - 1.25 \text{ [dB]}$$

3dB

- Compare to ideal quantizer:

$$\overline{e^2} = \int_{-\Delta/2}^{+\Delta/2}\frac{e^2}{\Delta}de = \frac{\Delta^2}{12} \quad \Rightarrow SNR = 6.02\cdot N + 1.76 \text{ [dB]}$$

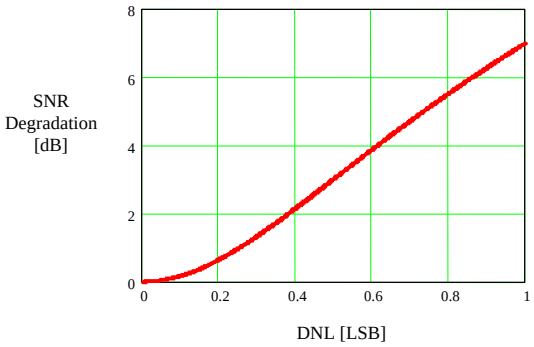
SNR Degradation due to DNL

- More general case:
  - Uniform quantization error ±0.5Δ
  - Uniform DNL error ±DNL [LSB]
  - Convolution yields trapezoid
  - SQNR becomes:

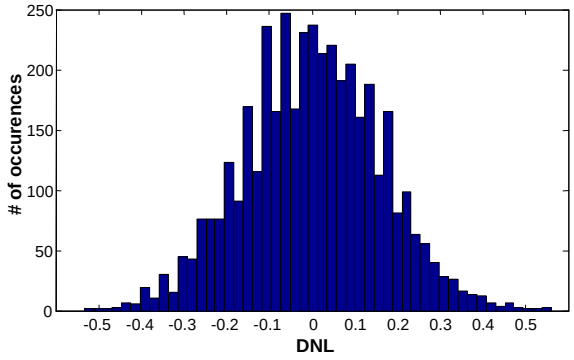
$$SQNR = \frac{\frac{1}{2}\left(\frac{2^N\Delta}{2}\right)^2}{\frac{\Delta^2}{12} + \frac{DNL^2}{3}}$$

SNR Degradation due to DNL

- Degradation in dB: $SQNR\_\deg = 1.76 - 10\log\left[\frac{\frac{1}{8}}{\frac{1}{12}+\frac{DNL^2}{3}}\right]$



Uniform DNL?



- DNL distribution of 12-bit ADC test chip
- Not quite uniform...

Adding It all up...

$$SQNR\_\deg = 1.76dB - 10\log\left[\frac{\frac{1}{8}}{\frac{1}{12}+\frac{0.3^2}{3}+0.5^2}\right]dB = 6.4dB$$

DNL Thermal noise

- Ideal 12b ADC: SNR=74dB
- Predicted from above: 74dB - 6.4dB = 67.6dB
- Measured: SNR=68dB

Effective Number of Bits

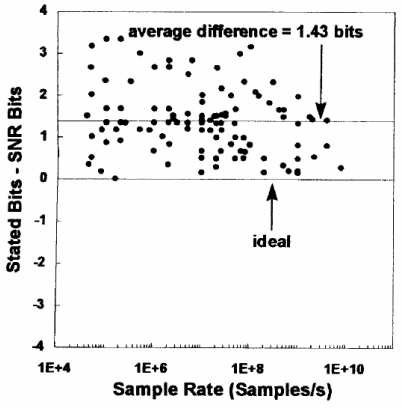
- Is a 12-Bit converter with 68dB SNDR really a 12-Bit converter?
- Effective Number of Bits

$$ENOB = \frac{SNDR - 1.76\text{dB}}{6.02\text{dB}} = \frac{68 - 1.76}{6.02} = 11.0\text{Bits}$$

ENOB

- At best, we get "ideal" ENOB only for zero thermal noise, zero DNL, zero INL
- Low noise is costly, 4x penalty in power per (ENOB-) bit or 6dB SNDR
- Rule of thumb for good peformance /power tradeoff: ENOB < N-1

ENOB Survey



R. H. Walden, "Analog-to-digital converter survey and analysis," *IEEE J. on Selected Areas in Communications*, pp. 539-50, April 1999

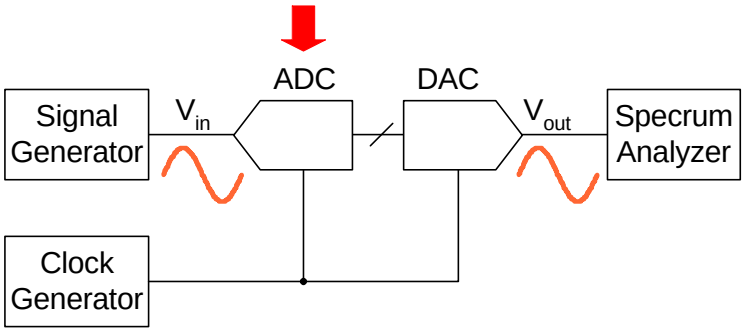
Converter Testing
Practical Aspects

Just Got Silicon Back...

- Now what ?
- Practical aspects of converter testing
- Equipment requirements
- Pitfalls

Direct ADC-DAC Test

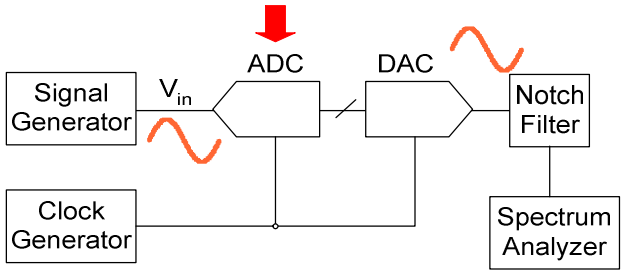
Device Under Test (DUT)



- Need a very good DAC
- Actually a good way to "get started"...

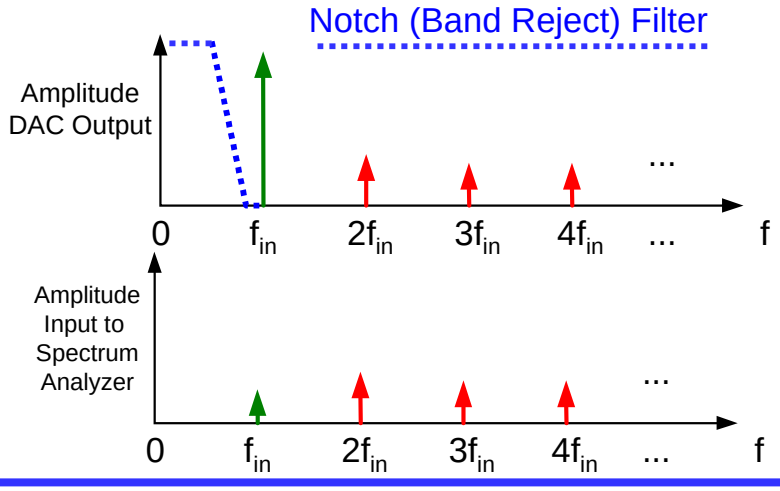
Direct ADC-DAC Test

Device Under Test (DUT)

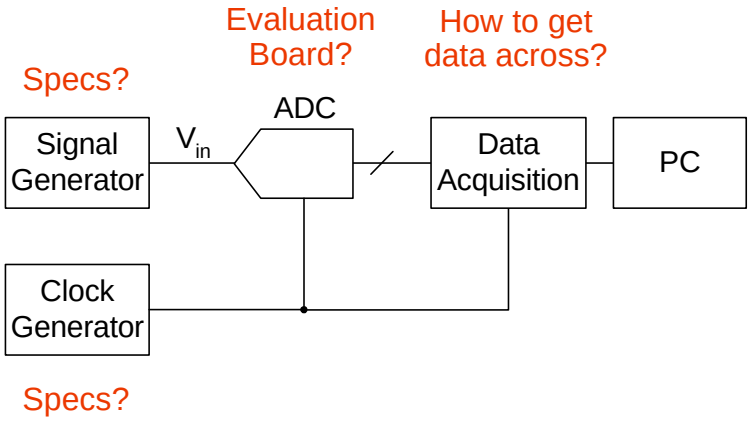


- Beware of spectrum analyzer nonlinearities
- For high performance converter linearity test, may need to notch out the signal to measure the ADC linearity via spectrum analyzer
- Need to build or purchase notch filter/s

Filtering



ADC Test Setup



State-Of-The-Art ADC (2001)

Resolution	14 bits
Conversion Rate	75 MSPS
Input Range	2 V_{pp} differential
SNR @ Nyquist	73 dB
SFDR @ Nyquist	88 dB
DNL	0.6 LSB
INL	2.0 LSB

[W. Yang et al., "A 3-V 340-mW 14-b 75-Msample/s CMOS ADC with 85-dB SFDR at Nyquist input," *IEEE J. of Solid-State Circuits,* Dec. 2001]

- Your converter will perform even better...
- Testing a high performance converter may be just as challenging as designing it!
- Key to success is to be aware of test setup and equipment limitations

Signal Source

- Need: SFDR>95dB @ $f_{in}=f_s/2=37.5$MHz
- Let's see, how about the "value priced" signal generator available in most labs...

- f=0...15MHz
- Harmonic distortion (f>1MHz): -35dBc

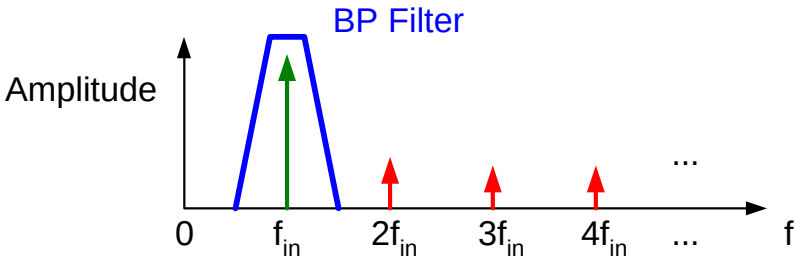
  → Does not cover the required frequency range & poor linearity

A Better Signal Source

- OK, now we've spent about $40k, this should work now... (?)

- f=100kHz...3GHz
- Harmonic distortion (f>1MHz): -30dBc !
- No way to produce the sine wave we need without a filter!

Filtering Out Harmonics



- Given HD=-30dBc, we need a stopband rejection > 65dB to get SFDR>95dB

Available Filters

Elliptical Function Bandpass Filters 1kHz to 20MHz

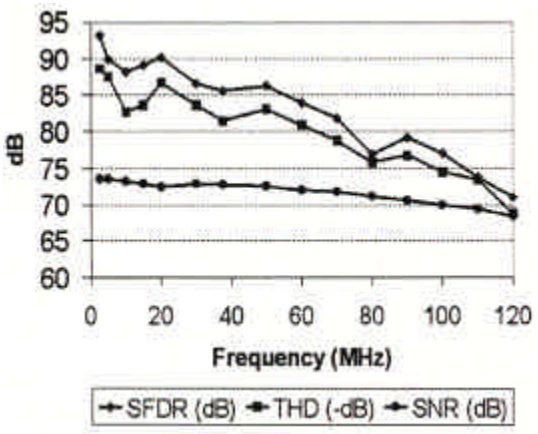
www.tte.com, or
www.allenavionics.com

Stopband to Passband Bandwidth Ratios

Series Number	BWR	*Stopband Attenuation
Q34	4.0:1	-40dBc
Q40	4.0:1	-40dBc
Q36	10.0:1	-60dBc
Q54	2.5:1	-40dBc
Q70	3.5:1	-60dBc
Q56	3.5:1	-60dBc

- Want to test at many frequencies → Need to have many different filters!

Example: ADC Linearity Test



Tunable Filter

www.klmicrowave.com

K&L Model	Frequency Range (MHz)	Passband Insertion Loss	Length Inch/mm	Width Inch/mm	Height Inch/mm
5BT-30/76-5-N/N	30-76	1.3 dB Max	9.80/249	5.38/137	2.75/50
5BT-63/125-5-N/N	63-125	1.3 dB Max	9.80/249	5.38/137	2.75/50
5BT-125/250-5-N/N	125-250	1.3 dB Max	9.80/249	5.38/137	2.75/50
5BT-250/500-5-N/N	250-500	1.0 dB Max	9.80/249	5.38/137	2.75/50
5BT-375/750-5-N/N	375-750	1.0 dB Max	9.80/249	5.38/137	2.75/50
5BT-500/1000-5-N/N	500-1000	1.0 dB Max	9.80/249	5.38/137	2.75/50
5BT-750/1500-5-N/N	750-1500	1.0 dB Max	9.80/249	5.38/137	2.75/50
5BT-1000/2000-5-N/N	1000-2000	1.0 dB Max	7.38/187	2.88/73	2.75/50
5BT-1200/2600-5-N/N	1200-2600	1.0 dB Max	7.38/187	2.88/73	2.75/50

Filter Distortion

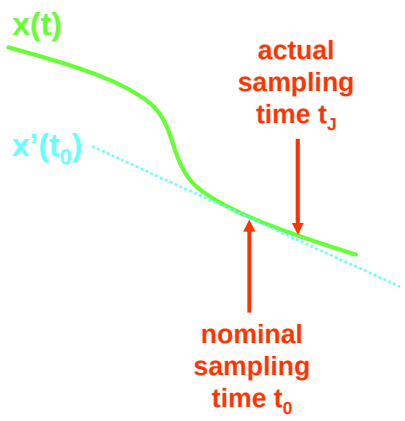
- Beware: The filters themselves also introduce distortion
- Distortion is usually not specified, need to call manufacturer
- Often guaranteed: HD<-85dBc,
- Don't trust your filters blindly...

Clock Generator

- Let us check if for the clock a "value-priced" signal generator will suffice...
- No! The clock signal controls sampling instants – which we assumed to be precisely equi-distant in time (period T)
- Variability in T causes errors
  - "Aperture Uncertainty" or "Aperture Jitter"
- How much Jitter can we tolerate?

Clock Jitter

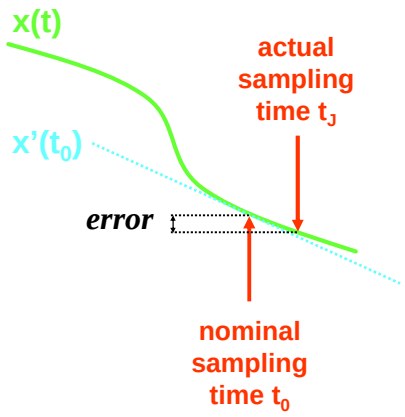
- Sampling jitter adds an error voltage proportional to the product of $(t_J - t_0)$ and the derivative of the input signal at the sampling instant
- Jitter doesn't matter when sampling dc signals ($x'(t_0)=0$)



Clock Jitter

- The error voltage is

$$e = x'(t_0)(t_J - t_0)$$



Jitter Example

Sinusoidal input

$$\begin{aligned} &Amplitude: && A \\ &Frequency: && f_x \\ &Jitter: && dt \end{aligned}$$

$$x(t) = A\sin(2\pi f_x t)$$

$$x'(t) = 2\pi f_x A\cos(2\pi f_x t)$$

$$|x'(t)|_{max} \le 2\pi f_x A$$

$$|e(t)| \le |x'(t)|\,dt$$

$$|e(t)| \le |2\pi f_x A|\,dt$$

Worst case

$$A = A_{FS}/2 \qquad f_x = f_s/2$$

$$|e(t)| << \frac{\Delta}{2} \cong \frac{A_{FS}}{2^{B+1}}$$

$$dt << \frac{1}{2^B \pi f_s}$$

# of Bits	f_s	dt <<
16	10 MHz	0.5 ps
12	100 MHz	0.8 ps
8	1000 MHz	1.2 ps

Law of Jitter

- The worst case looks pretty stringent …
  what about the "average"?
- Let's calculate the mean squared jitter error (variance)
- If we're sampling a sinusoidal signal

  $x(t) = A\sin(2\pi f_x t)$,

  then
  - $x'(t) = 2\pi f_x A\cos(2\pi f_x t)$
  - $E\{[x'(t)]^2\} = 2\pi^2 f_x^2 A^2$
- Assume the jitter has variance $E\{(t_J - t_0)^2\} = \tau^2$

Law of Jitter

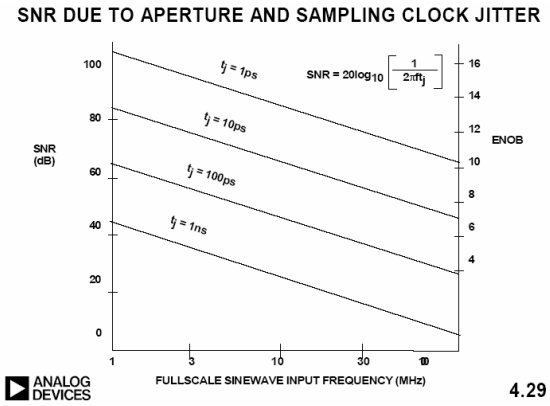
- If $x'(t)$ and the jitter are independent
  - $E\{[x'(t)(t_J - t_0)]^2\} = E\{[x'(t)]^2\}\, E\{(t_J - t_0)^2\}$
- Hence, the jitter error power is

  $$\mathbf{E\{e^2\} = 2\pi^2 f_x^2 A^2 \tau^2}$$
- If the jitter is uncorrelated from sample to sample, this "jitter noise" is white

Law of Jitter

$$DR_{\text{jitter}} = \frac{A^2/2}{2p^2 f_x^2 A^2 t^2} = \frac{1}{2p^2 f_x^2 t^2} = -20\log_{10}(2pf_x t)$$

ADC under test:
SNR=73dB
f_{in}=37.5MHz
$\Rightarrow \tau$<<1ps rms !



More on Jitter

- Once we have a good enough generator, other circuit and test setup related issues may determine jitter, but...
- Usually, clock jitter in the single-digit pico-second range can be prevented by appropriate design techniques
  - Separate supplies
  - Separate analog and digital clocks
  - Short inverter chains between clock source and destination
- Few, if any, other analog-to-digital conversion non-idealities have the same symptoms as sampling jitter:
  - RMS noise proportional to input frequency
  - RMS noise proportional to input amplitude

  →In cases where clock jitter limits the dynamic range, it's easy to tell, but may be difficult to fix...

Evaluation Board

- Planning begins with converter pin-out
  - Example of poor pin-out→ clock pin right next to a digital output...
- Not "Black Magic", but weeks of design time and studing
- Key aspects
  - Supply/ground routing, bypass capacitors
  - Coupling between signals
- Good idea to look at ADC vendor datasheets for example layouts/schematics/application notes

Vendor Eval Board Layout

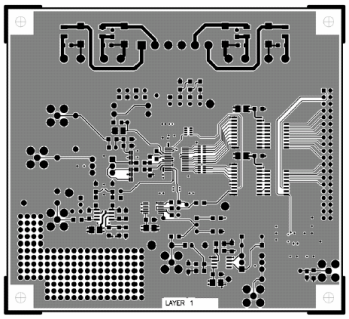


Figure 21. TSSOP Evaluation Board Layout, Primary Side

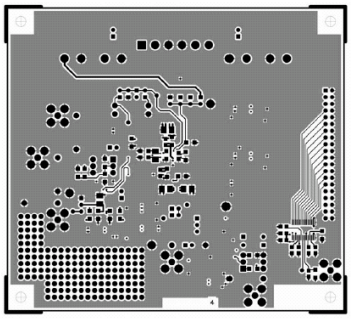


Figure 22. TSSOP Evaluation Board Layout, Secondary Side

[Analog Devices AD9235 Data Sheet]

One thing to remember...

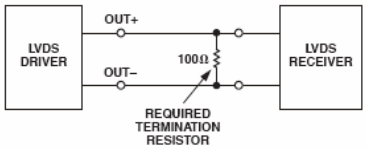
- A converter does not just have one "input"
  - Clock
  - Power Supply, Ground
  - Reference Voltage
- For good practices on how to avoid issues see e.g.:
  - Analog Devices Application Note 345**:** "Grounding for Low-and-High-Frequency Circuits"
  - Maxim Application Note 729**:** "Dynamic Testing of High-Speed ADCs, Part 2"

How to Get the Bits Off Chip?

- "Full swing" CMOS signaling works well for f_{CLK}<100MHz
- But we want to build faster ADCs...
- Alternative to CMOS: LVDS – Low Voltage Differential Signaling
- LVDS vs. CMOS:
  - Higher speed, more power efficient at high speed
  - Two pins/bit!

LVDS Outputs

Figure 1. LVDS Output Levels



Analog Devices Application Note 586: "LVDS Data Outputs for High Speed ADCs"

LVDS Outputs

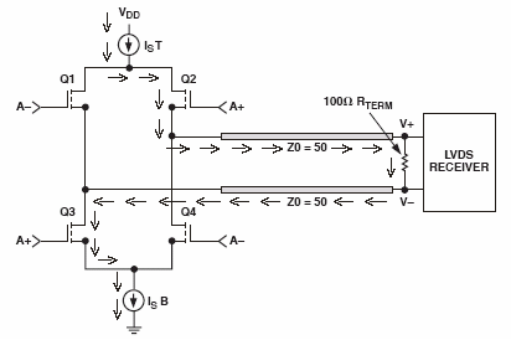
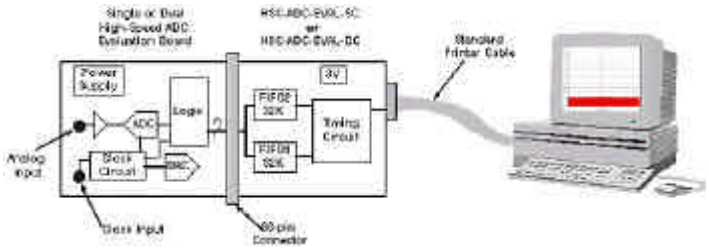


Figure 4. LVDS Output Current

Analog Devices Application Note 586: "LVDS Data Outputs for High Speed ADCs"

Data Acquisition

- Several options:
  - Logic analyzer with PC interface
  - FIFO board, interface to PC DAQ card
  - Vendor kit, simple interface to printer port:



[Analog Devices, High-Speed ADC FIFO Evaluation Kit]