EE247
Lecture 10
Switched-Capacitor Filters

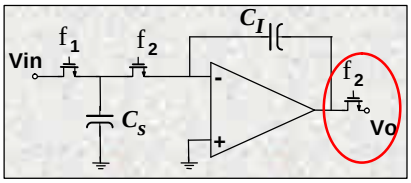
- Summary of last lecture
- Switched-capacitor filter design considerations
- Switched-capacitor filters utilizing double sampling technique
- Effect of non-idealities
- Bilinear switched-capacitor filters
- Filter design summary

Summary of last lecture
Switched-Capacitor Filters

- LDI integrators
  - Effect of parasitic capacitance
  - Bottom-plate integrator topology
- Resonators
- Bandpass filters
- Lowpass filters
  - Termination implementation
  - Transmission zero implemention

LDI SC Integrator

LDI (Lossless Discrete Integrator) → same as DDI but output is sampled ½ clock cycle earlier



LDI

$$\frac{V_O}{V_{in}}(Z) = -\frac{C_s}{C_I} \times \frac{Z^{-1/2}}{1-Z^{-1}}, \quad Z = e^{jwT}$$

$$= -\frac{C_s}{C_I} \times \frac{e^{-jwT/2}}{1-e^{-jwT}} = \frac{C_s}{C_I} \times \frac{1}{e^{-jwT/2}-e^{+jwT/2}}$$

$$= -j\frac{C_s}{C_I} \times \frac{1}{2\sin(wT/2)}$$

$$= -\frac{C_s}{C_I}\frac{1}{jwT} \times \frac{wT/2}{\sin(wT/2)}$$

Ideal Integrator) Magnitude Error

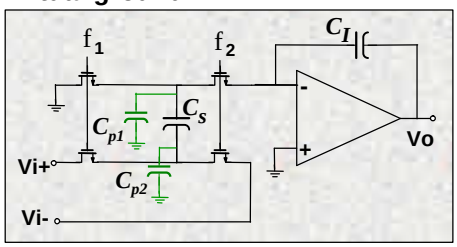
No Phase Error!
For signals at frequency <<sampling freq.
→ Magnitude error negligible

Parasitic Insensitive Bottom-Plate SC Integrator

Sensitive parasitic cap. → C_{p1} → rearrange circuit so that C_{p1} does not charge/discharge

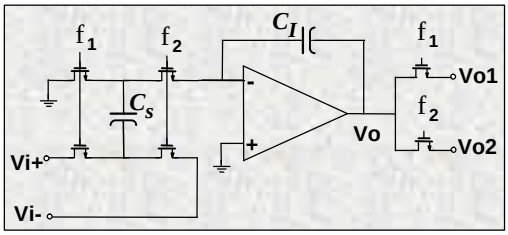
f1=1 → capacitor grounded

f2=1 → capacitor at virtual ground



Solution: Bottom plate capacitor integrator

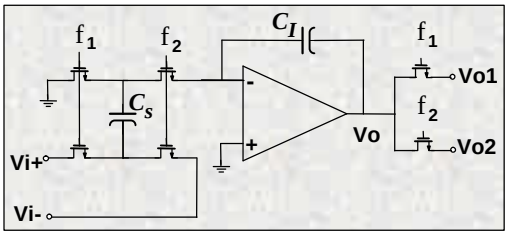
Bottom Plate S.C. Integrator

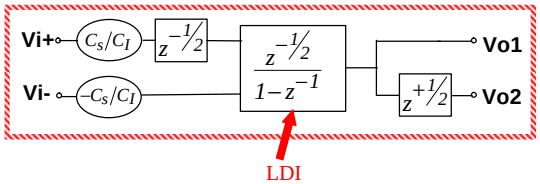


Input/Output z-transform
Note: Delay from Vi+ and Vi- to output is different
→ Special attention needed to input/output connections

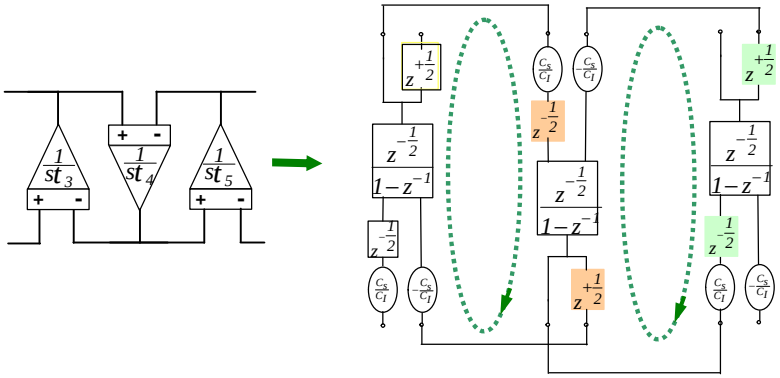
	Vo1 on f**1**	Vo2 on f**2**
Vi+ on f**1**	$\frac{z^{-1}}{1-z^{-1}}$	$\frac{z^{-1/2}}{1-z^{-1}}$
Vi- on f**2**	$\frac{z^{-1/2}}{1-z^{-1}}$	$\frac{-1}{1-z^{-1}}$

Bottom Plate S.C. Integrator z-Transform Model





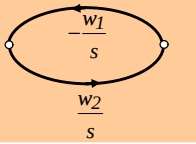
LDI Switched Capacitor Ladder Filter

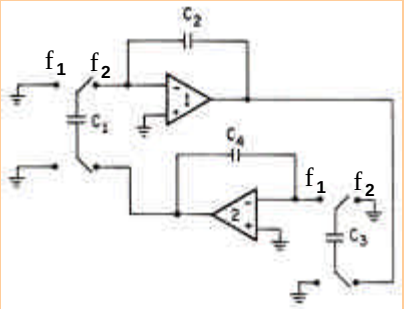


Delay around integ. Loop is ($Z^{-1/2} \times Z^{+1/2} = 1$) ➔ LDI function

Switched Capacitor LDI Resonator

Resonator Signal Flowgraph



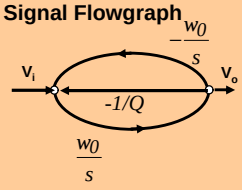


$$w_1 = \frac{1}{R_{eq1} C_2} = f_s \times \frac{C_1}{C_2}$$

$$w_2 = \frac{1}{R_{eq3} C_4} = f_s \times \frac{C_3}{C_4}$$

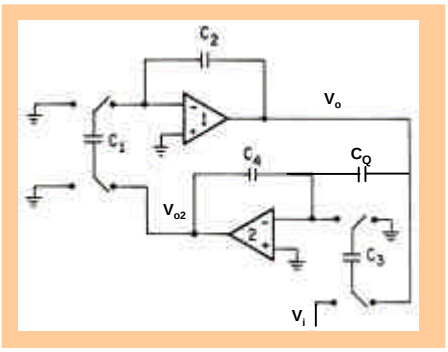
Switched Capacitor LDI Bandpass Filter Continuous-Time Termination

Bandpass Filter Signal Flowgraph

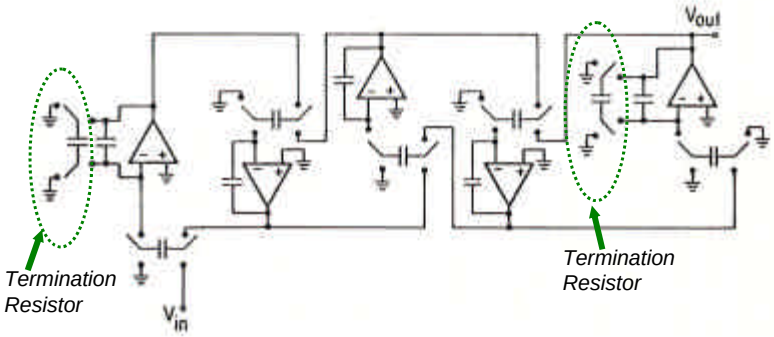


$$w_0 = s \times \frac{C_3}{C_4} = f_s \times \frac{C_1}{C_2}$$

$$Q = \frac{C_4}{C_Q}$$



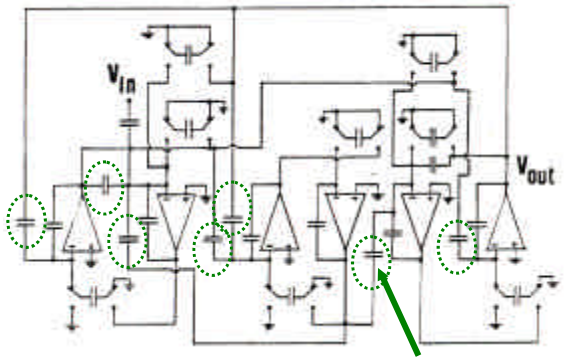
Fifth Order All-Pole LDI Low-Pass Ladder Filter Complex Conjugate Terminations



•Complex conjugate terminations (alternate phase switching)

Ref: Tat C. Choi, "High-Frequency CMOS Switched-Capacitor Filters," U. C. Berkeley, Department of Electrical Engineering, Ph.D. Thesis, May 1983 (ERL Memorandum No. UCB/ERL M83/31).

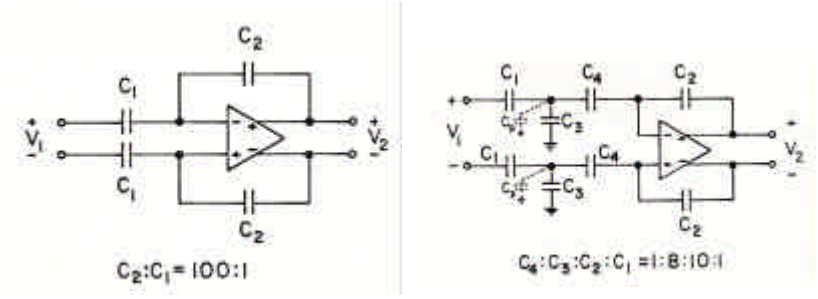
Sixth Order Elliptic LDI Bandpass Filter



Transmission Zero

Ref: Tat C. Choi, "High-Frequency CMOS Switched-Capacitor Filters," U. C. Berkeley, Department of Electrical Engineering, Ph.D. Thesis, May 1983 (ERL Memorandum No. UCB/ERL M83/31).

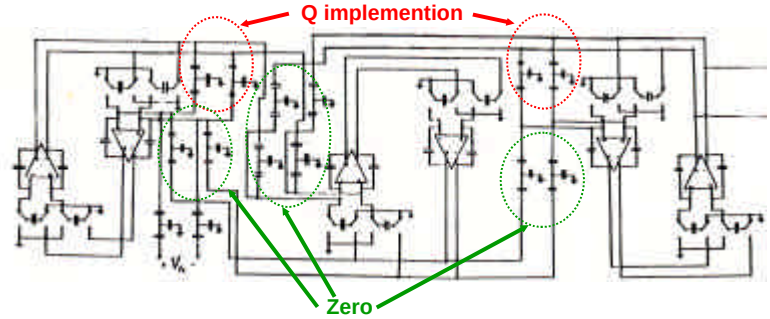
Use of T-Network



High Q filter → large cap. ratio for Q & transmission zero implementation
To reduce large ratios required → T-networks utilized

Ref: Tat C. Choi, "High-Frequency CMOS Switched-Capacitor Filters," U. C. Berkeley, Department of Electrical Engineering, Ph.D. Thesis, May 1983 (ERL Memorandum No. UCB/ERL M83/31).

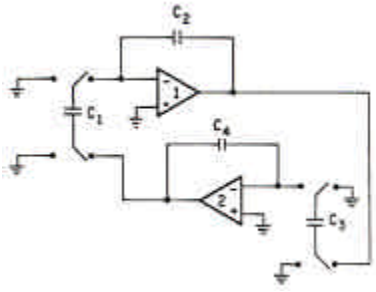
Sixth Order Elliptic Bandpass Filter Utilizing T-Network



- **T-networks utilized** for:
  - **Q implemention**
  - **Transmission zero implementation**

Ref: Tat C. Choi, "High-Frequency CMOS Switched-Capacitor Filters," U. C. Berkeley, Department of Electrical Engineering, Ph.D. Thesis, May 1983 (ERL Memorandum No. UCB/ERL M83/31).

S.C. Resonator

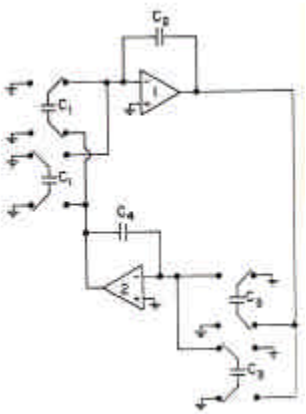


Regular sampling
Each opamp busy settling only during one of the clock phases
→ Idle during the other clock phase

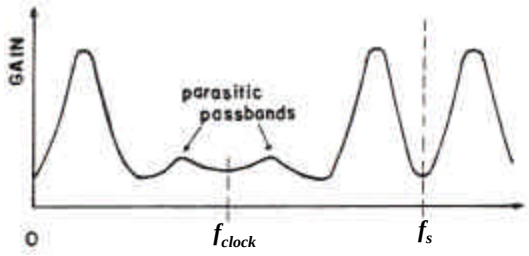
S.C. Resonator Using Double-Sampling

Double-sampling:

- **2nd set of switches & sampling caps added to all integrators**
- **While one set of switches/caps sampling the other one transfers charge into the intg. cap**
- **Opamps busy during both clock phases**
- **Effective sampling freq. twice clock freq. while opamp bandwidth stays the same**



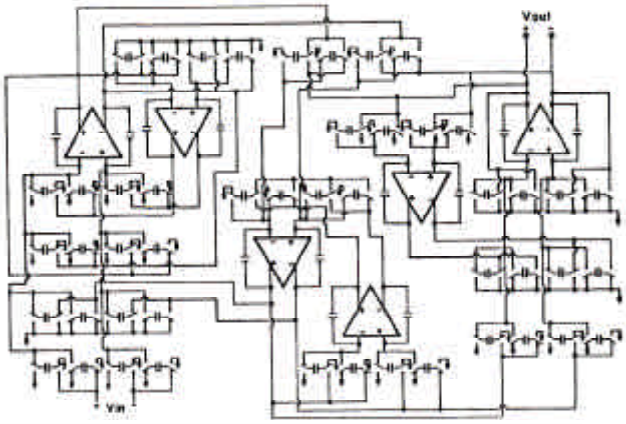
Double-Sampling Issues



Issues to be aware of:
- Jitter in the clock
- Unequal clock phases
-Mismatch in sampling caps.
→ parasitic passbands

Ref: Tat C. Choi, "High-Frequency CMOS Switched-Capacitor Filters," U. C. Berkeley, Department of Electrical Engineering, Ph.D. Thesis, May 1983 (ERL Memorandum No. UCB/ERL M83/31).

Double-Sampled Fully Differential S.C. 6th Order All-Pole Bandpass Filter



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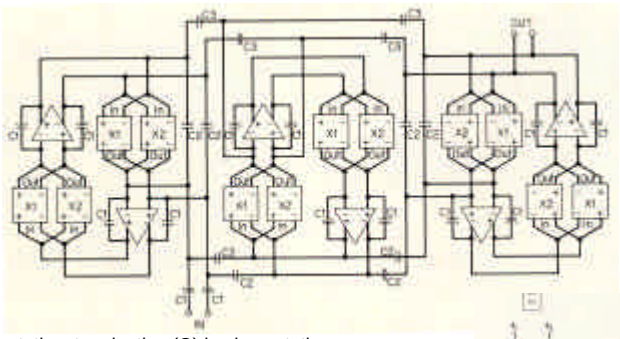
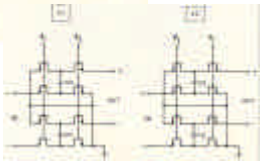
Double-Sampled Fully Differential 6th Order S.C. All-Pole Bandpass Filter





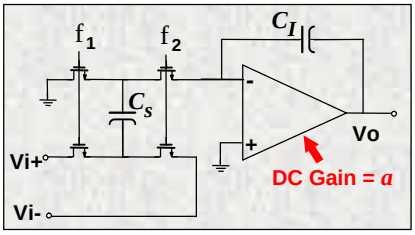
-Cont. time termination (Q) implementation
-Folded-Cascode opamp with f_t = *100MHz* used
-Center freq. *3.1MHz*, filter *Q=55*
-Clock freq. *12.83MHz* → effective oversampling ratio *8.27*
-Measured dynamic range *46dB* (*IM3=1%)*

Ref: B.S. Song, P.R. Gray "Switched-Capacitor High-Q Bandpass Filters for IF Applications," *IEEE Journal of Solid State Circuits*, Vol. 21, No. 6, pp. 924-933, Dec. 1986.

Effect of Opamp Nonidealities on Switched Capacitor Filter Behaviour

- Opamp finite gain
- Opamp finite bandwidth
- Finite slew rate of the opamp

Effect of Opamp Non-Idealities Finite DC Gain



$$H(s) \approx -f_s \frac{C_s}{C_I} \frac{1}{s + f_s \frac{C_s}{C_I} \times \frac{1}{a}}$$

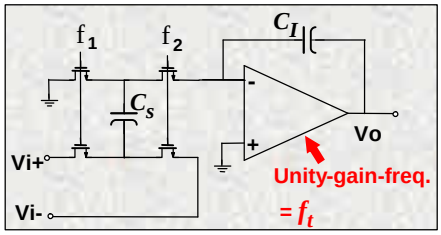
$$H(s) \approx \frac{-w_o}{s + w_o \times \frac{1}{a}}$$

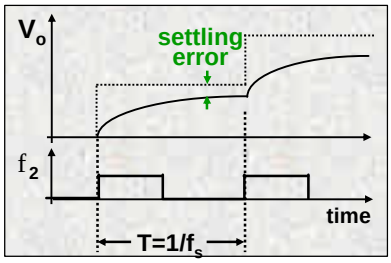
$$Q \approx \frac{a \times w}{w_o}$$

$$\Rightarrow \boxed{Q \approx a}$$

→**Finite DC gain same effect in SC filters compared to CT filters**

Effect of Opamp Non-Idealities
Finite Opamp Bandwidth





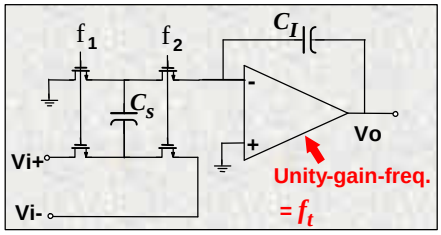
Assumption-

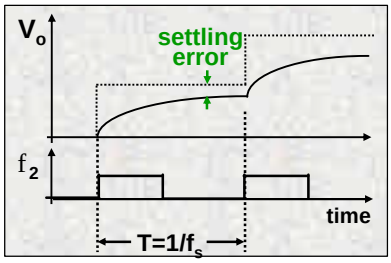
Opamp → does not slew

Opamp has only one pole → exponential settling

Ref: K.Martin, A. Sedra, "Effect of the OPamp Finite Gain & Bandwidth on the Performance of Switched-Capacitor Filters," IEEE Trans. Circuits Syst., vol. CAS-28, no. 8, pp. 822-829, Aug 1981.

Effect of Opamp Non-Idealities
Finite Opamp Bandwidth





$$H_{actual}(Z) \approx H_{ideal}(Z)\left[1 - e^{-k} + e^{-k} \times \frac{C_I}{C_I + C_S} Z^{-1}\right]$$

$$where \quad k = p \times \frac{C_I}{C_I + C_S} \times \frac{f_t}{f_s}$$

$f_t \rightarrow$ Opamp unity-gain-frequency , $f_s \rightarrow$ Clock frequency

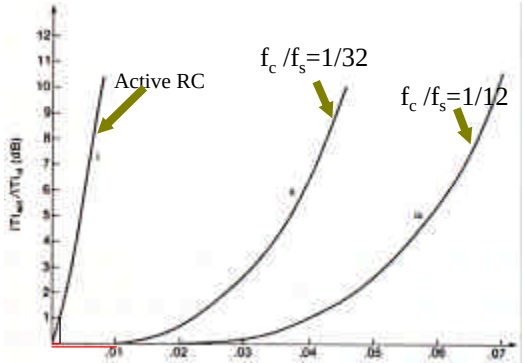
Ref: K.Martin, A. Sedra, "Effect of the Opamp Finite Gain & Bandwidth on the Performance of Switched-Capacitor Filters," IEEE Trans. Circuits Syst., vol. CAS-28, no. 8, pp. 822-829, Aug 1981.

Effect of Opamp Finite Bandwidth on Filter Magnitude Response

$|T|_{non\text{-}ideal} / |T|_{ideal}$ (dB)

Magnitude deviation due to finite opamp unity-gain-frequency

Example: 2nd order bandpass with Q=25



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Effect of Opamp Finite Bandwidth on Filter Magnitude Response

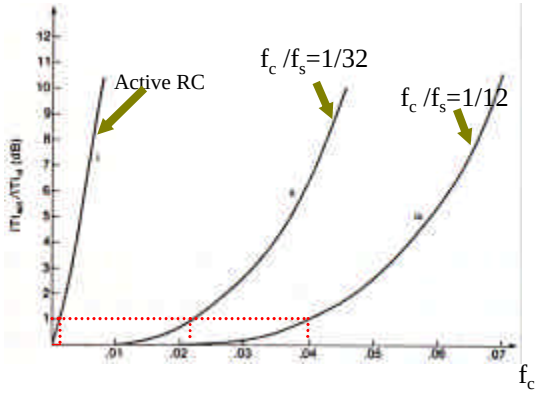
$|T|_{non\text{-}ideal} / |T|_{ideal}$ (dB)

Example:
For 1dB magnitude response deviation:

1- f_c/f_s=1/12
f_c/f_t~0.04
→ $f_t > 25 f_c$

2- f_c/f_s=1/32
f_c/f_t~0.022
→ $f_t > 45 f_c$

3- *Cont.-Time*
f_c/f_t~1/700
→ $f_t > 700 f_c$



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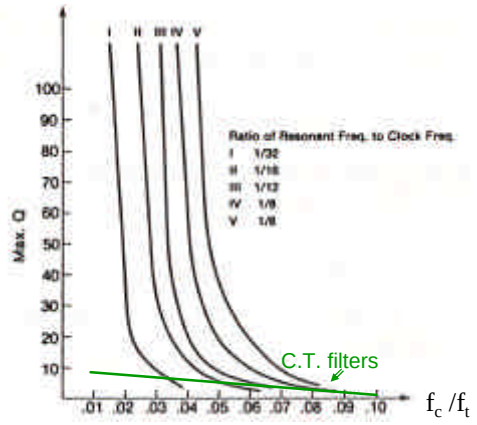
Effect of Opamp Finite Bandwidth
Maximum Achievable Q

Max. allowable biquad Q for peak gain change <10%



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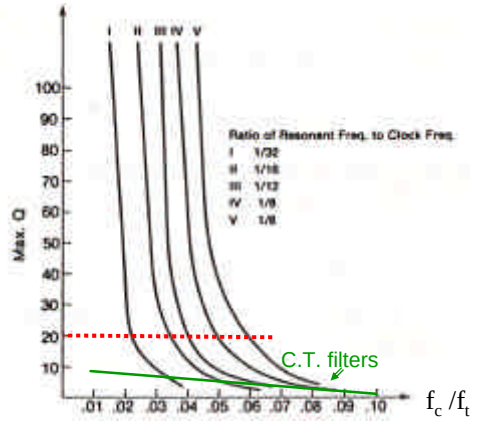
Effect of Opamp Finite Bandwidth
Maximum Achievable Q

Example:
For Q of 20 required
Max. allowable biquad Q
for peak gain change <10%

1- $f_c/f_s=1/32$
$f_c/f_t \sim 0.022$
→ $f_t > 45 f_c$

2- $f_c/f_s=1/12$
$f_c/f_t \sim 0.04$
→ $f_t > 25 f_c$

3- $f_c/f_s=1/6$
$f_c/f_t \sim 0.062$
→ $f_t > 16 f_c$



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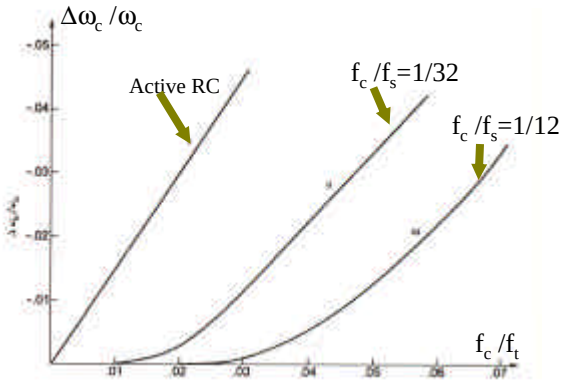
Effect of Opamp Finite Bandwidth on Filter Critical Frequency

Critical frequency deviation due to finite opamp unity-gain-frequency

Example: 2nd order filter



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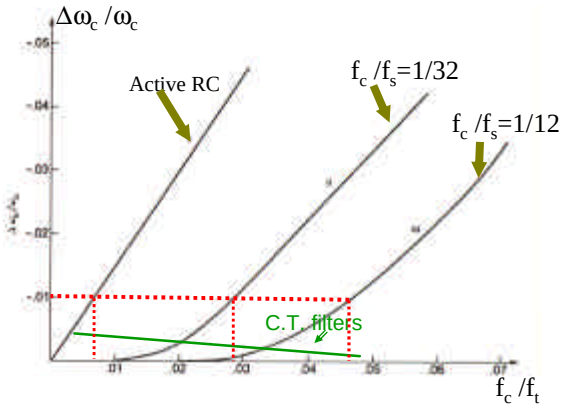
Effect of Opamp Finite Bandwidth on Filter Critical Frequency

Example:
For maximum critical frequency shift of <1%

1- $f_c/f_s=1/32$
$f_c/f_t\sim0.028$
→ $f_t>36f_c$

2- $f_c/f_s=1/12$
$f_c/f_t\sim0.046$
→ $f_t>22f_c$

3- *Active RC*
$f_c/f_t\sim0.008$
→ $f_t>125f_c$



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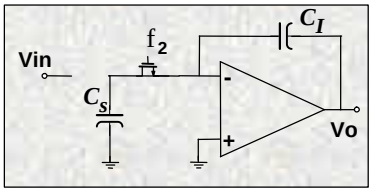
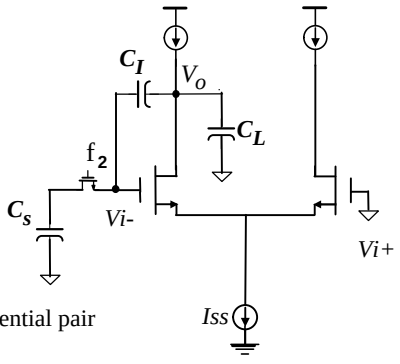
Sources of Distortion in Switched-Capacitor Filters

- Opamp gain non-linearity
- Capacitor non-linearity
- Distortion incurred by finite setting time of the opamp
- Distortion induced by finite slew rate of the opamp
- Distortion due to switch clock feed-through and charge injection

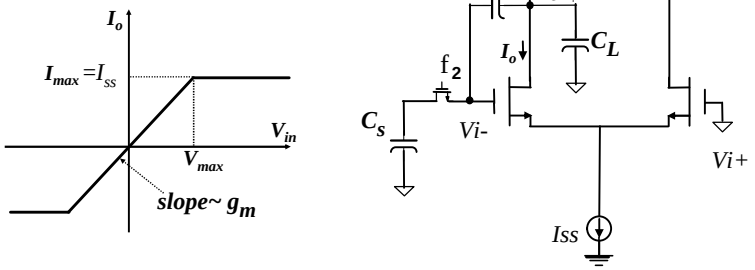
What is Slewing?





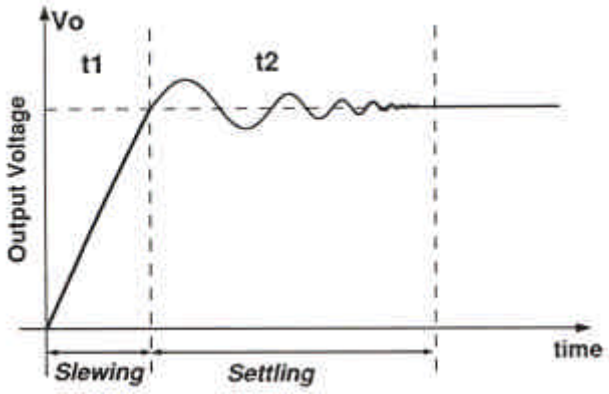
Assume opamp is of a simple differential pair class A transconductance type

Why Slew?

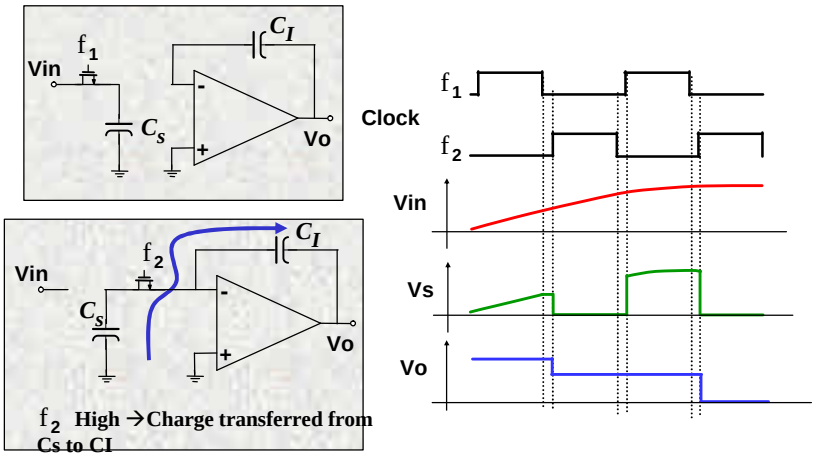


$V_{cs} > V_{max}$ → Output current constant $I_o = Iss$ → *Slewing*
After Vcs is discharged enough to have Vcs<Vmax → Linear settling

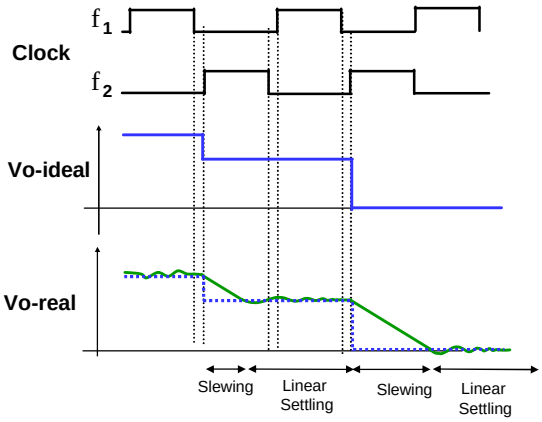
Distortion Induced by Finite Slew Rate of the Opamp



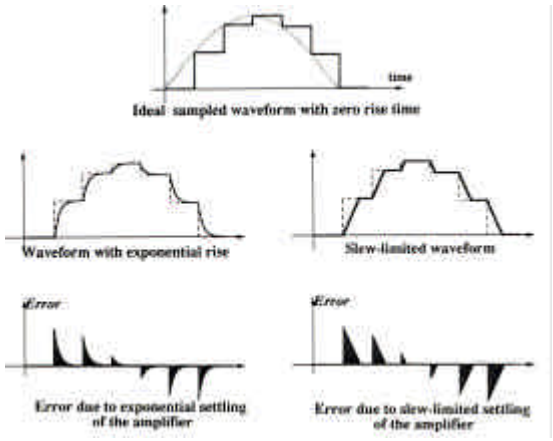
Ideal S.C.Output Waveform



Slew Limited Switched-Capacitor Output Settling



Distortion Induced by Finite Slew Rate of the Opamp



Ref: K.L. Lee, "Low Distortion Switched-Capacitor Filters," U. C. Berkeley, Department of Electrical Engineering, Ph.D. Thesis, Feb. 1986 (ERL Memorandum No. UCB/ERL M86/12).

Distortion Induced by Finite Slew Rate of the Opamp

- Error due to exponential settling changes linearly with signal amplitude
- Error due to slew-limited settling changes non-linearly with signal amplitude (doubling signal amplitude X4 error)

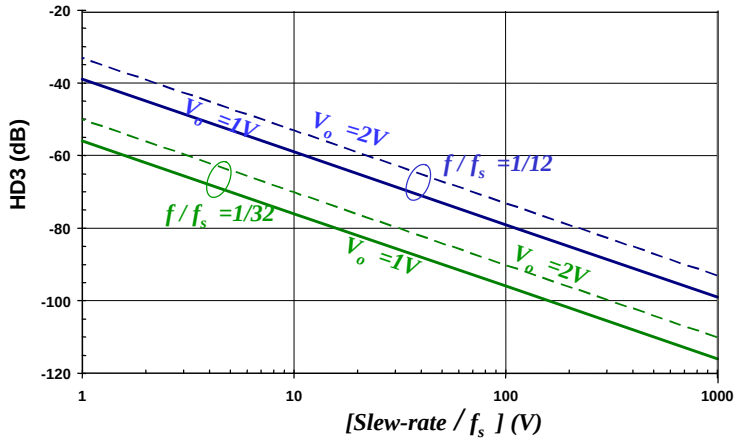
  →For high-linearity need to have either high slew rate or non-slewing opamp

$$HD_k = \frac{V_o}{S_r T_s} \frac{8\left(\sin {w_o T_s}/{2}\right)^2}{pk\left(k^2-4\right)}$$

$$\rightarrow HD_3 = \frac{V_o}{S_r T_s} \frac{8\left(\sin {w_o T_s}/{2}\right)^2}{15p}$$

Ref: K.L. Lee, "Low Distortion Switched-Capacitor Filters," U. C. Berkeley, Department of Electrical Engineering, Ph.D. Thesis, Feb. 1986 (ERL Memorandum No. UCB/ERL M86/12).

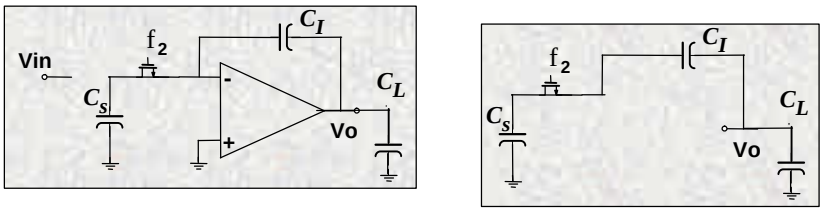
Distortion Induced by Finite Slew Rate of the Opamp Example



Distortion Induced by Finite Slew Rate of the Opamp

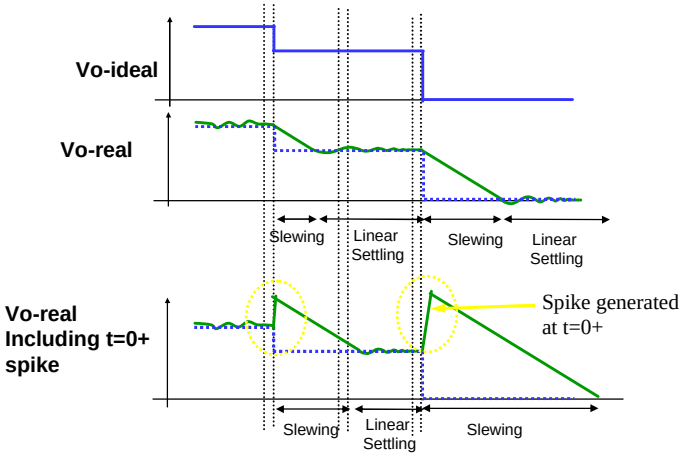
- Note that for a high order switched capacitor filter → only the last stage slewing will affect the output linearity (as long as the previous stages settle to the required accuracy)
  - → Can reduce slew limited linearity by using an amplifier with a higher slew rate *only* for the last stage
  - → Can reduce slew limited linearity by using class A/B amplifiers
    - Even though the output/input characteristics is non-linear the significantly higher slew rate compared to class A amplifiers helps improved slew rate induced distortion
- In cases where the output is sampled by another sampled data circuit (e.g. an ADC or a S/H) → no issue with the slewing of the output as long as the output settles to the required accuracy & is sampled at the right time

More Realistic Switched-Capacitor Circuit Slew Scenario



At the instant *Cs* connects to input of opamp
→Opamp not yet active at t=0+ due to finite opamp delay
→Feedforward path from input to output generates a voltage spike at the output
→Eventually, opamp becomes active- slewing starts

More Realistic SC Slew Scenario



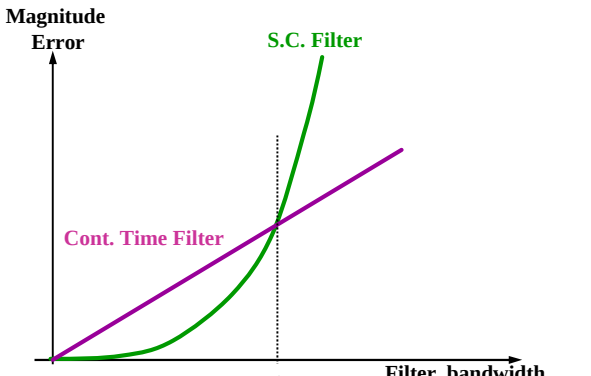
Ref: R. Castello, "Low Voltage, Low Power Switched-Capacitor Signal Processing Techniques," U. C. Berkeley, Department of Electrical Engineering, Ph.D. Thesis, Aug. 1984 (ERL Memorandum No. UCB/ERL M84/67).

Sources of Noise in Switched-Capacitor Filters

- Opamp Noise
  - Thermal noise
  - 1/f noise
- Thermal noise associated with the switching process (kT/C)
  - Same as continuous-time filters
- Precaution regarding aliasing of noise required

S.C. Filters versus Continuous-Time Filter Limitations

Considering overall effects:
-Opamp finite unity-gain-bandwidth
- Opamp settling issues
-Opamp finite slew rate
- Clock feedthru
- Switch+ sampling cap. Time-constant



Assuming constant opamp f_t

→ Limited S.C. filter performance frequency range

Bilinear Transform

- Bilinear integrator $v_o(kT) = v_o(kT-T) + \frac{T}{2}\left[v_i(kT) + v_i(kT-T)\right]$

$$\left[1-z^{-1}\right]V_o(z) = \frac{T}{2}\left[1+z^{-1}\right]V_i(z)$$

$$H(z) = \frac{V_o(z)}{V_i(z)} = \frac{T}{2}\frac{1+z^{-1}}{1-z^{-1}}$$

- Frequency translation

$$\left.\frac{1}{s}\right|_{s=2p\,jf_{RC}} = H_{SC}(z)\Big|_{z=e^{2p\,jf_{SC}T}}$$

Bilinear

$$f_{RC} = \frac{f_s}{p}\tan\left(p\,\frac{f_{SC}}{f_s}\right)$$

LDI

$$f_{RC} = \frac{f_s}{p}\sin\left(p\,\frac{f_{SC}}{f_s}\right)$$

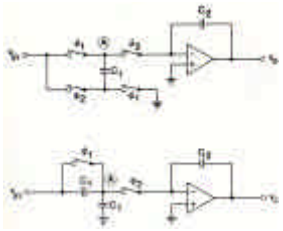
Bilinear Integrator

-Not implemented by "standard" SC integrators

-Synthesis:

Biquads: direct coefficient comparison

Example: SC integrator:



$$H(Z) = -\frac{C_S}{C_I}\times\frac{1+Z^{-1}}{1-Z^{-1}}$$

$$= -\frac{C_S}{C_I}\times\frac{1+e^{-jwT}}{1-e^{-jwT}}$$

$$= \frac{C_S}{C_I}\,\frac{1}{jwT_S}\,\frac{wT_S}{tan\,wT_S/2}$$

Ideal Integrator

Magnitude Error

No Phase Error!

For signals at frequency <<sampling freq.

→ Magnitude error negligible

Ref: R. Gregorian, G. Temes, "Analog CMOS Integrated Circuits," Wiley, 1986, pp 277 .

LDI & Bilinear Transformation
Frequency Warping

LDI :

$$\frac{1}{s} \quad \Rightarrow \quad \frac{Z^{-1/2}}{1-Z^{-1}} = \frac{T_s}{2}\frac{1}{j\sin wT_s/2}$$

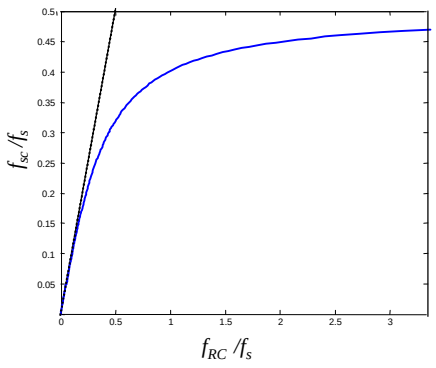
$$s \quad \Rightarrow \quad \frac{2}{T_s} j\sin wT_s/2$$

Bilinear

$$\frac{1}{s} \quad \Rightarrow \quad \frac{1+Z^{-1}}{1-Z^{-1}} = \frac{1+e^{-jwT}}{1-e^{-jwT}} = \frac{T_s}{2}\frac{1}{j\tan wT_s/2}$$

$$s \quad \Rightarrow \quad \frac{2}{T_s} j\tan wT_s/2$$

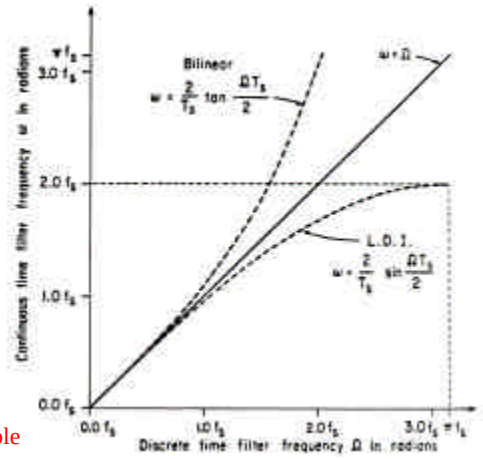
Bilinear Transform



$$f_{RC} = \frac{f_s}{p}\tan\left(p\frac{f_{SC}}{f_s}\right)$$

- Entire jω axis maps onto the unit circle
- Mapping is nonlinear (tan distortion)
  → prewarp specifications of RC prototype
  Matlab filter design automates this (see, e.g. `bilinear`)

Bilinear & LDI Transformation Frequency Warping



As long as $f \ll f_s$ error negligible

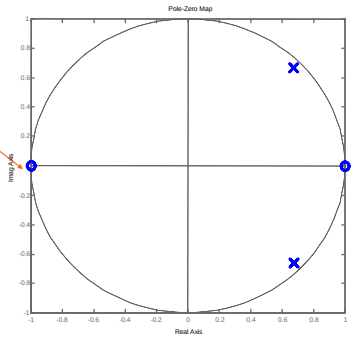
"Bilinear" Bandpass

$f_s = 100\text{kHz}$

$f_c = f_s/8$

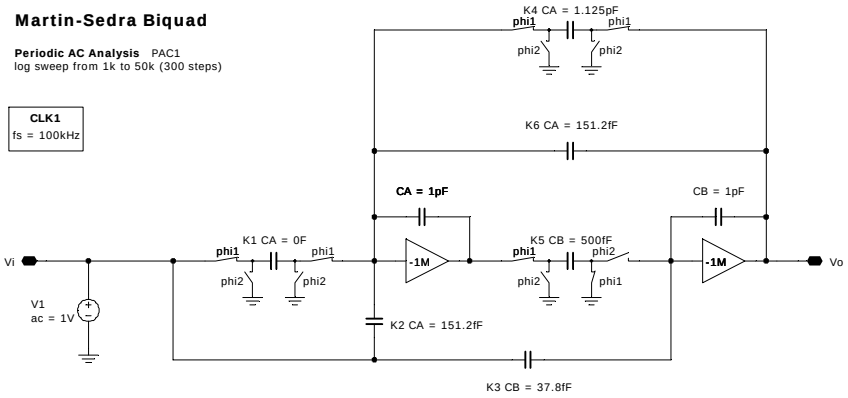
$Q = 10$

zero at $f_s/2$



Matlab:

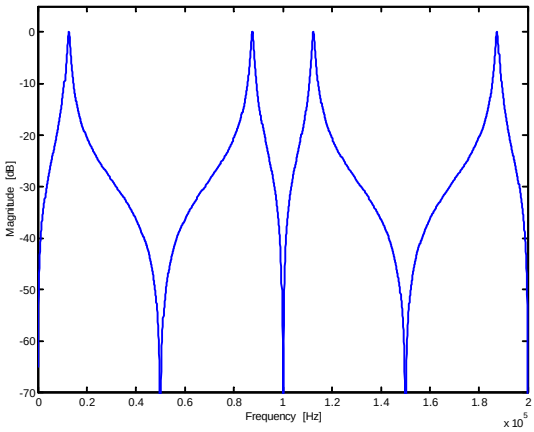
$$H(z) = \frac{0.0378\,z^2 - 0.0378}{z^2 - 1.362\,z + 0.9244}$$



$$\frac{V_o(z)}{V_i(z)} = \frac{K_3 z^2 + (-2K_3 + K_1K_5 + K_2K_5)z + (K_3 - K_2K_5)}{z^2 + (-2 + K_4K_5 + K_5K_6)z + (1 - K_5K_6)}$$

Ref: K. Martin and A. S. Sedra, "Strays-insensitive switched-capacitor filters based on the bilinear z transform," Electron. Lett., vol. 19, pp. 365-6, June 1979.

Magnitude Response



LD vs Bilinear Transform

- LDI transform:
  - Realized by “standard” SC integrators
  - Some high frequency zeros are lost
  - Simple filter synthesis:
    - Replace RC integrators with SC integrators
    - Ensure that inverting and non-inverting integrators alternate in loops
- Bilinear transform
  - Maps entire $j\omega$ axis onto unit circle (nonlinear mapping)
  - Not implemented by “standard” SC integrators
  - Synthesis:
    - Biquads: direct coefficient comparison
    - Ladders: see
      R. B. Datar and A. S. Sedra, “Exact design of strays-insensitive switched capacitor high-pass ladder filters”, Electron. Lett., vol. 19, no 29, pp. 1010-12, Nov. 1983.

SC Filter Summary

- ✓ Pole and zero frequencies proportional to
  - Sampling frequency f_s
  - Capacitor ratios
  - ➢ High accuracy and stability in response
  - ➢ Long time constants realizable without large R, C
- ✓ Compatible with transconductance amplifiers
  - Reduced circuit complexity, power
- ✓ Amplifier bandwidth requirements less stringent comparable to CT filters (low freqs only)
- ☹ Issue: Sampled data filter → require anti-aliasing prefiltering

Summary
Filter Performance verus Topology

	Max. Usable Bandwidth	SNDR	Freq. tolerance w/o tuning	Freq. tolerance + tuning
Opamp-RC	~10MHz	60-90dB	+-30-50%	1-5%
Opamp-MOSFET-C	~ 5MHz	40-60dB	+-30-50%	1-5%
Opamp-MOSFET-RC	~ 5MHz	50-90dB	+-30-50%	1-5%
Gm-C	~ 100MHz	40-70dB	+-30-50%	1-5%
Switched Capacitor	~ 10MHz	40-90dB	<<1%	_