EE247
Lecture 9
Switched-Capacitor Filters

- Summary of last lecture
- DDI integrators
- LDI integrators
  - Effect of parasitic capacitance
  - Bottom-plate integrator topology
- Resonators
- Bandpass filters
- Lowpass filters
  - Termination implementation

Summary Last Session
Switched-Capacitor Resistors

Charge transferred in one cycle:

$$Q = C(v_{IN} - v_{OUT})$$

$$i = Q/t = Qxf_s \rightarrow i = f_S C(v_{IN} - v_{OUT})$$

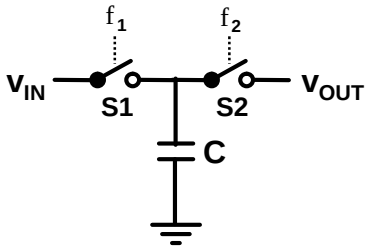
With the current through the switched capacitor resistor proportional to the voltage across it, the equivalent "switched capacitor resistance" is:

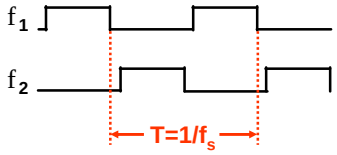
$$R_{eq} = \frac{1}{f_S C}$$

$$Example$$

$$f = 1MHz, C = 1pF$$

$$\rightarrow R_{eq} = 1Mega\Omega$$



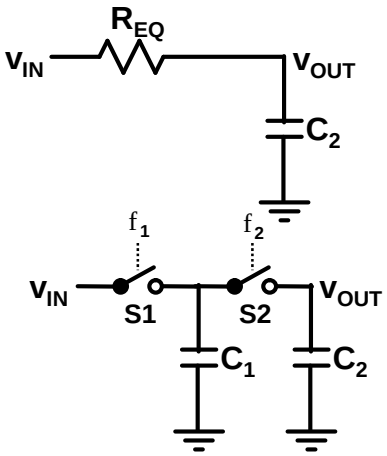


Switched-Capacitor Filter

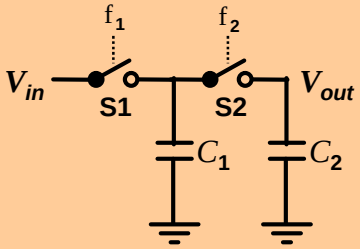
- Let's build an "SC" filter …
- We'll start with a simple RC LPF
- Replace the physical resistor by an equivalent SC resistor
- 3-dB bandwidth:

$$w_{-3dB} = \frac{1}{R_{eq}C_2} = f_s \times \frac{C_1}{C_2}$$

$$f_{-3dB} = \frac{1}{2p} f_s \times \frac{C_1}{C_2}$$

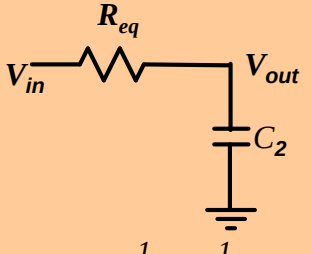


Switched-Capacitor Filter Advantage versus Continuous-Time Filters



$$f_{-3dB} = \frac{1}{2p} f_s \times \frac{C_1}{C_2}$$

- Corner freq. proportional to:
  System clock (accurate to few ppm)
  C ratio accurate → < 0.1%



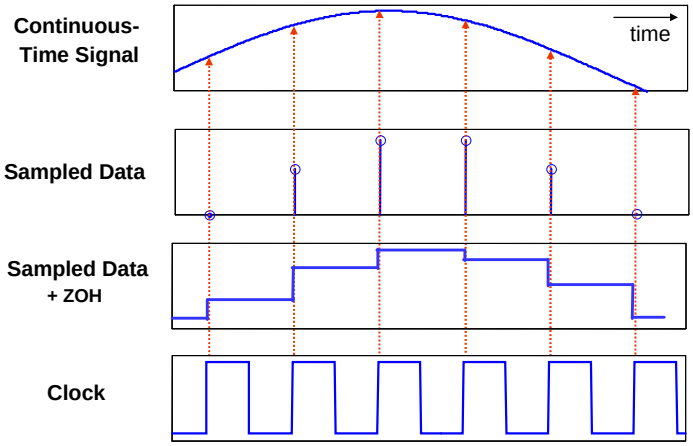
$$f_{-3dB} = \frac{1}{2p} \times \frac{1}{R_{eq}C_2}$$

- Corner freq. proportional to:
  Absolute value of Rs & Cs
  Poor accuracy → 20 to 50%

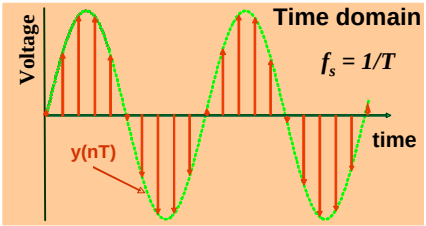
Main advantage of SC filter inherent corner frequency accuracy

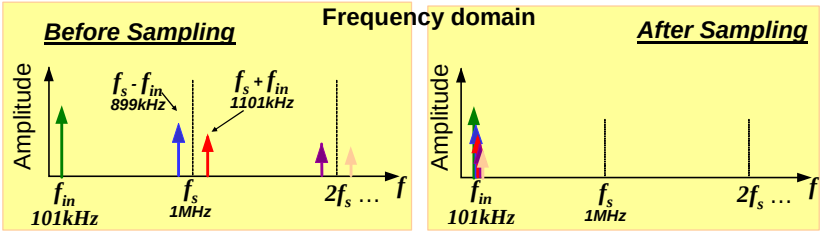
Typical Sampling Process

Continuous-Time(CT) ⇒ Sampled Data (SD)



Sampling Sine Waves



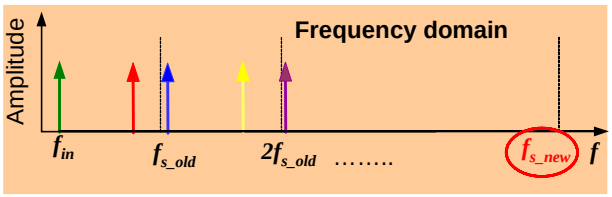


Aliasing

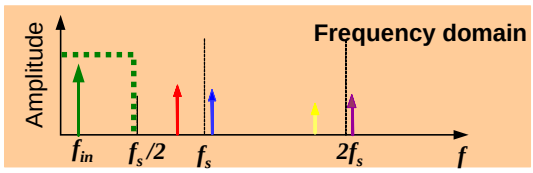
- Multiple continuous time signals can produce identical series of sampled voltages
- The folding back of signals from $nf_S \pm f_{sig}$ down to f_{fin} is called aliasing
  - Sampling theorem: $f_s > 2f_{max\_Signal}$
- If aliasing occurs, no signal processing operation downstream of the sampling process can recover the original continuous time signal
- To Avoid aliasing → two possibilities:
  1. Sample fast enough to cover all spectral components, including "parasitic" ones outside band of interest
  2. Limit f_{max_Signal} through filtering

How to Avoid Aliasing

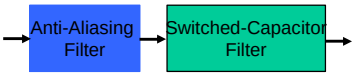
1- Push sampling frequency to x2 of the highest freq.
→ In most cases not practical

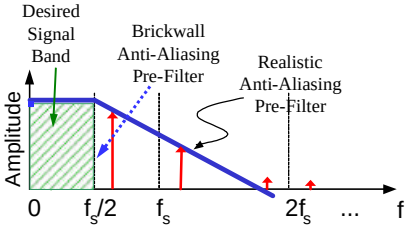


2- Pre-filter signal to eliminate signals above 1/2 sampling frequency- then sample



Anti-Aliasing Filter

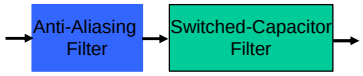


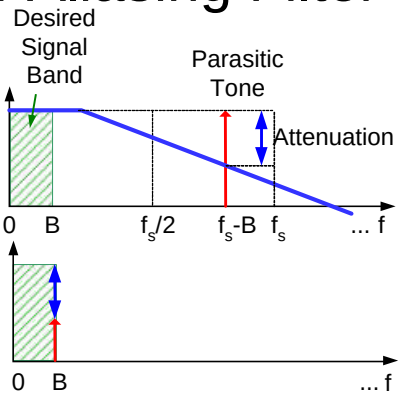


Case1- $B = f_{max-Signal} = f_s/2$

- Non-practical since an extremely high order anti-aliasing filter (close to an ideal brickwall filter) is required
- Practical anti-aliasing filter →Nonzero filter "transition band"
- In order to make this work, we need to sample much faster than 2x the signal bandwidth
  →"Oversampling"

Practical Anti-Aliasing Filter



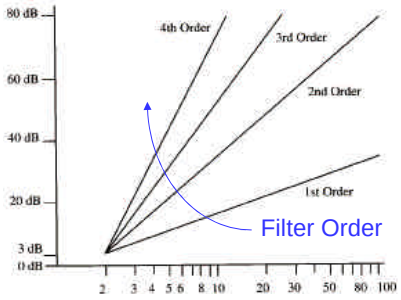


Case2 - $B = f_{max-Signal} << f_s/2$

- More practical anti-aliasing filter
- Preferable to have an anti-aliasing filter with:
  →The lowest order possible
  →No frequency tuning required (if frequency tuning is required then why use SC filter, just use the prefilter!?)

Tradeoff
Oversampling Ratio versus Anti-Aliasing Filter Order

Maximum Aliasing Dynamic Range

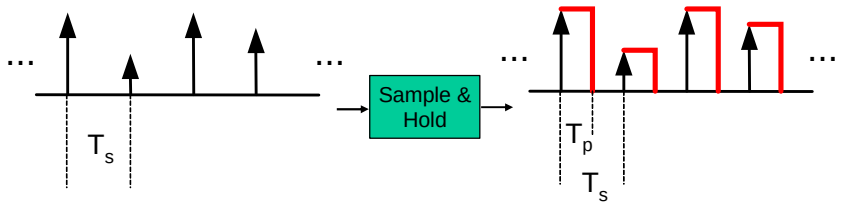


[R. v. d. Plassche, *CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters*, 2nd ed., p.41]

* *Assumption→ anti-aliasing filter is Butterworth type*

- Tradeoff: Sampling speed vs. filter order

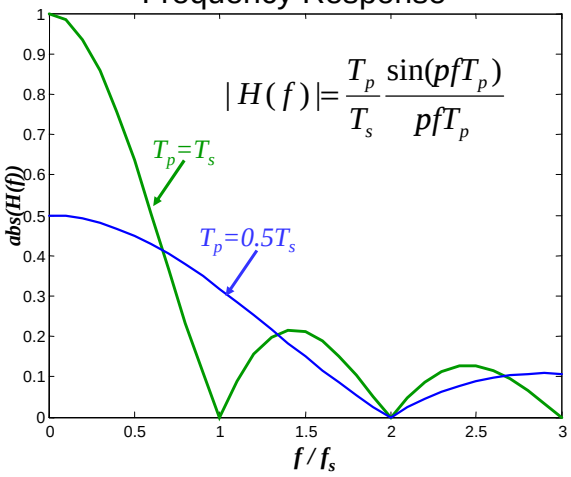
Effect of Sample & Hold



•Using the Fourier transform of a rectangular impulse:

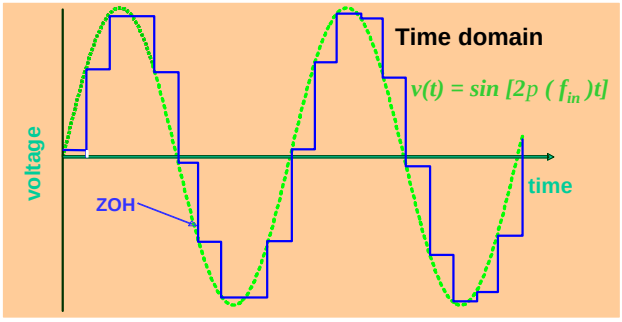
$$|H(f)| = \frac{T_p}{T_s}\frac{\sin(pfT_p)}{pfT_p}$$

Effect of Sample & Hold on Frequency Response

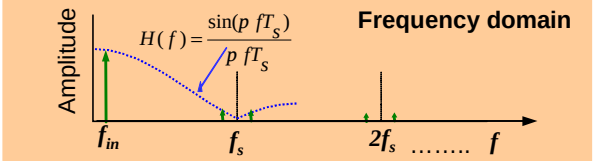


Sample & Hold Effect (Reconstruction of Analog Signals)

$T_p = T_s$



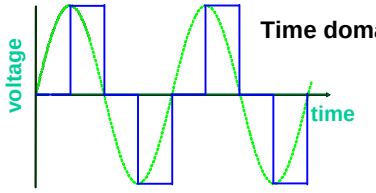
Magnitude droop due to sinx/x effect



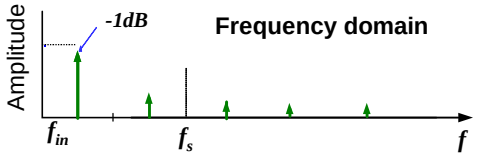
Sample & Hold Effect
(Reconstruction of Analog Signals)

Magnitude droop
due to sinx/x effect:

Case 1) $f_{sig}=f_s/4$



Droop= *-1dB*

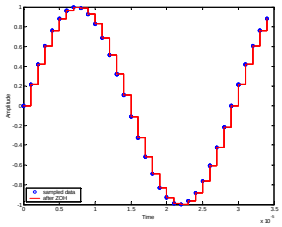


Sample & Hold Effect
(Reconstruction of Analog Signals)

Magnitude droop due
to sinx/x effect:

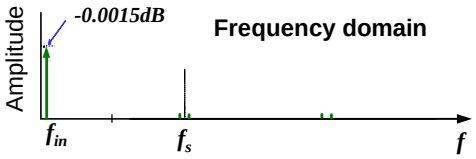
Case 2)
$f_{sig}=f_s/100$

Time domain

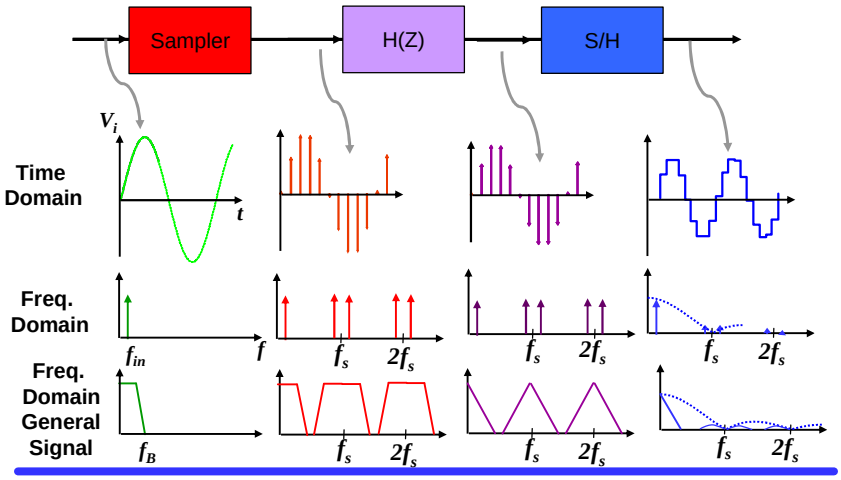


Droop= *-0.0015dB*

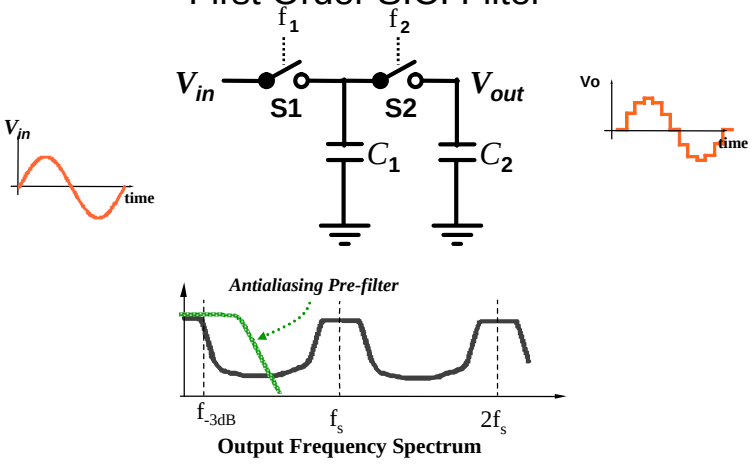
→ High oversampling ratio desirable



Sampling Process Including S/H



First Order S.C. Filter



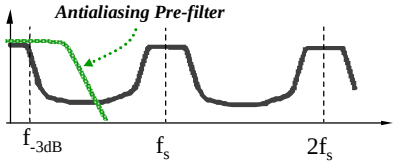
Output Frequency Spectrum

Switched-Capacitor Filters → problem with aliasing

Sampled-Data Filters
Anti-aliasing Requirements

- Frequency response repeats at f_s , $2f_s$, $3f_s$…..
- High frequency signals close to f_s , $2f_s$,….folds back into passband (aliasing)
- Most cases must pre-filter input to a sampled-data filter to remove signal at $f > f_s/2$ (*nyquist* → $f_{max} < f_s/2$)
- Usually, anti-aliasing filter included on-chip as continuous-time filter with relaxed specs. (no tuning)

Example : Anti-Aliasing Filter



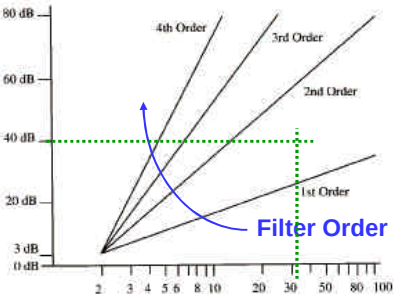
- Voice-band SC filter $f_{-3dB} = 4kHz$ & $f_s = 256kHz$
- Anti-aliasing filter requirements:
  - Need 40dB attenuation at clock freq.
  - Incur no phase-error from 0 to 4kHz
  - Gain error 0 to 4kHz < 0.05dB
  - Allow +-30% variation for anti-aliasing corner frequency (no tuning)

    →Oversampling ratio= 256kHz/2x4kHz=32

    → Need to find minimum filter order

Oversampling Ratio versus Anti-Aliasing Filter Order

Maximum Aliasing Dynamic Range



[R. v. d. Plassche, *CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters*, 2nd ed., p.41]

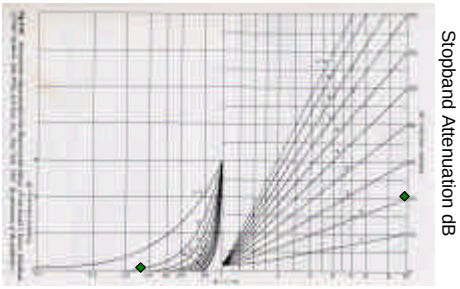
* *Assumption→ anti-aliasing filter is Butterworth type*

→2nd order Butterworth

→Need to find minimum corner frequency for mag. droop < 0.05dB

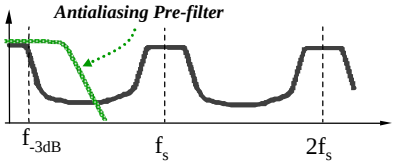
Example : Anti-Aliasing Filter Specifications

- Nomalized frequency for 0.05dB droop → 0.34→ 4kHz/0.34=12kHz
- Set anti-aliasing filter corner frequency for minimum corner frequency 12kHz → Nominal corner frequency 12x1.3=15.6kHz
- Check if attenuation requirement is satisfied for widest filter bandwidth → 15.6x1.3=20.2kHz
- Normalized filter corner freq. to clock freq.=256/20.2=12.6
- Check phase-error within 4kHz bandwidth



From: Williams and Taylor, p. 2-37

Example : Anti-Aliasing Filter



- Voice-band SC filter $f_{-3dB}=4kHz$ & $f_s=256kHz$
- Anti-aliasing filter requirements:
  - Need 40dB attenuation at clock freq.
  - Incur no phase-error from 0 to 4kHz
  - Gain error 0 to 4kHz < 0.05dB
  - Allow +-30% variation for anti-aliasing corner frequency (no tuning)

    →2-pole Butterworth LPF with nominal corner freq. of 15.6kHz & no tuning

Ease of anti-aliasing → high ratio for $f_{sampling}$ / f_{-3dB}

Switched-Capacitor Noise

- The mean-squared noise current due to S1 and S2's kT/C noise is :

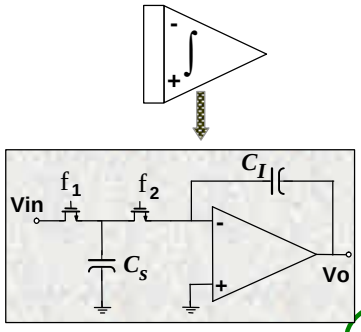
$$\overline{i^2} = (Qf_s)^2 = 2k_BTCf_s^2$$

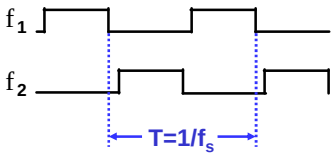
- This noise is approximately white and distributed between 0 and $f_s/2$ (noise spectra → single sided by convention)
  The spectral density of the noise is:

$$\frac{\overline{i^2}}{\Delta f} = \frac{2k_BTCf_s^2}{f_s/2} = 4k_BTCf_s = \frac{4k_BT}{R_{EQ}} \qquad using \qquad R_{EQ} = \frac{1}{f_sC}$$

→ **S.C. resistor noise equals a physical resistor noise with same value!**

Switched-Capacitor Integrator





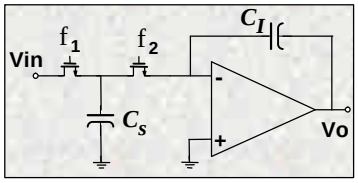
for $f_{signal} \ll f_{sampling}$ $V_0 = \frac{f_s \times C_S}{C_I} \int V_{in}\, dt$

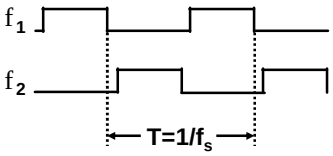
$w_0 = f_s \times \frac{C_S}{C_I}$

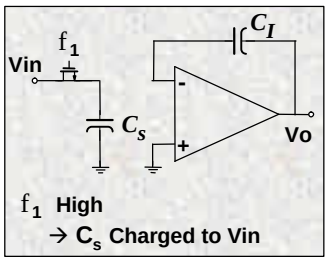
Main advantage: No tuning needed

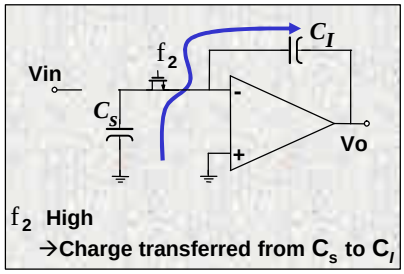
→ critical frequency function of ratio of caps & clock freq.

SC Integrator









Continuous-Time versus Discrete Time Design Flow

Continuous-Time

- Write differential equation
- Laplace transform (F(s))
- Let s=jω → F(jω)
- Plot |F(jω)|, phase(F(jω)

Discrete-Time

- Write difference equation, → relates output sequence to input sequence

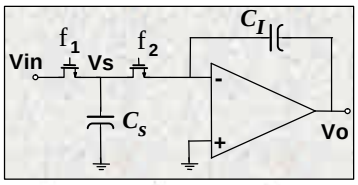
$$V_o(nT_s) = V_i\ [(n-1)T_s] - \ldots\ldots\ldots$$

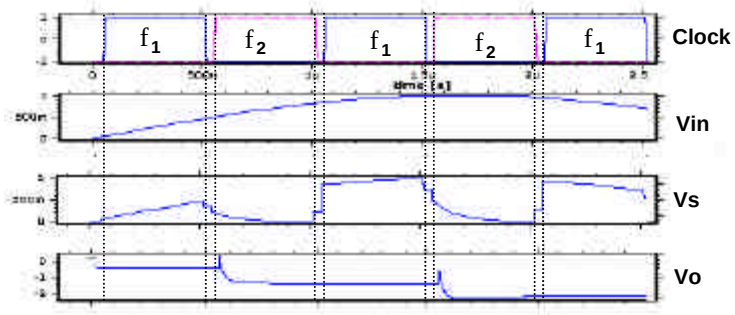
- Use delay operator Z^{-1} to transform the recursive realization to algebraic equation in Z domain

$$V_o(Z) = Z^{-1} V_i(Z) \ldots\ldots$$

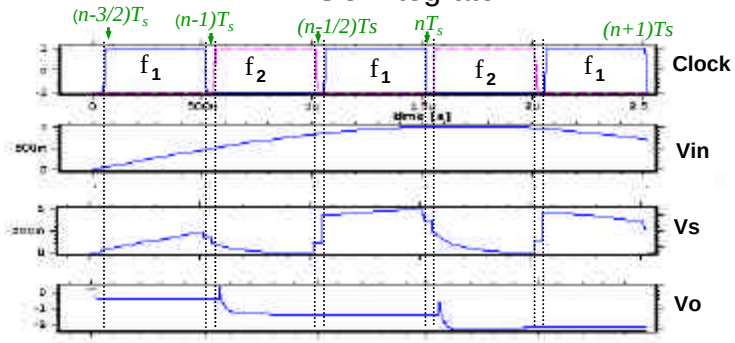
- Set $Z = e^{jwT}$
- Plot mag./phase versus frequency

SC Integrator





SC Integrator



$\Phi_1 \rightarrow \quad Q_s[(n-1)T_s] = C_s V_i[(n-1)T_s]\ , \quad Q_I[(n-1)T_s] = Q_I[(n-3/2)T_s]$

$\Phi_2 \rightarrow \quad Q_s[(n-1/2)\,T_s] = 0\ , \quad Q_I[(n-1/2)\,T_s] = Q_I[(n-3/2)\,T_s] + Q_s[(n-1)\,T_s]$

$\Phi_{1\_} \rightarrow \quad Q_s[nT_s] = C_s V_i[nT_s]\ , \quad \boxed{Q_I[nT_s] = Q_I[(n-1)\,T_s] + Q_s[(n-1)\,T_s]}$

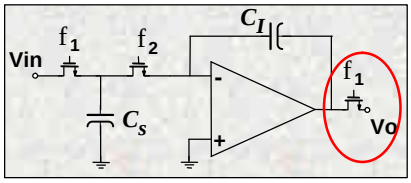
Since $V_o = -Q_I/C_I$ & $V_i = Q_s/C_s \rightarrow C_I V_o(nT_s) = C_I V_o[(n-1)\,T_s] - C_s V_i[(n-1)\,T_s]$

Discrete Time Design Flow

- Transforming the recursive realization to algebraic equation in Z domain:
  - Use Delay operator Z :

$$nT_S \ldots\ldots\ldots\ldots\ldots\ldots \rightarrow 1$$
$$[(n-1)T_S] \ldots\ldots\ldots\ldots \rightarrow Z^{-1}$$
$$[(n-1/2)T_S] \ldots\ldots\ldots \rightarrow Z^{-1/2}$$
$$[(n+1)T_S] \ldots\ldots\ldots\ldots \rightarrow Z^{+1}$$
$$[(n+1/2)T_S] \ldots\ldots\ldots \rightarrow Z^{+1/2}$$

SC Integrator



$$-C_I V_O(nT_S) = -C_I V_O[(n-1)T_S] + C_S V_{in}[(n-1)T_S]$$

$$V_O(nT_S) = V_O[(n-1)T_S] - \frac{C_S}{C_I} V_{in}[(n-1)T_S]$$

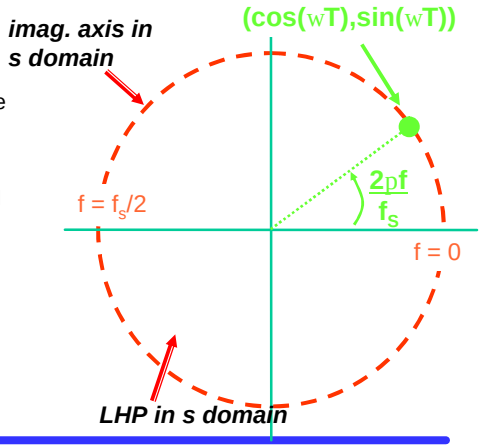
$$V_O(Z) = Z^{-1} V_O(Z) - Z^{-1} \frac{C_S}{C_I} V_{in}(Z)$$

$$\frac{V_O}{V_{in}}(Z) = -\frac{C_S}{C_I} \times \boxed{\frac{Z^{-1}}{1-Z^{-1}}}$$

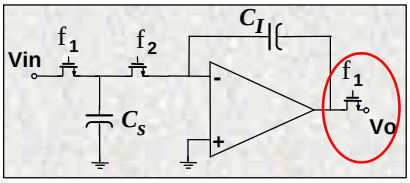
DDI (Direct-Transform Discrete Integrator)

z-Domain Frequency Response

- LHP singularities in s-plane map into inside of unit-circle in Z domain
- RHP singularities in s-plane map into outside of unit-circle in Z domain
- The jω axis maps onto the unit circle
- Particular values:
  - f = 0 → z = 1
  - f = f_s/2 → z = -1
- The frequency response is obtained by evaluating H(z) on the unit circle at
  $z = e^{j\omega T} = \cos(\omega T) + j\sin(\omega T)$
- Once z=-1 (f_s/2) is reached, the frequency response repeats, as expected
- The angle to the pole is equal to 360° (or 2π radians) times the ratio of the pole frequency to the sampling frequency



Switched-Capacitor Direct-Transform Discrete Integrator



$$\frac{V_o}{V_{in}}(Z) = -\frac{C_s}{C_I} \times \frac{Z^{-1}}{1-Z^{-1}}$$

$$= -\frac{C_s}{C_I} \times \frac{1}{Z-1}$$

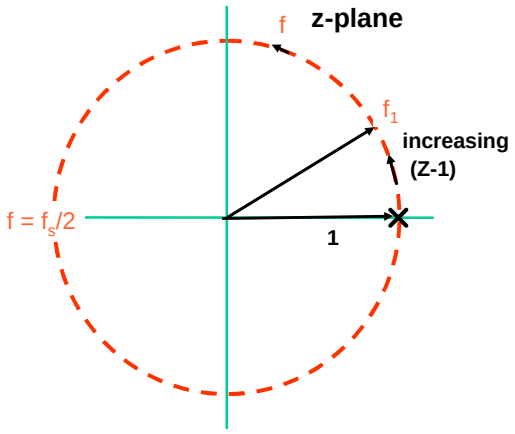
DDI Integrator Pole-Zero Map in z-Plane

Z-1=0 → Z=1 on unit circle

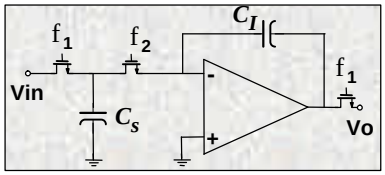
Pole from f→0 in s-plane mapped to z=+1

As frequency increases z domain pole moves on unit circle (CCW)

Onces pole gets to (Z=-1),(f=f_s /2), frequency response repeats



DDI SC Integrator



$$\frac{V_o}{V_{in}}(Z) = -\frac{C_s}{C_I} \times \frac{Z^{-1}}{1-Z^{-1}}$$

$$\frac{V_o}{V_{in}}(Z) = -\frac{C_s}{C_I} \times \frac{1}{Z-1}, \quad Z = e^{jwT}$$

$$= -\frac{C_s}{C_I} \times \frac{1}{e^{jwT}-1} =$$

$Series expansion\ for\ e^x$

$$e^x = 1 + x + \frac{x^2}{2!} + \frac{x^3}{3!} + \frac{x^4}{4!} \ldots\ldots$$

$$\frac{V_o}{V_{in}}(w) = -\frac{C_s}{C_I} \times \frac{1}{\left[1 + jwT + \frac{(jwT)^2}{2!} + \frac{(jwT)^3}{3!} + \ldots.\right]} - 1$$

$$= -\frac{C_s}{C_I} \times \frac{1}{jwT - \frac{(wT)^2}{2!} + \frac{(wT)^3}{3!} + \ldots.}$$

$for\ wT << 1$

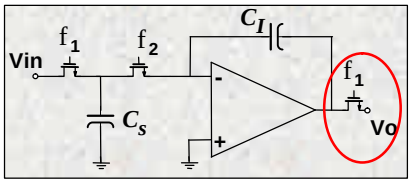
$$\frac{V_o}{V_{in}}(w) = -\frac{C_s}{C_I} \times \frac{1}{jwT}$$

$Since T = 1/f_s$

$$\frac{V_o}{V_{in}}(w) = -\frac{C_s}{C_I} \times \frac{f_s}{s} = -\frac{1}{C_I R_{eq} s}$$

$\rightarrow ideal\ integrator$

DDI SC Integrator



$$\frac{V_o}{V_{in}}(Z) = -\frac{C_s}{C_I} \times \frac{Z^{-1}}{1-Z^{-1}} \quad , \quad Z = e^{jwT}$$

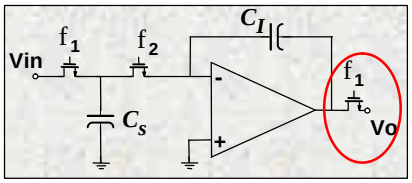
$$= \frac{C_s}{C_I} \times \frac{1}{1-e^{jwT}} = \frac{C_s}{C_I} \times \frac{e^{-jwT/2}}{e^{-jwT/2} - e^{jwT/2}}$$

$$= -j\frac{C_s}{C_I} \times e^{-jwT/2} \times \frac{1}{2\sin(wT/2)}$$

$$= -\frac{C_s}{C_I}\frac{1}{jwT} \times \frac{wT/2}{\sin(wT/2)} \times e^{-jwT/2}$$

Ideal Integrator) Magnitude Error Phase Error

DDI SC Integrator



$$\frac{V_O}{V_{in}}(Z) = -\frac{C_s}{C_I}\frac{1}{jwT} \times \frac{wT/2}{sin(wT/2)} \times e^{-jwT/2}$$

Ideal Integrator) Magnitude Error Phase Error

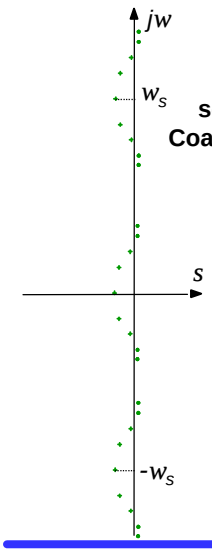
Example: Mag. & phase error for:

1- f / fs=1/12 → Mag. Error = 1% or 0.1dB
Phase error=15 degree
Q_{intg} = -3.8

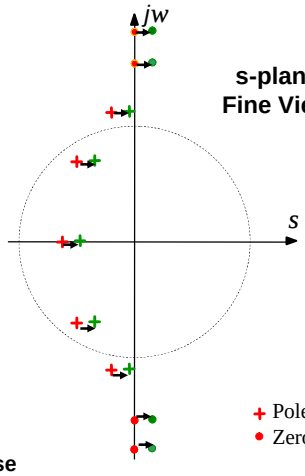
2- f / fs=1/32 → Mag. Error=0.16% or 0.014dB
Phase error=5.6 degree
Q_{intg} = -10.2

DDI Integrator
→ magnitude error no problem
phase error major problem

Switched Capacitor Filter Build with DDI Integrator



s-plane Coarse View

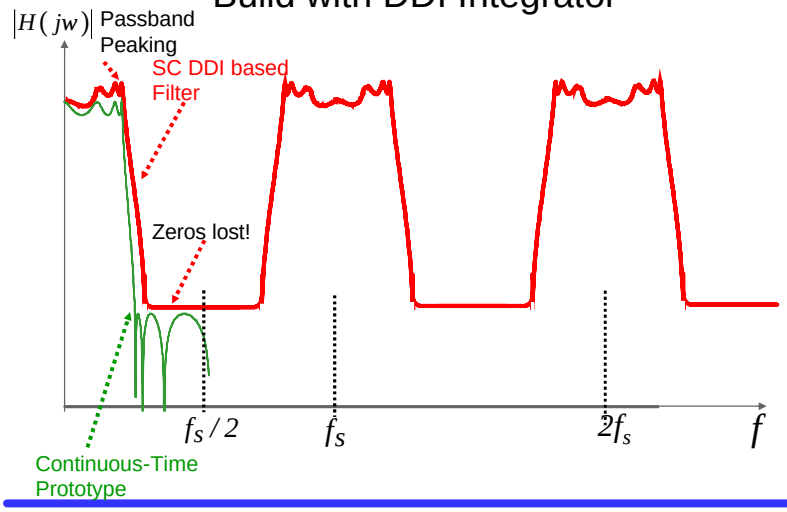


s-plane Fine View

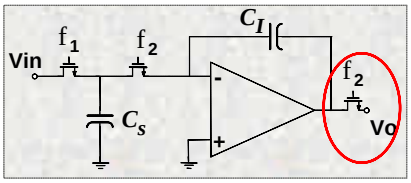
Example: 5th Order Elliptic Filter Singularities pushed towards RHP due to integrator excess phase

+ Pole
• Zero

Switched Capacitor Filter Build with DDI Integrator



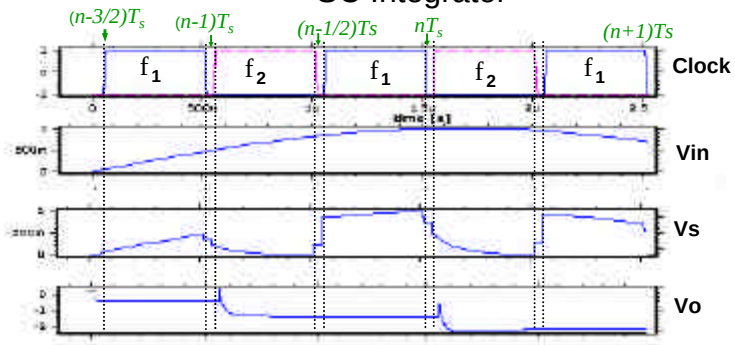
SC Integrator



Sample output ½ clock cycle earlier

→ Sample output on f_2

SC Integrator



$\Phi_1 \rightarrow \quad Q_s[(n-1)T_s] = C_s V_i[(n-1)T_s]\,, \quad Q_I[(n-1)T_s] = Q_I[(n-3/2)T_s]$

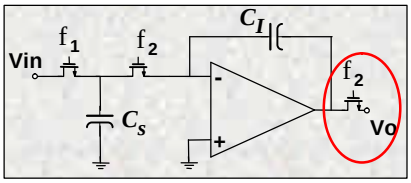
$\Phi_2 \rightarrow \quad Q_s[(n-1/2)\,T_s] = 0\,, \quad Q_I[(n-1/2)\,T_s] = Q_I[(n-3/2)\,T_s] + Q_s[(n-1)\,T_s]$

$\Phi_1 \rightarrow \quad Q_s[nT_s] = C_s V_i[nT_s]\,, \quad Q_I[nT_s] = Q_I[(n-1)\,T_s] + Q_s[(n-1)\,T_s]$

$\Phi_2 \rightarrow \quad Q_s[(n+1/2)\,T_s] = 0\,, \quad Q_I[(n+1/2)\,T_s] = Q_I[(n-1/2)\,T_s] + Q_s[n\,T_s]$

LDI SC Integrator

LDI (Lossless Discrete Integrator) → same as DDI but output is sampled ½ clock cycle earlier



LDI

$$\frac{V_O}{V_{in}}(Z) = -\frac{C_s}{C_I} \times \frac{Z^{-1/2}}{1-Z^{-1}}\,, \quad Z = e^{jwT}$$

$$= -\frac{C_s}{C_I} \times \frac{e^{-jwT/2}}{1-e^{-jwT}} = \frac{C_s}{C_I} \times \frac{1}{e^{-jwT/2}-e^{+jwT/2}}$$

$$= -j\frac{C_s}{C_I} \times \frac{1}{2\sin(wT/2)}$$

$$= -\frac{C_s}{C_I}\frac{1}{jwT} \times \frac{wT/2}{\sin(wT/2)}$$

Ideal Integrator) Magnitude Error

No Phase Error!
For signals at frequency <<sampling freq.
→ Magnitude error negligible

Frequency Warping

- Frequency response
  - Continuous time (s-plane): imaginary axis
  - Sampled time (z-plane): unit circle
- Continuous to sampled time transformation
  - Should map imaginary axis onto unit circle
  - How do SC integrators map frequencies?

$$H_{SC}(z) = \frac{C_s}{C_{int}} \frac{z^{-½}}{1 - z^{-1}}$$
$$= -\frac{C_s}{C_{int}} \frac{1}{2j \sin pfT}$$

CT – SC Integrator Comparison

CT Integrator

$$H_{RC}(s) = -\frac{1}{st}$$
$$= -\frac{1}{2pjf_{RC}t}$$

SC Integrator

$$H_{SC}(z) = \frac{C_s}{C_{int}} \frac{z^{-½}}{1 - z^{-1}}$$
$$= -\frac{C_s}{C_{int}} \frac{1}{2j \sin pf_{SC}T}$$

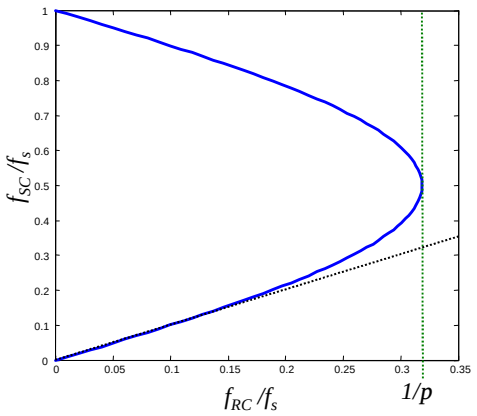
Identical time constants:

$$t = RC = \frac{C_{int}}{f_s C_s}$$

Compare: $H_{RC}(f_{RC}) = H_{SC}(f_{SC})$ →

$$f_{RC} = \frac{f_s}{p} \sin\left(p \frac{f_{SC}}{f_s}\right)$$

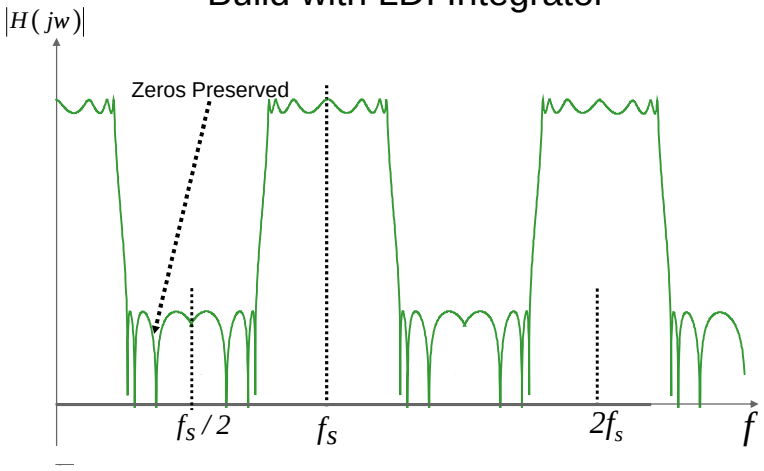
LDI Integration



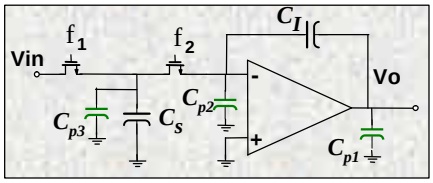
$$f_{RC} = \frac{f_s}{p}\sin\left(p\,\frac{f_{SC}}{f_s}\right)$$

- "RC" frequencies up to f_s/π map to physical (real) "SC" frequencies
- Frequencies above f_s/π do not map to physical frequencies
- Mapping is symmetric about $f_s/2$ (aliasing)
- "Accurate" only for $f_{RC} << f_s$

Switched Capacitor Filter Build with LDI Integrator



SC Integrator
Parasitic Sensitivity



Effect of parasitic capacitors:

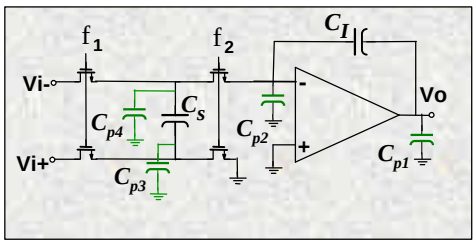
1- C_{p1} - driven by opamp o.k.

2- C_{p2} - at opamp virtual gnd o.k.

3- C_{p3} – Charges to Vin & discharges into C_I

→ Problem parasitic sensitive

SC Integrator
Parasitic Sensitivity



Effect of parasitic capacitors:

1- C_{p1} - driven by opamp o.k.

2- C_{p2} - at opamp virtual gnd o.k.

3- C_{p3} - driven by Vi+ or gnd o.k.

4- C_{p4} – Charges to Vi- &

discharges into C_I

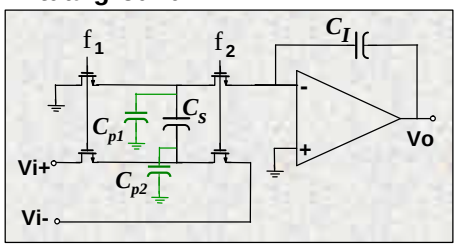
→ Problem parasitic sensitive

Parasitic Insensitive Bottom-Plate SC Integrator

Sensitive parasitic cap. → C_{p1} → rearrange circuit so that C_{p1} does not charge/discharge

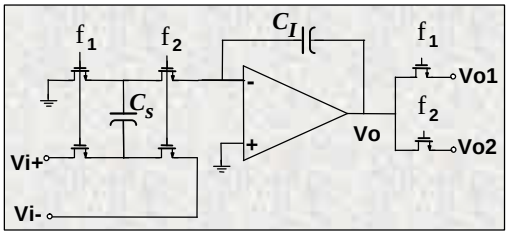
f1=1 → capacitor grounded

f2=1 → capacitor at virtual ground



Solution: Bottom plate capacitor integrator

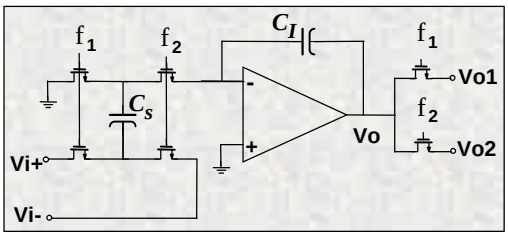
Bottom Plate S.C. Integrator

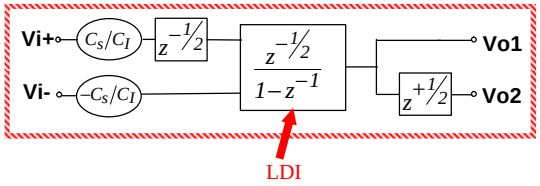


Input/Output z-transform
Note: Delay from Vi+ and Vi- to output is different
→ Special attention needed to input/output connections

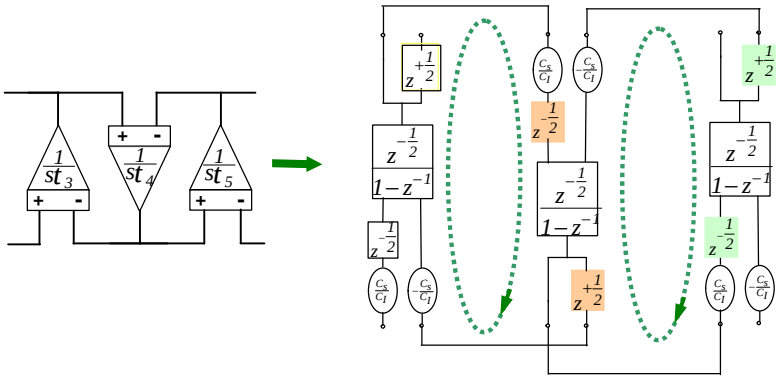
	Vo1 on f1	Vo2 on f2
Vi+ on f1	$\frac{z^{-1}}{1-z^{-1}}$	$\frac{z^{-1/2}}{1-z^{-1}}$
Vi- on f2	$\frac{z^{-1/2}}{1-z^{-1}}$	$\frac{-1}{1-z^{-1}}$

Bottom Plate S.C. Integrator z-Transform Model





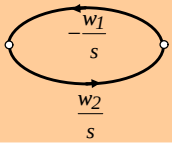
LDI Switched Capacitor Ladder Filter

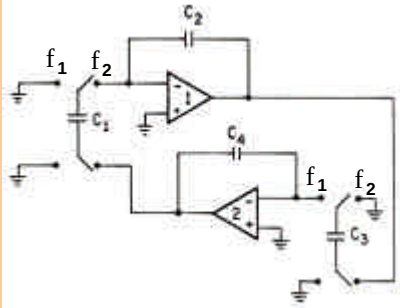


Delay around integ. Loop is ($Z^{-1/2}$ x $Z^{+1/2}$ =1) ➔ LDI function

Switched Capacitor LDI Resonator

Resonator Signal Flowgraph

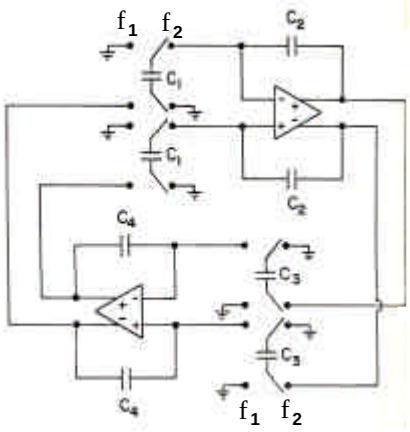




$$w_1 = \frac{1}{R_{eq1}C_2} = f_s \times \frac{C_1}{C_2}$$

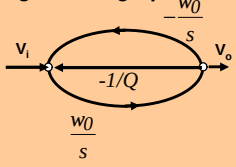
$$w_2 = \frac{1}{R_{eq3}C_4} = f_s \times \frac{C_3}{C_4}$$

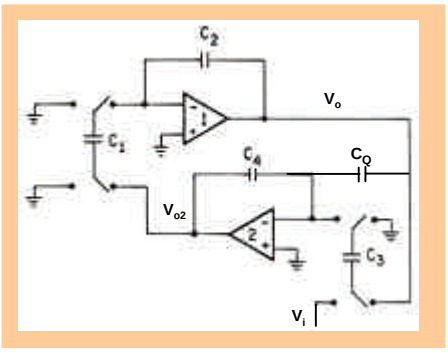
Fully Differential Switched Capacitor Resonator



Switched Capacitor LDI Bandpass Filter Continuous-Time Termination

Bandpass Filter Signal Flowgraph





$$w_0 = s \times \frac{C_3}{C_4} = f_s \times \frac{C_1}{C_2}$$

$$Q = \frac{C_4}{C_Q}$$

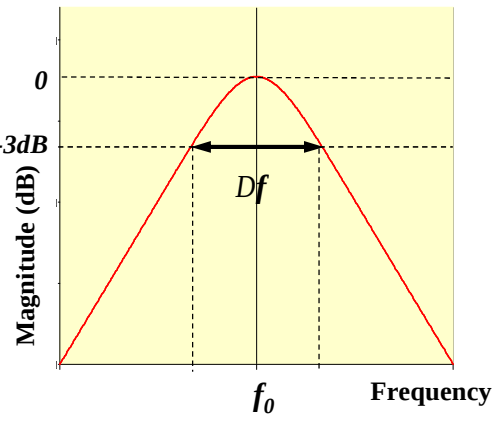
Switched Capacitor LDI Bandpass Filter Continuous-Time Termination

$$f_0 = \frac{1}{2p} f_s \times \frac{C_1}{C_2}$$

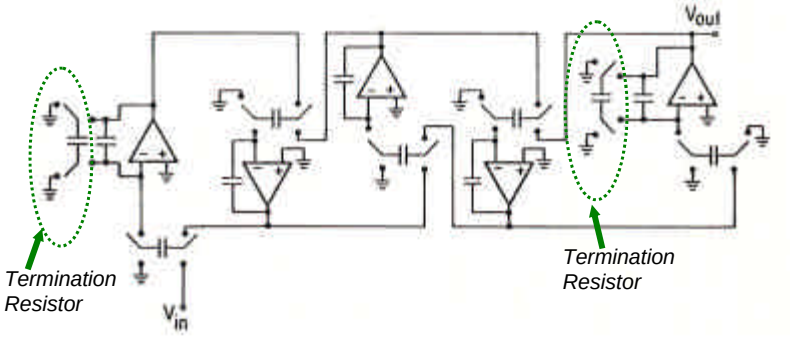
$$\Delta f = \frac{f_0}{Q}$$

$$= \frac{1}{2p} f_s \times \frac{C_1 C_Q}{C_2 C_4}$$

Both accurately determined by cap ratios & clock frequency



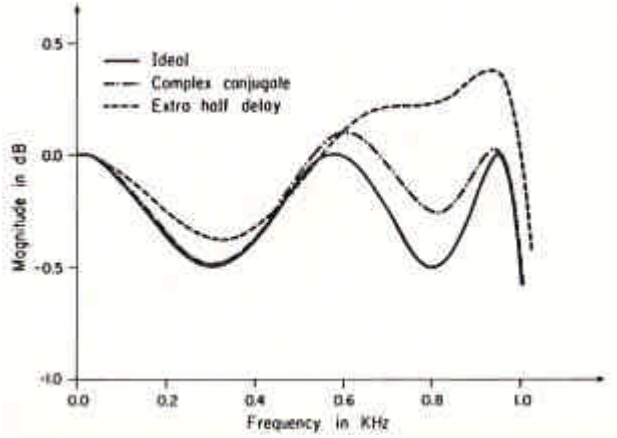
Fifth Order All-Pole LDI Low-Pass Ladder Filter
Complex Conjugate Terminations



•Complex conjugate terminations (alternate phase switching)

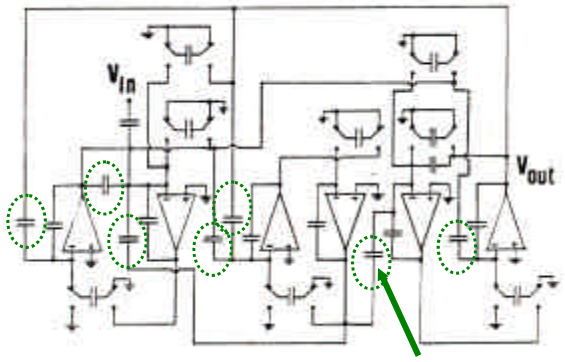
Ref: Tat C. Choi, "High-Frequency CMOS Switched-Capacitor Filters," U. C. Berkeley, Department of Electrical Engineering, Ph.D. Thesis, May 1983 (ERL Memorandum No. UCB/ERL M83/31).

Fifth Order All-Pole Low-Pass Ladder Filter
Termination Implementation



Ref: Tat C. Choi, "High-Frequency CMOS Switched-Capacitor Filters," U. C. Berkeley, Department of Electrical Engineering, Ph.D. Thesis, May 1983 (ERL Memorandum No. UCB/ERL M83/31).

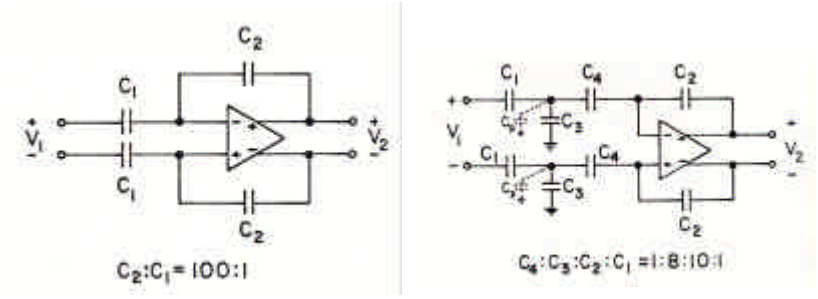
Sixth Order Elliptic LDI Bandpass Filter



Transmission Zero

Ref: Tat C. Choi, "High-Frequency CMOS Switched-Capacitor Filters," U. C. Berkeley, Department of Electrical Engineering, Ph.D. Thesis, May 1983 (ERL Memorandum No. UCB/ERL M83/31).

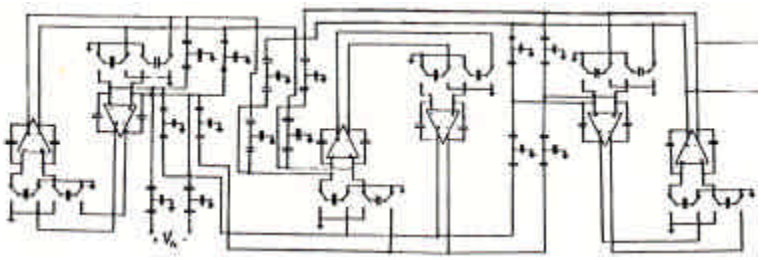
Use of T-Network



High Q filter → large cap. ratio for Q & transmission zero implementation
To reduce large ratios required → T-networks utilized

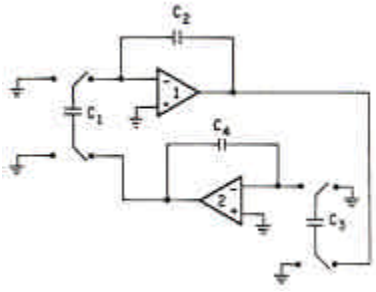
Ref: Tat C. Choi, "High-Frequency CMOS Switched-Capacitor Filters," U. C. Berkeley, Department of Electrical Engineering, Ph.D. Thesis, May 1983 (ERL Memorandum No. UCB/ERL M83/31).

Sixth Order Elliptic Bandpass Filter Utilizing T-Network



Ref: Tat C. Choi, "High-Frequency CMOS Switched-Capacitor Filters," U. C. Berkeley, Department of Electrical Engineering, Ph.D. Thesis, May 1983 (ERL Memorandum No. UCB/ERL M83/31).

S.C. Resonator

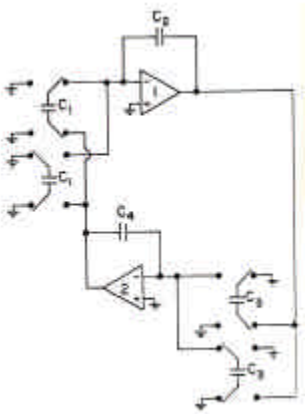


Regular sampling
Each opamp busy settling only during one of the clock phases
→ Idle during the other clock phase

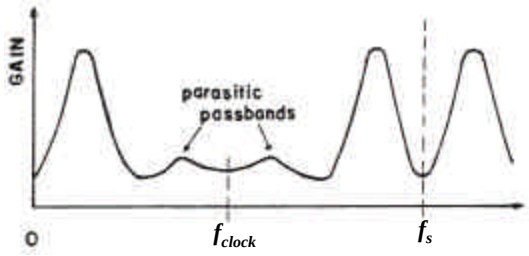
S.C. Resonator Using Double-Sampling

Double-sampling:

- **2nd set of switches & sampling caps added to all integrators**
- **While one set of switches/caps sampling the other one transfers charge into the intg. cap**
- **Opamps busy during both clock phases**
- **Effective sampling freq. twice clock freq. while opamp bandwidth stays the same**



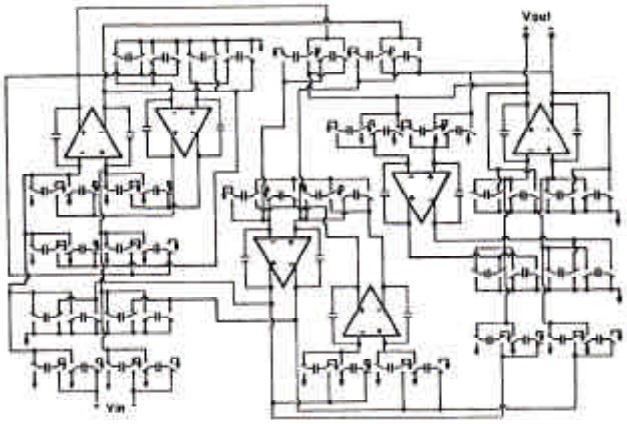
Double-Sampling Issues



Issues to be aware of:
- Jitter in the clock
- Unequal clock phases
-Mismatch in sampling caps.
→ parasitic passbands

Ref: Tat C. Choi, "High-Frequency CMOS Switched-Capacitor Filters," U. C. Berkeley, Department of Electrical Engineering, Ph.D. Thesis, May 1983 (ERL Memorandum No. UCB/ERL M83/31).

Double-Sampled Fully Differential S.C. 6th Order All-Pole Bandpass Filter



Ref: Tat C. Choi, "High-Frequency CMOS Switched-Capacitor Filters," U. C. Berkeley, Department of Electrical Engineering, Ph.D. Thesis, May 1983 (ERL Memorandum No. UCB/ERL M83/31).