Trends of IC Microfabrication

Source: SEMI, SIA, IC Insights; Rev. January 14, 2002
The beauty of silicon

For four decades, the semiconductor industry has steadily reduced the unit cost of IC components by

1. Scaling device dimensions downward

2. Scaling wafer diameter upward

<table>
<thead>
<tr>
<th></th>
<th>1990</th>
<th>1995</th>
<th>2000</th>
</tr>
</thead>
<tbody>
<tr>
<td>DRAMs</td>
<td>4 MB</td>
<td>64 MB</td>
<td>1 GB</td>
</tr>
<tr>
<td>Feature size</td>
<td>0.8 μm</td>
<td>0.35 μm</td>
<td>0.15 μm</td>
</tr>
<tr>
<td>Wafer diameter</td>
<td>6”</td>
<td>8”</td>
<td>12”</td>
</tr>
<tr>
<td>Cost per Megabit</td>
<td>$6.50</td>
<td>$3.14</td>
<td>$0.10</td>
</tr>
</tbody>
</table>
Moore's law: "The complexity for minimum component cost has increased at a rate of roughly a factor of two per year" [5], later amended to doubling every 18 to 24 months.

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## SIA roadmap

### Memory and Logic Technology Requirements

<table>
<thead>
<tr>
<th>Year of First Product Shipment Technology Generation</th>
<th>1999 180 nm</th>
<th>2001 150 nm</th>
<th>2003 130 nm</th>
<th>2006 100 nm</th>
<th>2009 70 nm</th>
<th>2012 50 nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Min. Logic $V_{dd}$ (V)</td>
<td>1.8-1.5</td>
<td>1.5-1.2</td>
<td>1.5-1.2</td>
<td>1.2-0.9</td>
<td>0.9-0.6</td>
<td>0.6-0.5</td>
</tr>
<tr>
<td>$T_{ox}$ Equivalent (nm)</td>
<td>3-4</td>
<td>2-3</td>
<td>2-3</td>
<td>1.5-2</td>
<td>&lt;1.5</td>
<td>&lt;1.0</td>
</tr>
<tr>
<td>Equivalent Maximum E-field (MV/cm)</td>
<td>5</td>
<td>5</td>
<td>5</td>
<td>&gt;5</td>
<td>&gt;5</td>
<td>&gt;5</td>
</tr>
<tr>
<td>Nominal $I_{on}$ @ 25°C (mA/mm) (NMOS/PMOS)</td>
<td>600/2 80</td>
<td>600/2 80</td>
<td>600/2 80</td>
<td>600/2 80</td>
<td>600/2 80</td>
<td>600/2 80</td>
</tr>
<tr>
<td>S/D Extension Junction Depth, Nominal (nm)</td>
<td>36-72</td>
<td>30-60</td>
<td>26-52</td>
<td>20-40</td>
<td>15-30</td>
<td>10-20</td>
</tr>
</tbody>
</table>
Another Perspective on Moore’s Law

… we are already producing $10^{18}$ transistors per year. Enough to supply every ant on the planet with ten transistors.

Twenty years from now, if the trend continues, there will be more transistors than there will be cells in the total number of human bodies on Earth.
Channel Engineering

SUBMICRON DEVICE STRUCTURE AND DESIGN

Spacer Formation Technology → Polysilicon Gate Stack Design → Low Series Resistance Contact Technology

Silicide → Deep S/D and LDD Tab Design ← Drain Profile Design

LDD Profile Design ← Channel Profile Design

Vertical (Channel) Engineering → Horizontal (Drain) Engineering
Gate Stack Technology

Equivalent Oxide Thickness

$Q_s \rightarrow$ high k-dielectric gives lower electrical thickness.

$C_{ox} \propto \frac{\varepsilon}{X_{ox}}$

Materials:
- Ta205
- BZT
- Al2O3
Nanotechnology for Gate Dielectrics

Source: Intel

90nm process

Capacitance: 1X
Leakage: 1X

Experimental high-k

1.6X
< 0.01X
High-K dielectric by Atomic Layer Deposition

Self-limiting surface reactions of suitable precursor compounds A and B, which form the desired product S in a binary reaction cycle consisting of two sequential half-reactions.

For an extensive list of precursors, see Ritala and Leskela, Handbook of Thin Film Materials, Vol.1, Chap 2 (2002)
Fig. 6-41 Elevated source/draains. (a) Key process steps in forming elevated source/draains using SEG. (b) Comparison of the doping profile in source/drain regions of a PMOS device after a BF<sub>2</sub><sup>+</sup> implant directly into the regions (and a conventional furnace anneal) versus a BF<sub>2</sub><sup>+</sup> implant into the SEG regions and an RTP anneal.79
The ingredients of scaling

Material Evolution in MOS

New materials

Improved processing

New geometries

Scaling Will continue as long as

$\frac{\delta \text{ cost}}{\delta \text{ performance}} < \text{ alternate technologies}$
Cu interconnect

High k gate dielectric

Contacts to nanodevices

Low-k ILD

Metal gate

Wafer bonding & layer transfer

Interconnects for nanodevices

Bulk CMOS

High mobility (strained Si on SiGe)

3D, heterogeneous integration

Molecular devices

Nanotube

Feature Size:

| 100 nm | 15 nm | 2 nm |

Time

International Technology Roadmap for Semiconductors
Thin-Body MOSFET

- $T_{ox} = 2$ nm
- $L_{gate} = 25$ nm
- $V_{dd} = 1$ V

- Thin body to control short-channel effects
- Elevated S/D to reduce $R_{sd}$

![Diagram of Thin-Body MOSFET](image)

**Ids vs. Vgs**

- $T_{si} = 25$ A
- $T_{si} = 50$ A
- $T_{si} = 75$ A
- $t_{si} = 100$ A

Graph showing logarithmic current density ($\log I_d$) vs. gate voltage ($V_{gs}$).
Dual Gate MOSFET

- **raised source/drain**
- **improves s/d resistance**
- **gate spacers to reduce capacitance**

![Diagram of a Dual Gate MOSFET](image)

- **heavily doped s/d**
- **lightly doped channel**
- **buried oxide**
- **top gate**
- **bottom gate**
- **silicon thickness**: 5–10 nm
- **aligned top and bottom gates**

**FIGURE 6.2** Generic features of double gate MOSFET device.
FinFET

* self-aligned double-gate structure *

Lg ~ (10 nm – 45 nm)

Fin width ~ (<10 nm – 120 nm)

Fin height: 50 nm

Tox ~ 2.5 nm

Body doping: 10^{16} n-type

Huang et al, IEDM, 1999
1. Four stress techniques — dual stress liners, stress memorization (SM) and an embedded SiGe S/D — were fully integrated on a partially depleted SOI substrate. (Source: IBM and AMD)
<table>
<thead>
<tr>
<th>ITRS year*</th>
<th>2009</th>
<th>2011</th>
<th>2013</th>
</tr>
</thead>
<tbody>
<tr>
<td>High performance</td>
<td>45 nm</td>
<td>32 nm</td>
<td>22 nm</td>
</tr>
<tr>
<td>FET technology</td>
<td>Planar</td>
<td>Planar</td>
<td>Planar/non-planar</td>
</tr>
<tr>
<td>Channel</td>
<td>Strained silicon/SOI</td>
<td>Strained Si/SOI + UTB or embedded strain/HOT</td>
<td>Strained Si/SOI + UTB with SiGe or Ge for high mobility</td>
</tr>
<tr>
<td>High-k dielectric</td>
<td>SiON/Hf-based high-k</td>
<td>Scaled Hf-based high-k/alternative high-k</td>
<td>Scaled Hf-based high-k/alternative high-k</td>
</tr>
<tr>
<td>Gate electrode</td>
<td>Polysilicon</td>
<td>Metals</td>
<td>Tunable WF metals</td>
</tr>
</tbody>
</table>

*Year of first introduction in manufacturing

Source: R. Jammy, IBM/Sematech
New Era of Manufacturable Stress Films

1. Tensile Silicon Nitride (NMOS)
2. Compressive Silicon Nitride (PMOS)
3. Tensile HARP PMD
4. Tensile HARP STI
5. Selective Epitaxial Silicon Germanium
6. Biaxially Strained SiGe Substrates

FUTURE of Strain Engineering
Candidates to replace the CMOS switch (after 2020)

<table>
<thead>
<tr>
<th>Logic device technologies (potential) operation</th>
<th>Scalability</th>
<th>Performance</th>
<th>Energy efficiency</th>
<th>Gain</th>
<th>Operational reliability</th>
<th>Room temperature operation</th>
<th>CMOS technological compatibility</th>
<th>CMOS architectural compatibility</th>
</tr>
</thead>
<tbody>
<tr>
<td>1-D structures (carbon nanotubes &amp; nanowires)</td>
<td>2.4</td>
<td>2.5</td>
<td>2.3</td>
<td>2.3</td>
<td>2.1</td>
<td>2.8</td>
<td>2.3</td>
<td>2.8</td>
</tr>
<tr>
<td>Resonant tunneling devices</td>
<td>1.5</td>
<td>2.2</td>
<td>2.1</td>
<td>1.7</td>
<td>1.7</td>
<td>2.5</td>
<td>2.0</td>
<td>2.0</td>
</tr>
<tr>
<td>Single electron transistors</td>
<td>1.9</td>
<td>1.5</td>
<td>2.6</td>
<td>1.4</td>
<td>1.2</td>
<td>1.9</td>
<td>2.1</td>
<td>2.1</td>
</tr>
<tr>
<td>Molecular devices</td>
<td>1.6</td>
<td>1.8</td>
<td>2.2</td>
<td>1.5</td>
<td>1.6</td>
<td>2.3</td>
<td>1.7</td>
<td>1.8</td>
</tr>
<tr>
<td>Ferromagnetic devices</td>
<td>1.4</td>
<td>1.3</td>
<td>1.9</td>
<td>1.5</td>
<td>2.0</td>
<td>2.5</td>
<td>1.7</td>
<td>1.7</td>
</tr>
<tr>
<td>Spin transistor</td>
<td>2.2</td>
<td>1.3</td>
<td>2.4</td>
<td>1.2</td>
<td>1.2</td>
<td>2.4</td>
<td>1.5</td>
<td>1.7</td>
</tr>
</tbody>
</table>

For each device, sum horizontally over eight criteria. Maximum sum=24, Minimum sum=8

Source: ITRS
Interesting Facts about Chip Manufacturing

• A typical 2-gram silicon chip requires 1.6 kilograms of fossil fuel, 72 grams of chemicals and 32 kilograms of water to manufacture.

• To make the high-grade silicon needed for the chips requires 160 times the energy used to produce raw silicon. This accounts for about half of the total energy used by the chip. Only a quarter is consumed during its processing life.

• Because a chip's components are so tiny and precisely engineered, far more materials, such as fuels and solvents, are needed for their manufacture than for more traditional goods.

• The mass of these secondary materials outweighs the product by a factor of 600. In contrast, making a typical car requires only about twice its weight in fossil fuels.

Environmental Impact of the Semiconductor Industry

Impact per square inch of Si

<table>
<thead>
<tr>
<th>Output from the Fab</th>
<th>Input to the Fab</th>
</tr>
</thead>
<tbody>
<tr>
<td>Liquid Waste</td>
<td>Water</td>
</tr>
<tr>
<td>75 Gal/in^2</td>
<td>30 gal/in^2</td>
</tr>
<tr>
<td>Hazardous Waste</td>
<td>Electricity</td>
</tr>
<tr>
<td>0.1 Kg/in^2</td>
<td>10 KWhr/in^2</td>
</tr>
<tr>
<td>Toxic Releases</td>
<td>Chemicals</td>
</tr>
<tr>
<td>0.01 Kg/in^2</td>
<td>0.2 kg/in^2</td>
</tr>
</tbody>
</table>
### Silicon Integrated Circuit Periodic Table

**Metal alloys**
- Melting temperature - °C
- Resistivity - μΩ•cm

**Silicides**
- Formation temperature - °C
- Max temperature on silicon - °C
- Resistivity - μΩ•cm
- Barrier to N-type and P-type silicon - eV

**Dopants & Semiconductors**
- Type - P or N
- Mismatch - radius divided by silicon radius
- Diffusivity in silicon @ 1,000°C - cm/s

**Metal Silicides**
- Transition metal
- Size of the element
- Resistivity - μΩ•cm

**Compounds**
- Thermal stability
- Melting temperature

**Oxides**
- Dielectric constant
- Breakdown voltage - V

**Halogen**
- Use - see key

**Inert**
- Dielectric constant
- Breakdown voltage - V

**Use key**
- AN - annealing
- ION - plasma ion generation
- OX - oxidation
- DP - defect passivation
- NT - nitride formation
- DI - diluent

**Materials that the atomic specie will etch**
- Excited dimer and emission wavelength - nm

**Bulk Gas**
- Use - see key
- Liquid temperature - °C
- Volume - ft³, gas / liquid

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