Basic Structure of CMOS Inverter

- Mask patterns
- N-well CMOS structure
- How many masks?
  Process flow?
The MOSIS CMOS Process

MOSIS is a foundry service that provides standard CMOS fabrication

P-well CMOS
Pattern mask opening
For p-well implant

Shallow implantation
of boron

Diffusion drive-in
To form p-well in
oxidizing ambient

Remove masking oxide
Pad oxide growth and CVD $\text{Si}_3\text{N}_4$. Pattern field oxide regions

Blanket implant of Boron for $p$ channel stop inside $p$-well

Protect $p$-well regions with photoresist.
Implant $\text{Ph}$ to form $n$ channel stop outside $p$-well regions

LOCOS Oxidation

Thermal oxidation of gate $\text{SiO}_2$
Pattern poly-Si gates

Protect ALL n-channel transistors with photoresist.

Boron implantation to form source/drain of p-channel transistors and contacts to p-well
Protect ALL p-channel transistors with photoresist.

Arsenic implantation to form source/drain of n-channel transistors and contacts to n-substrate

CVD SiO\textsubscript{2} (Low-temperature oxide)

Pattern and etch contact openings to source/drain, well contact, and substrate contact.
Metal 1 deposition

Pattern and etch
Metal 1 interconnects

CVD SiO₂
Pattern and etch contact openings to Metal 1.

Metal 2 deposition.

Pattern, and etch Metal 2 interconnects.
3D view of a CMOS inverter after contact etch.
Well Engineering

P-tub

N-tub

Twin Tub

Various CMOS structures. (a) p-tub. (b) n-tub. (c) twin tub.
Twin Well CMOS Process Flow

(a) Si$_3$N$_4$, SiO$_2$, n-well I/I

(b) p-well I/I, B, SiO$_2$

(c) B

(d) n$^+$, Photoresist, p-well, n-well, v-epi, n$^+$ substrate

(e) Thermal oxide, P-glass, SiN, Polysilicon, Al, n$^+$, p$^+$, p-well, n-well, v-epi, n$^+$ substrate
Retrograde Well

- formed by high energy (>200keV) implantation
1) Very low thermal budget for well formation
   (no need for diffusion drive-in)

2) Retrograde Well is formed AFTER field oxidation
   ⇒ small lateral diffusion and localized high conc under FOX
Example: Formation of Channel Stop and Retrograde Well in a single step
Multiple Implants for Well Engineering

Advanced “Profiled” Wells for Sub-Micron Devices
(after Reference 136)

A. N-Well Vertical Profile* (under the gate)

- Vth CONTROL
- BURIED CHANNEL DEPTH CONTROL
- S/D JUNCTION CAPACITANCE

- LATCH-UP SUPPRESSION
- SOFT ERROR REDUCTION

HOT CARRIER CONTROL
- PUNCHTHROUGH SUPPRESSION
- CHANNEL STOP

PHOSPHORUS: 600 keV, 3x10^{13} cm^{-2}

PHOSPHORUS: 70 keV, 6x10^{12} cm^{-2}

PHOSPHORUS: 200 keV, 4x10^{12} cm^{-2}

CONCENTRATION (cm^{-3})

DEPT (μm)
Basic Silicon-on-Insulator (SOI) CMOS Process Flow

(a)

(b)

(c)

(d)

(e)
SOI Process Flow (continued)
Self-Aligned Channel V-gate by Optical Lithography (SALVO) Process

Smallest feature printable by lithography

Oxide spacer

poly-Si gate

Normal S/D implant

CVD oxide

SiO₂

TiSi₂

Angled Implant n+ pocket

Thermal gate oxide

* Sub-50nm channels
SALVO Process Flow

See HW#9 Problem

Chang et al, IEDM 2000