Process Integration

Self-aligned Techniques
- LOCOS- self-aligned channel stop
- Self-aligned Source/Drain
- Lightly Doped Drain (LDD)
- Self-aligned silicide (SALICIDE)
- Self-aligned oxide gap

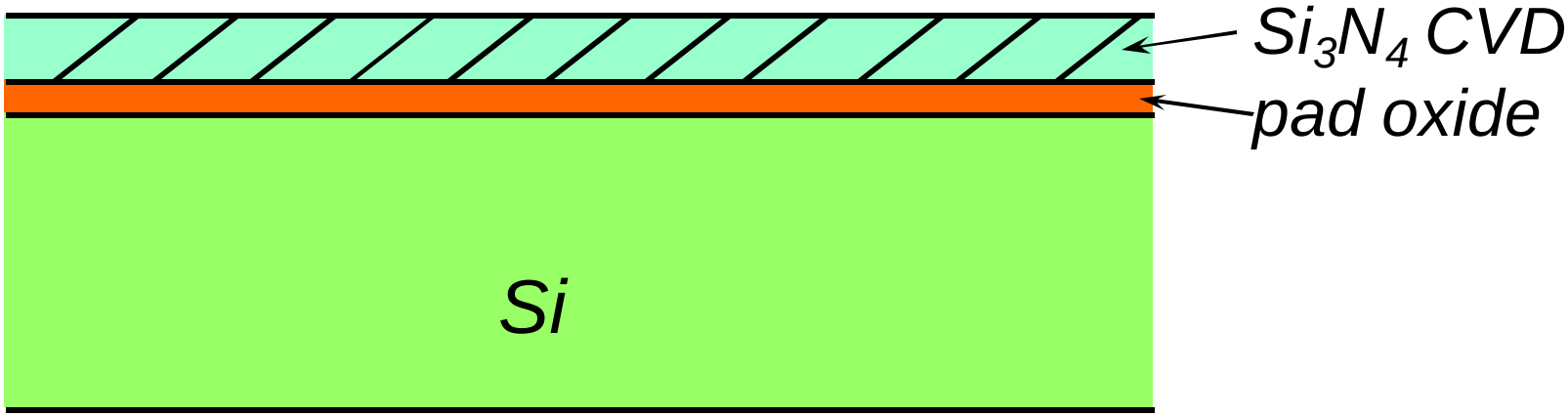
MEMS Release Techniques
- Sacrificial Layer Removal
- Substrate Undercut

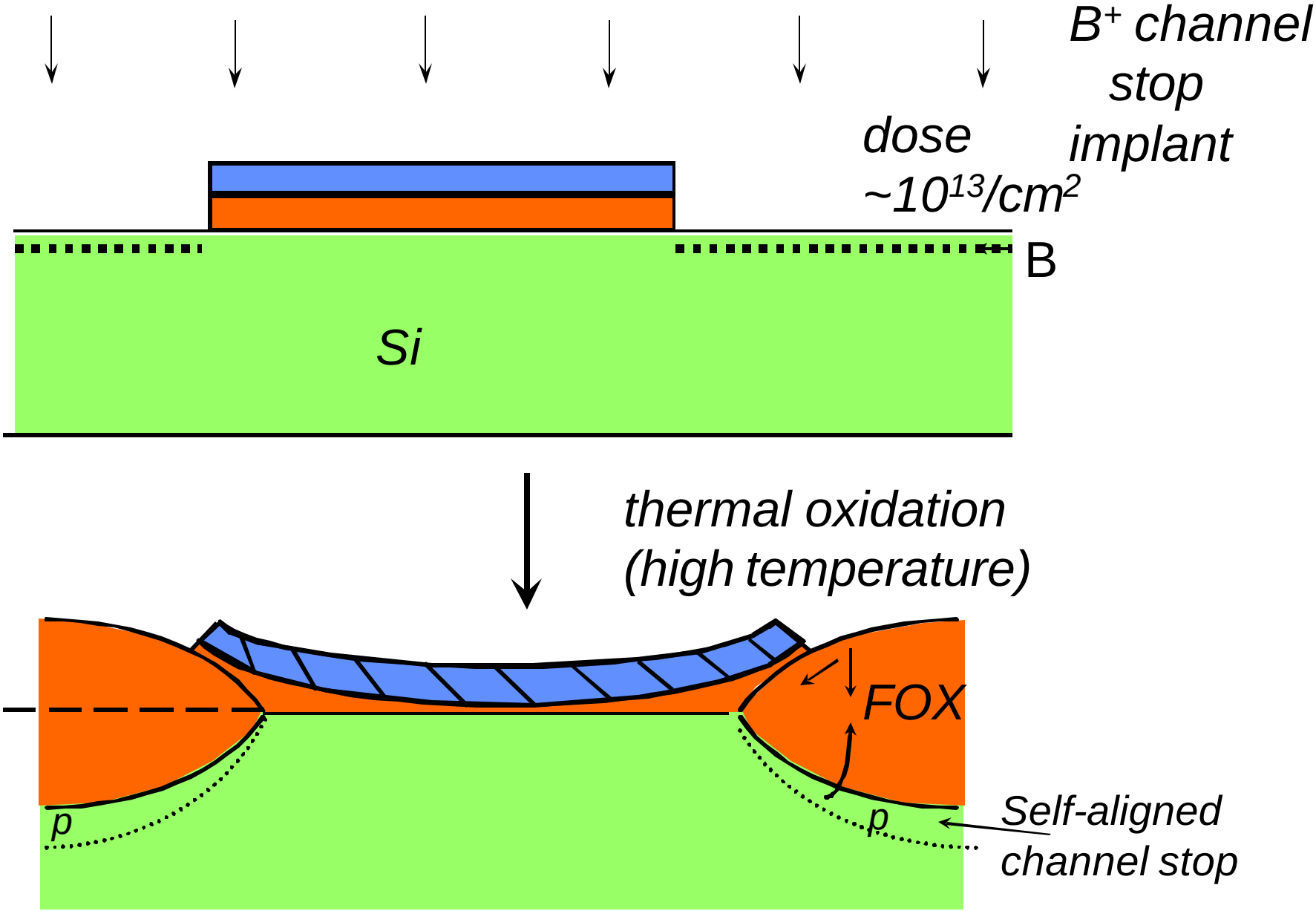
Example IC Process Flows
- NMOS - Generic NMOS Process Flow
- CMOS - The MOSIS Process Flow

Advance MOS Techniques
- Twin Well CMOS , Retrograde Wells , SOI CMOS

Self-aligned channel stop with Local Oxidation (LOCOS)

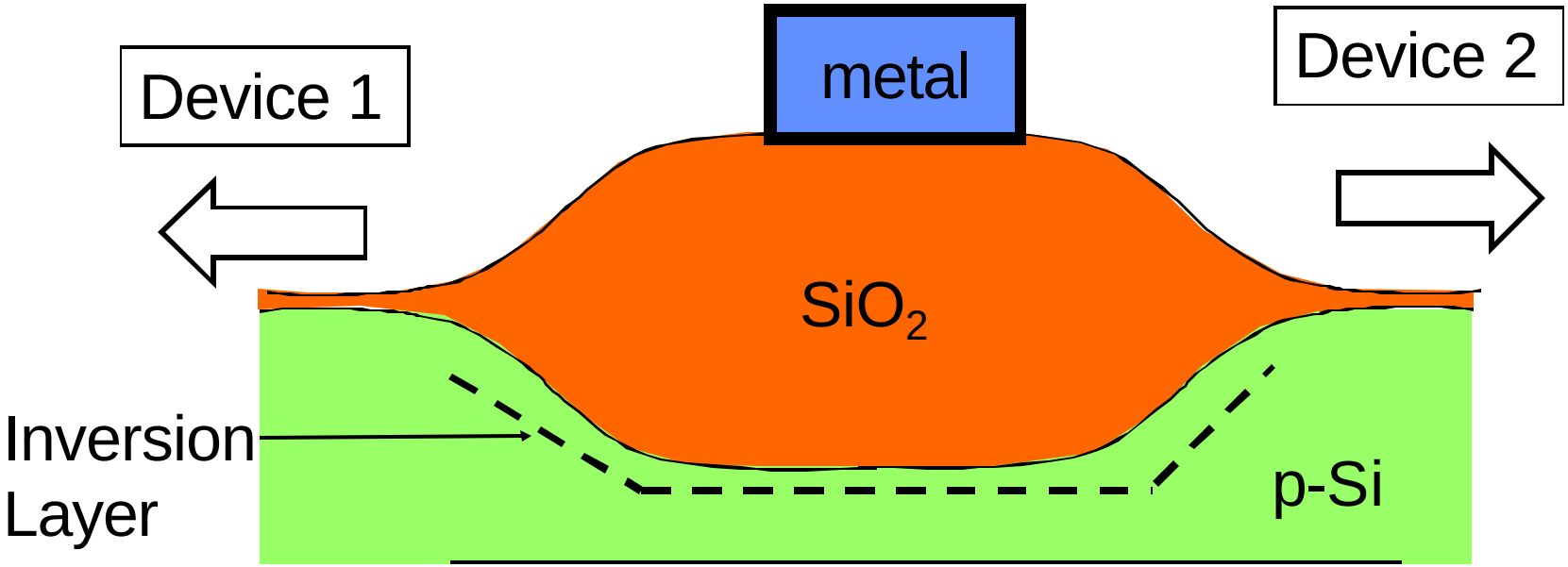
LOCOS Process Flow



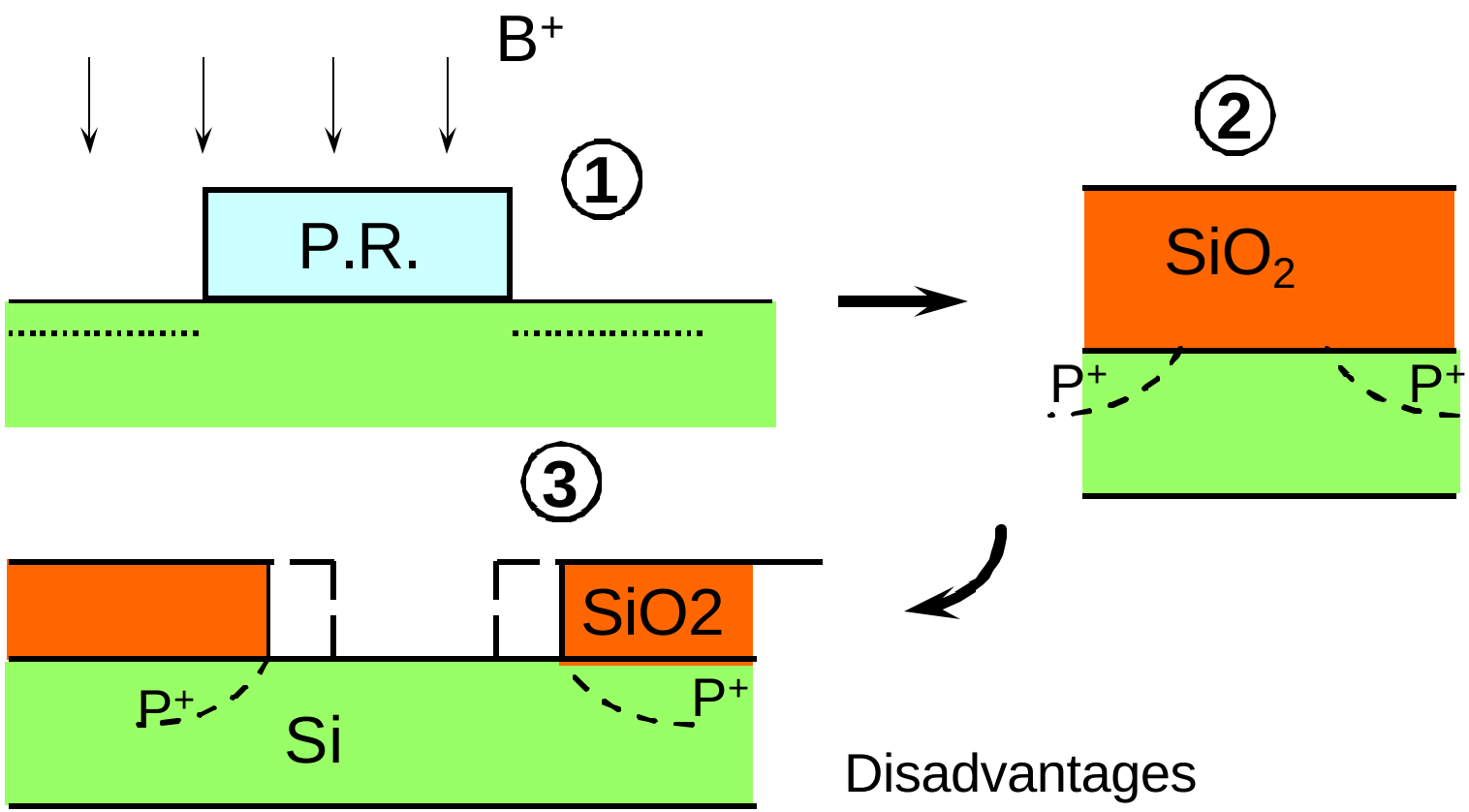

B+ channel stop implant
dose ~10^13/cm^2
B
Si
thermal oxidation (high temperature)
FOX
p
p
Self-aligned channel stop

Comment: Field Oxide Channel Inversion

If poly or metal lines lie on top of the Field Oxide (FOX), they will form a parasitic MOS structure.If these lines carrying a high voltage, they may create an inversion layer of free carriers at the Si substrate and shorts out neighboring devices. **The relatively highly doped Si underneath (the "channel stop") raises the threshold voltage of this parasitic MOS. If this threshold voltage value is higher than the highest circuit voltage, inversion will not occur.**



Comments : Non self-aligned alternative:

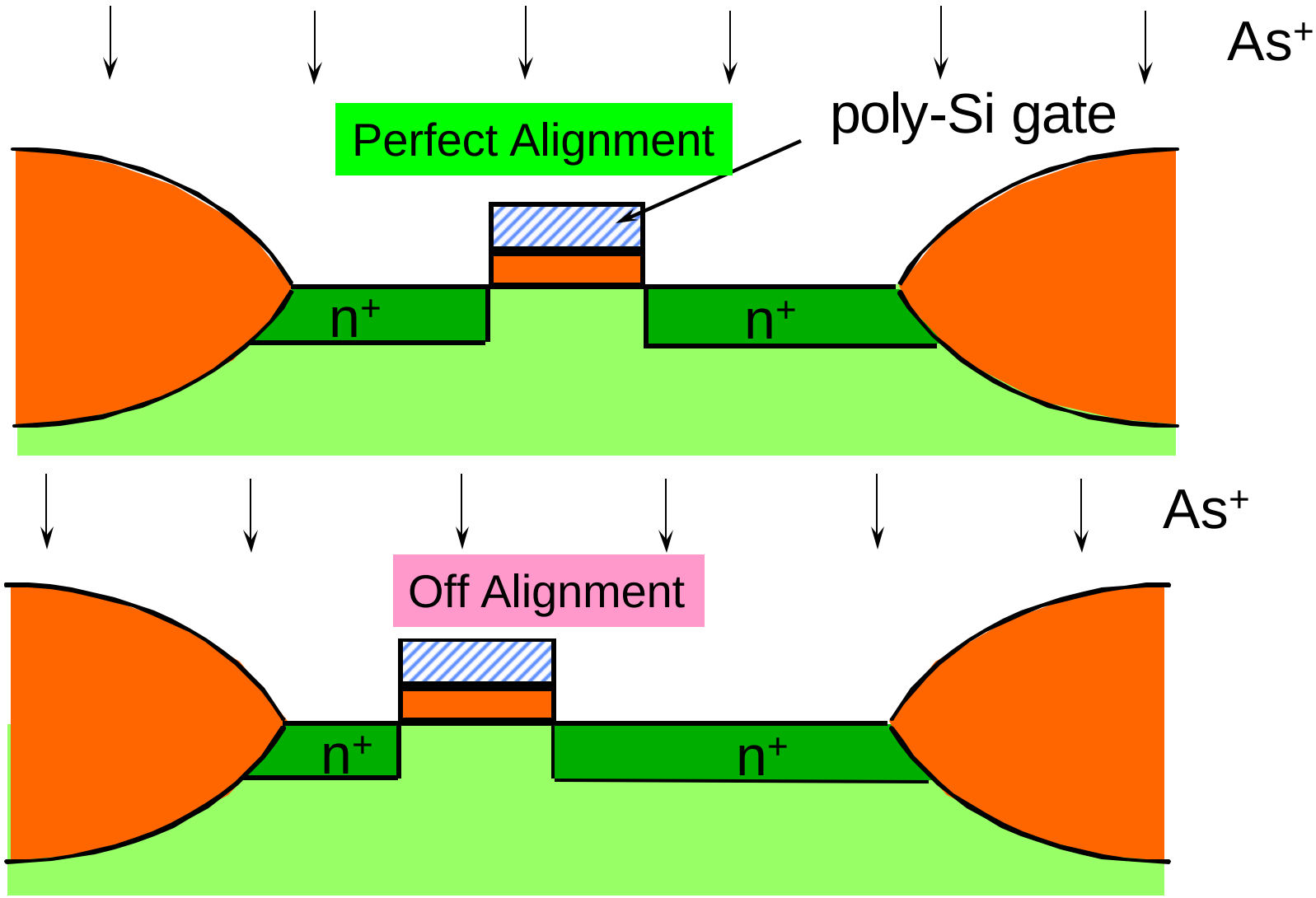


Disadvantages

1 Two lithography steps

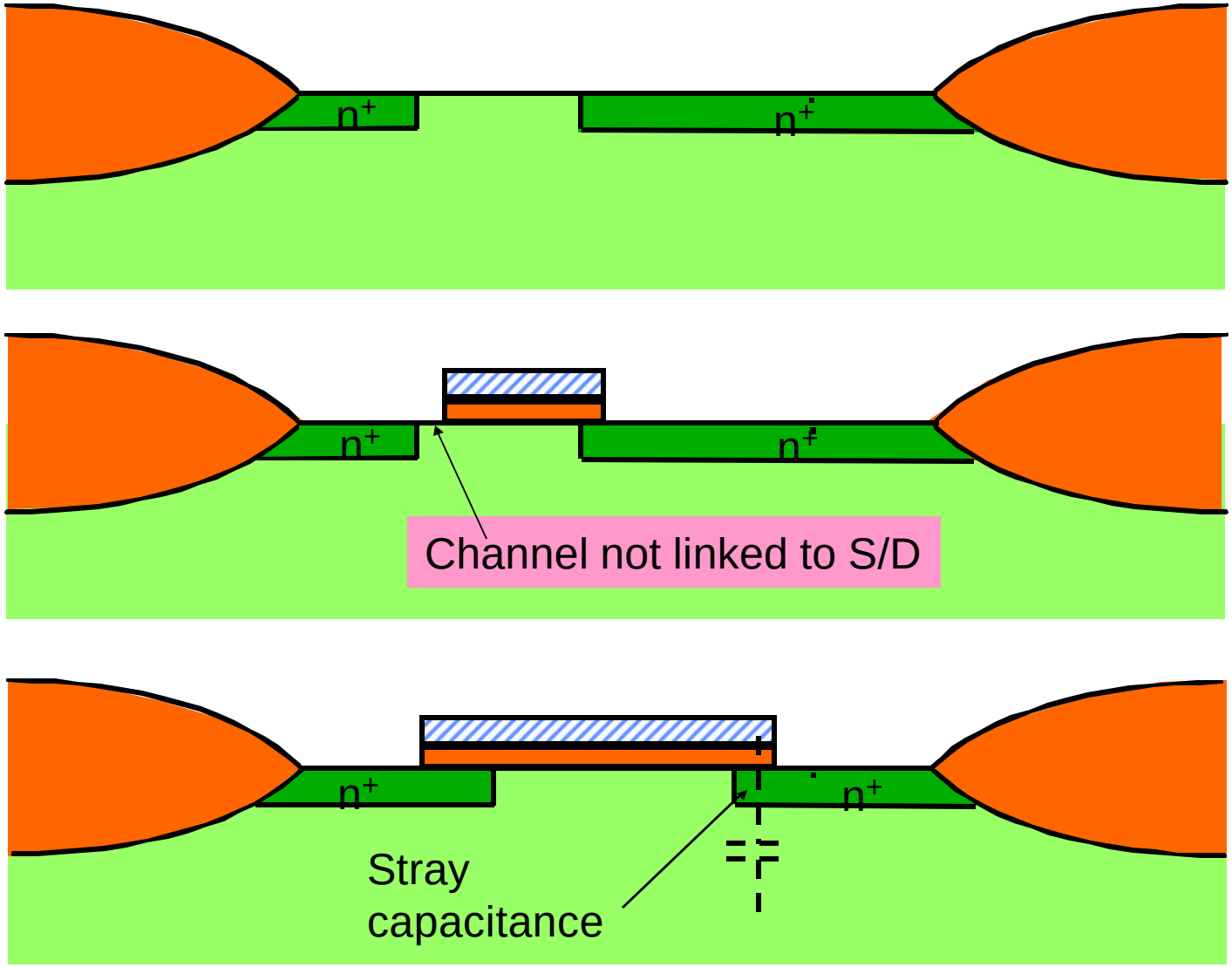
2 Channel stop doping not FOX aligned

Self-aligned Source and Drain



* The n+ S/D always follows gate

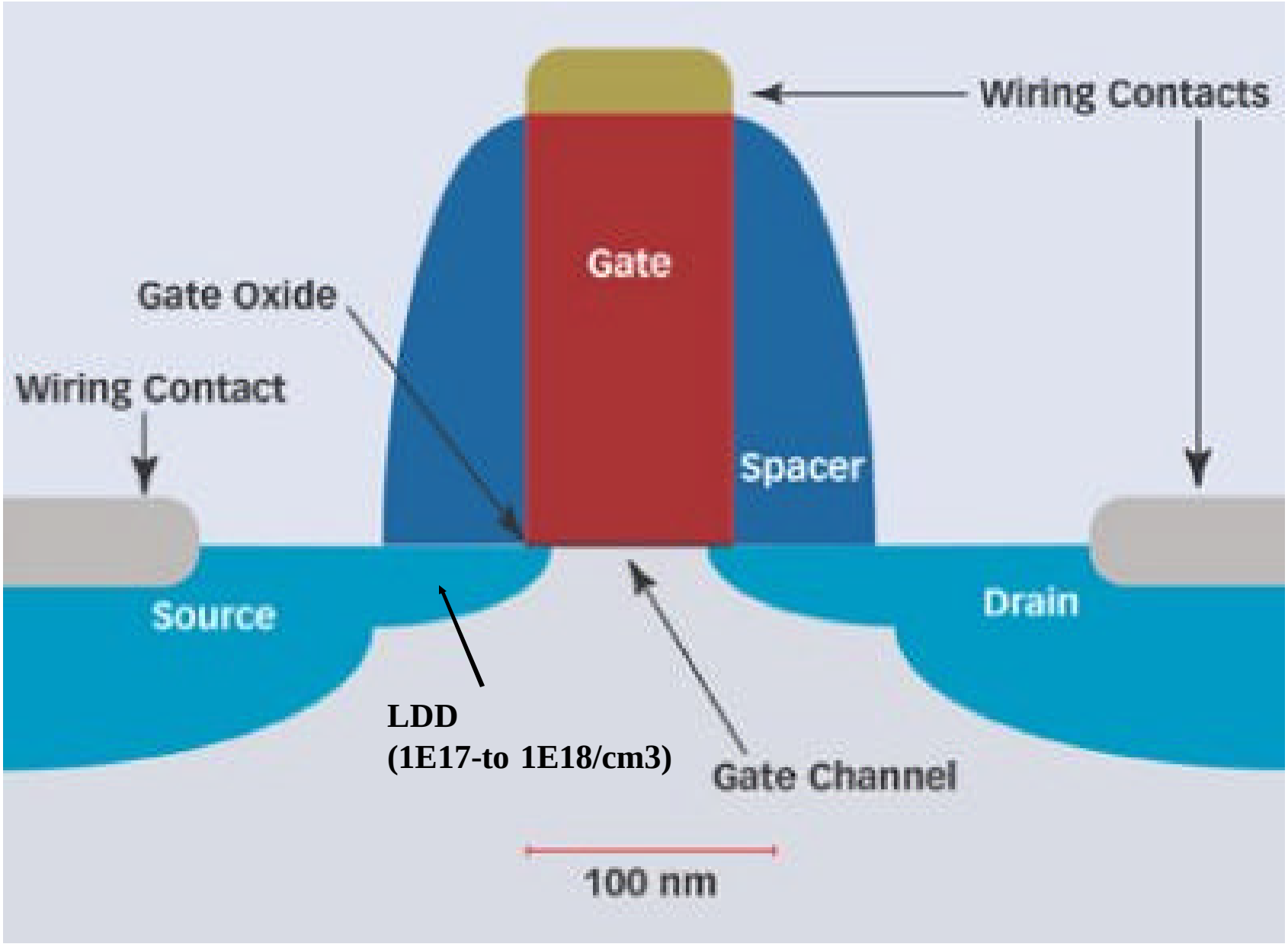
Comment: Non self-aligned Alternative



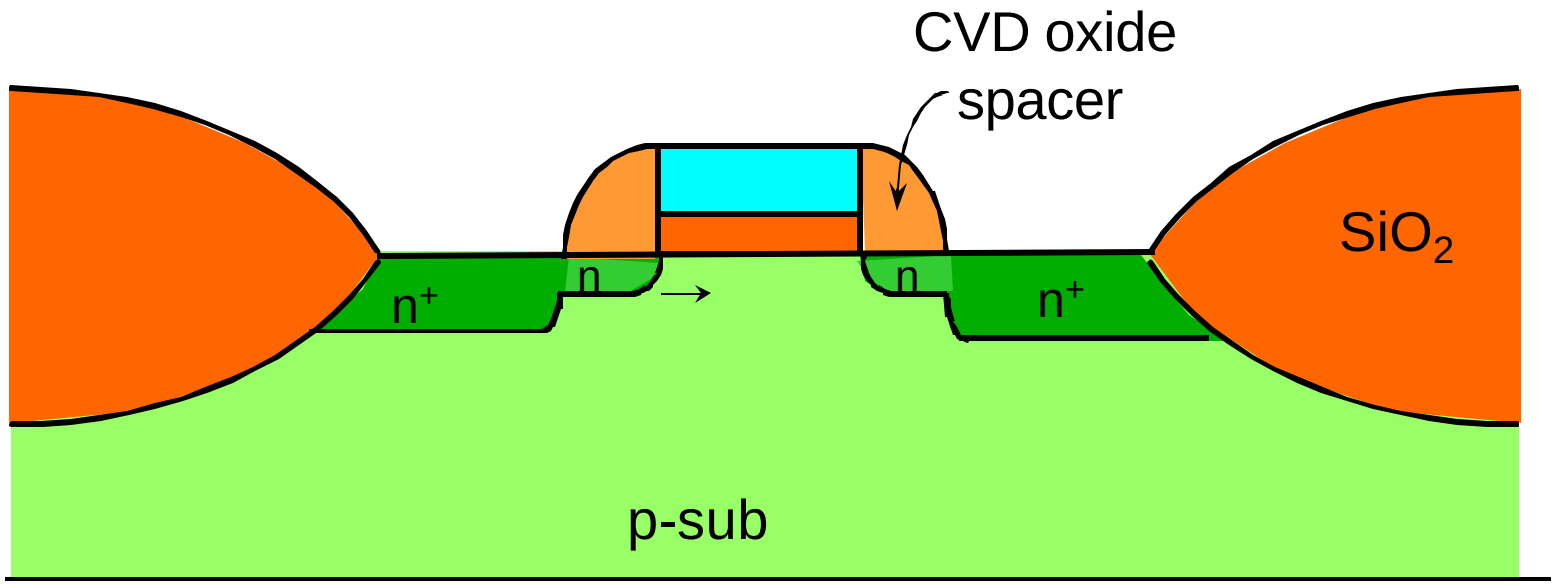
Solution: Use gate overlap to avoid offset error.

Disadvantages: Two lithography steps, excess gate overlap capacitance

Lightly Doped Drain (LDD)

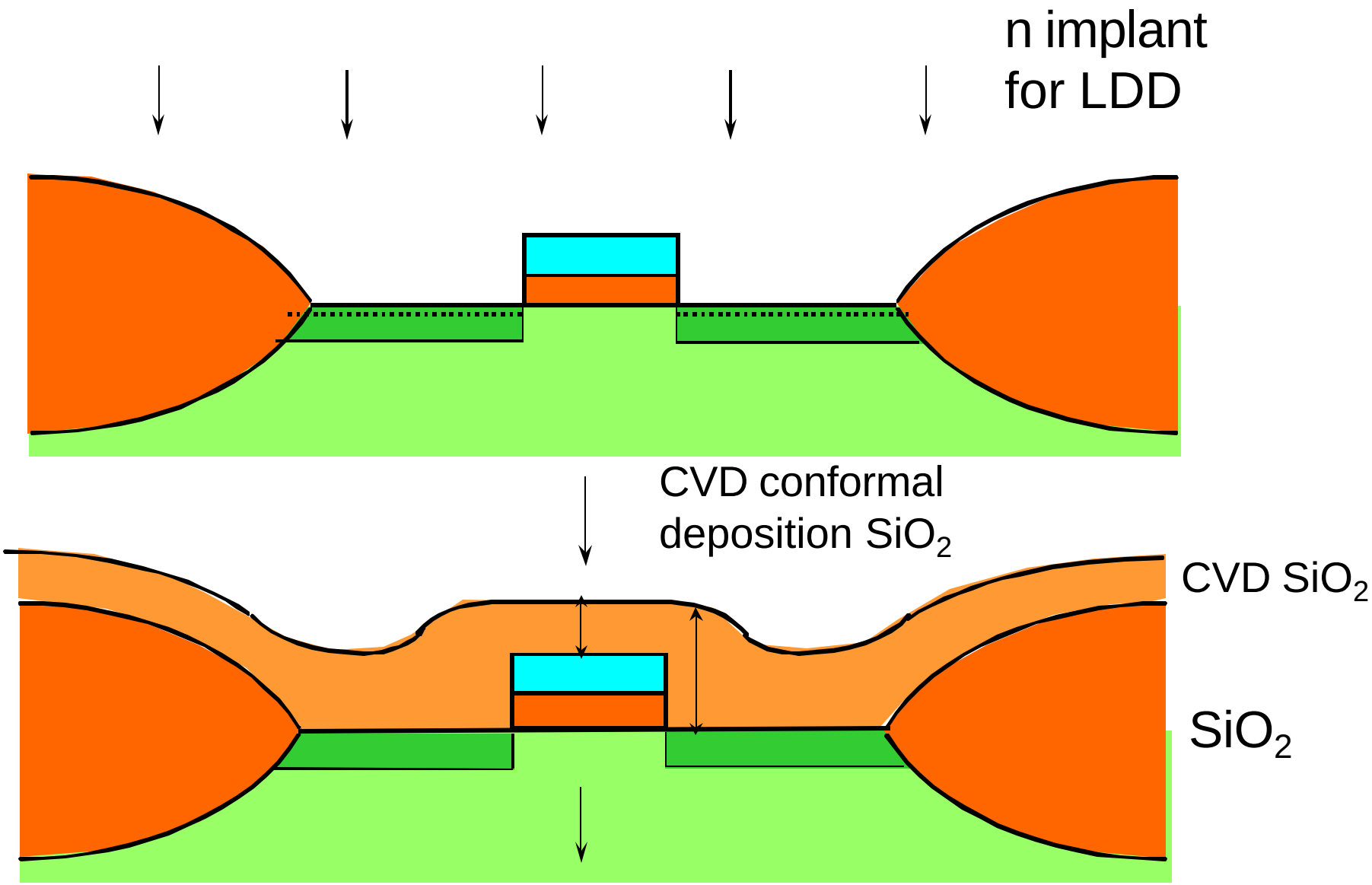


Lightly Doped Source/Drain MOSFET (LDD)

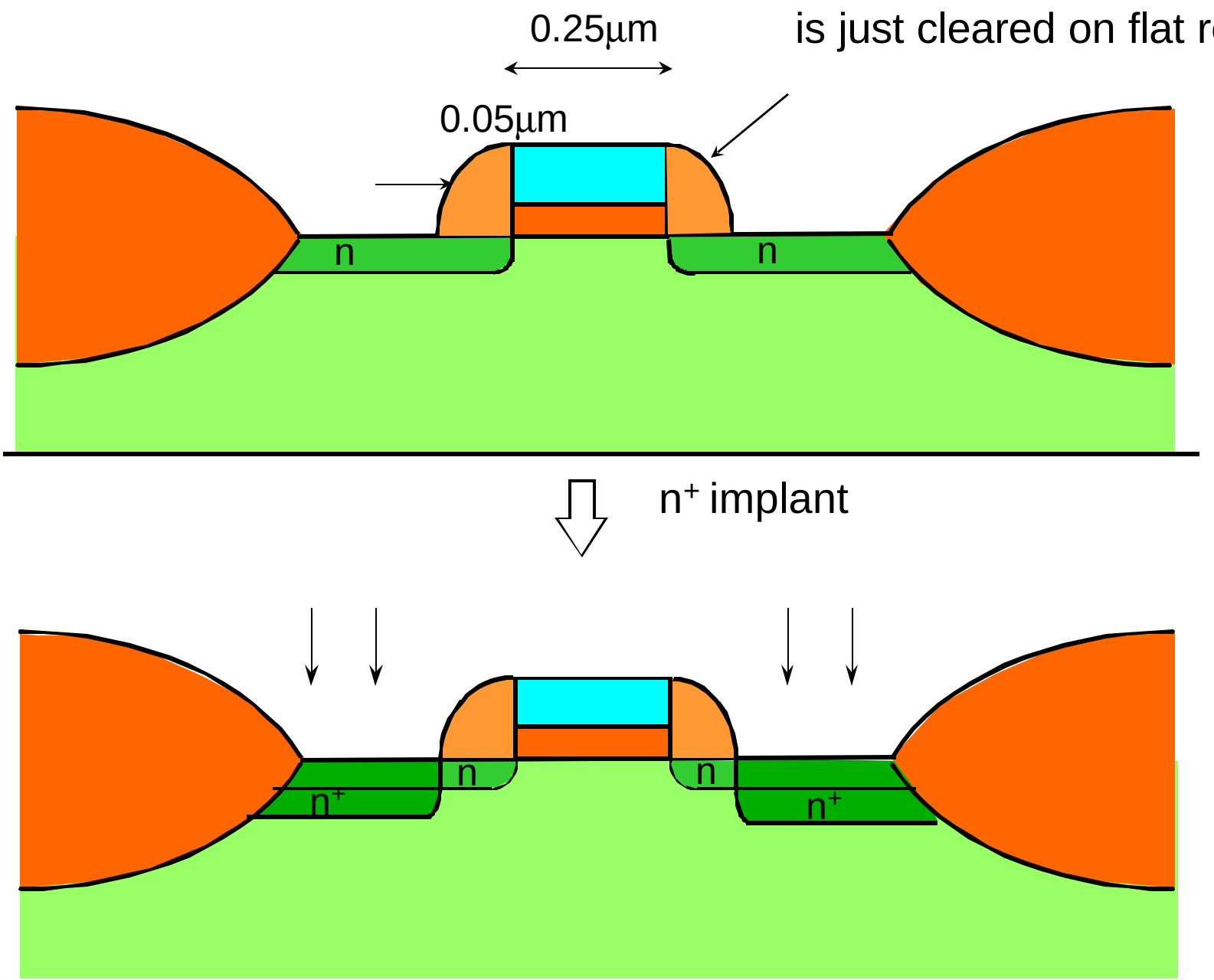


The n-pockets (LDD) doped to medium conc (~1E18) are used to smear out the strong E-field between the channel and heavily doped n+ S/D, in order to reduce hot-carrier generation.

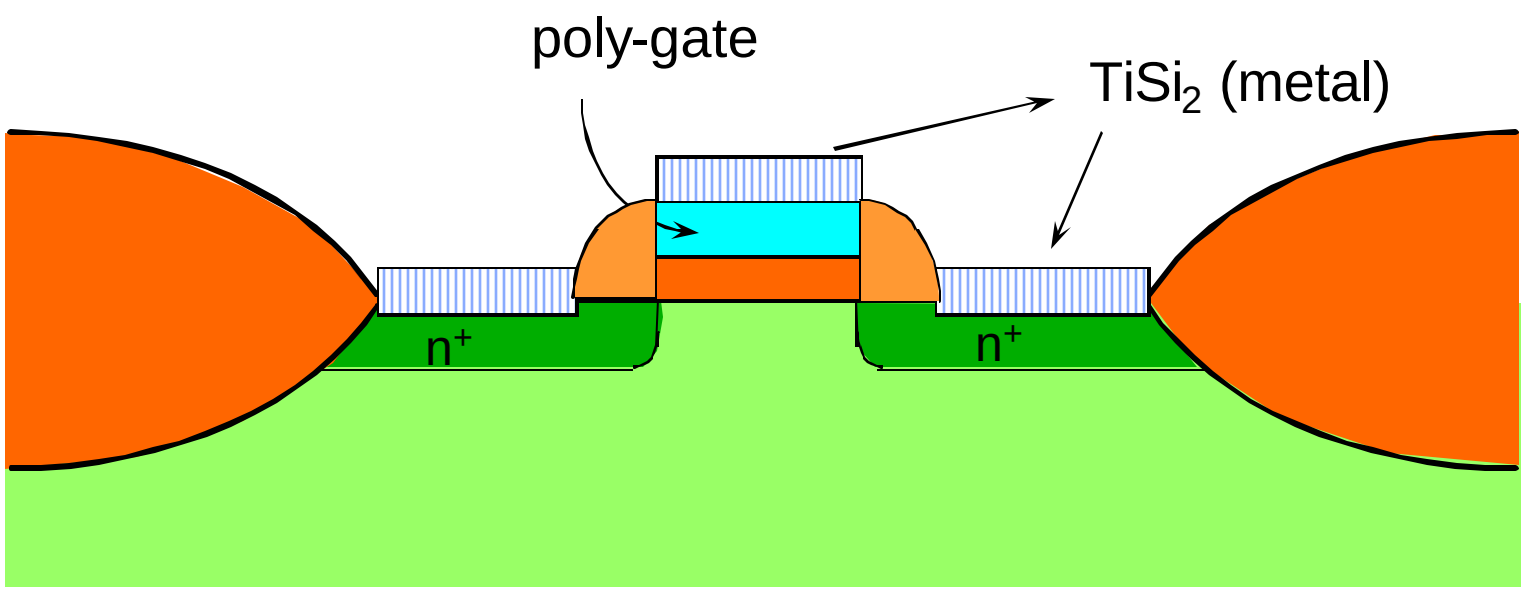
LDD Process Flow using Ion Implantation



Spacer left when CVD SiO_2 is just cleared on flat region.

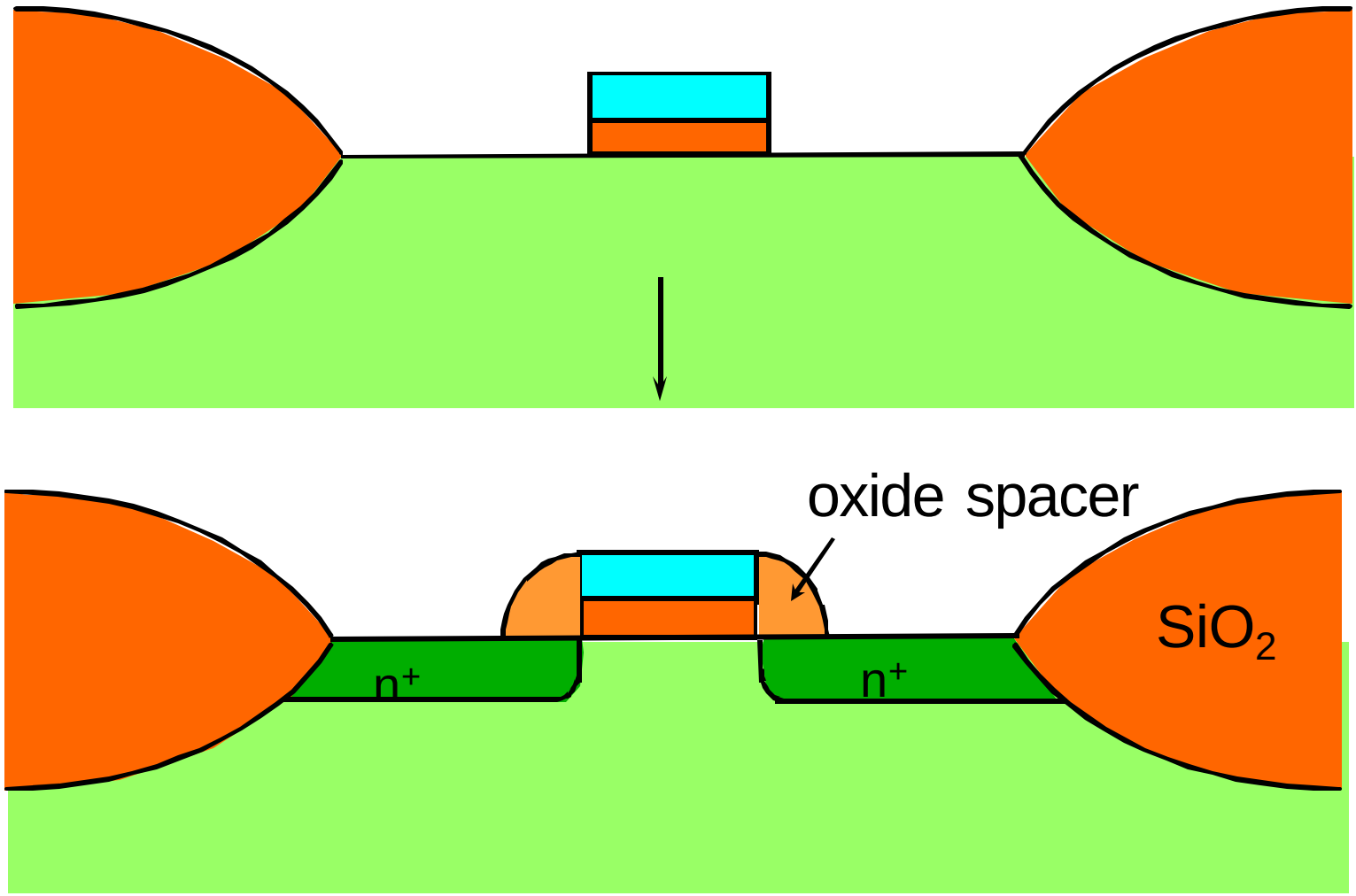


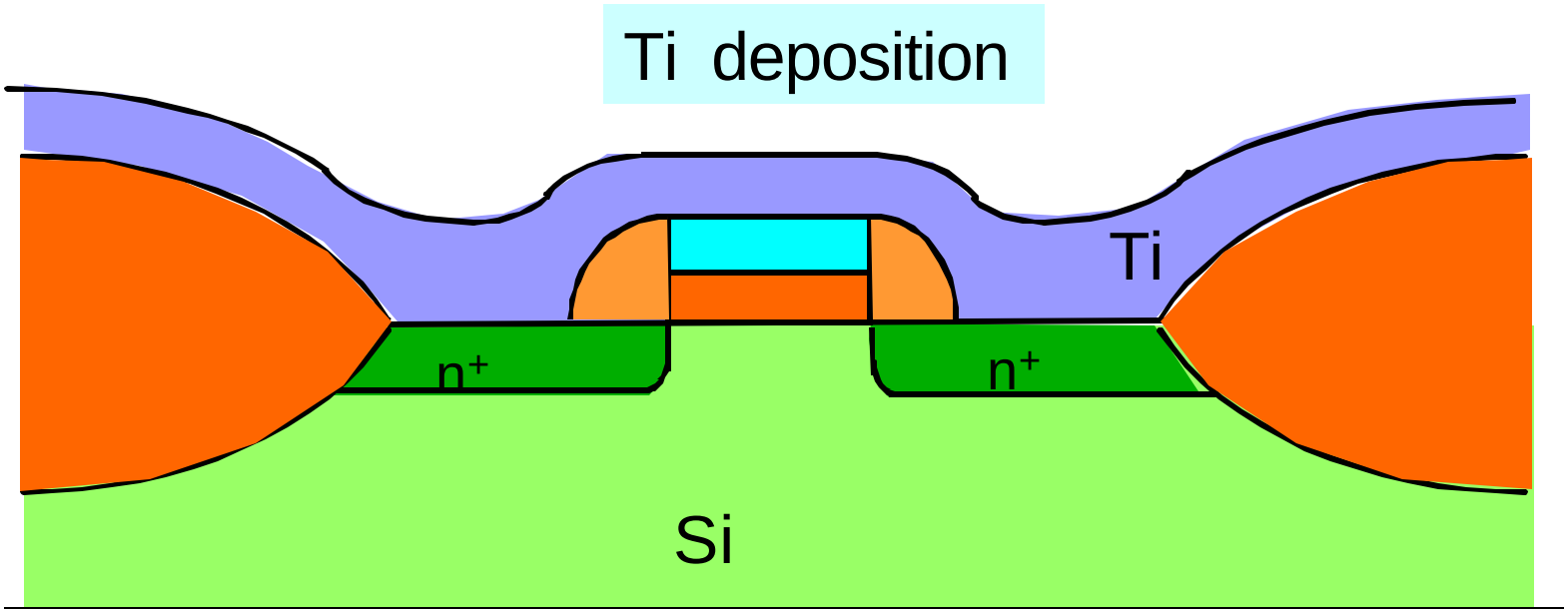
Self-Aligned Silicide Process (**SALICIDE**) using Ion Implantation and Metal-Si reaction



Metal silicides are metallic.
They lower the sheet resistance of S/D and the poly-gate

SALICIDE Process Flow

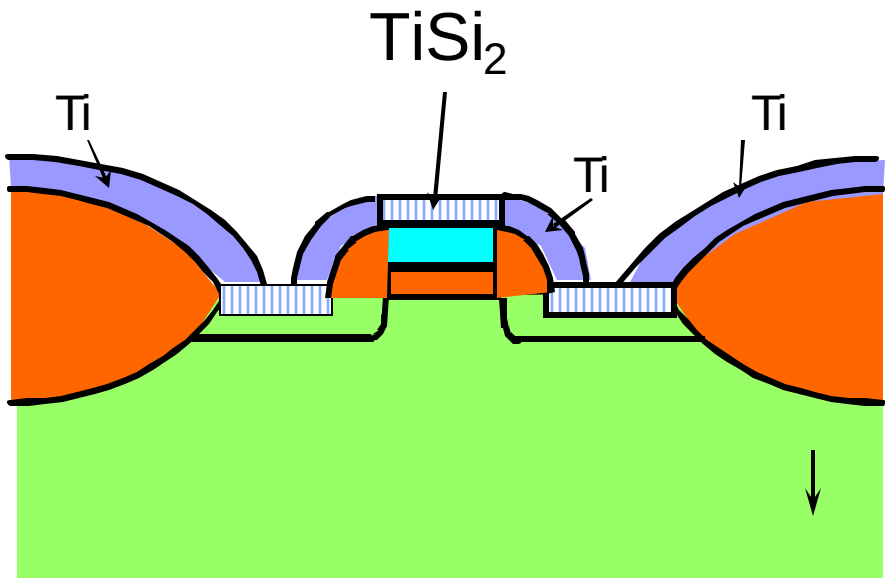




$$heat\ treatment\ (> 700^{o}C)$$

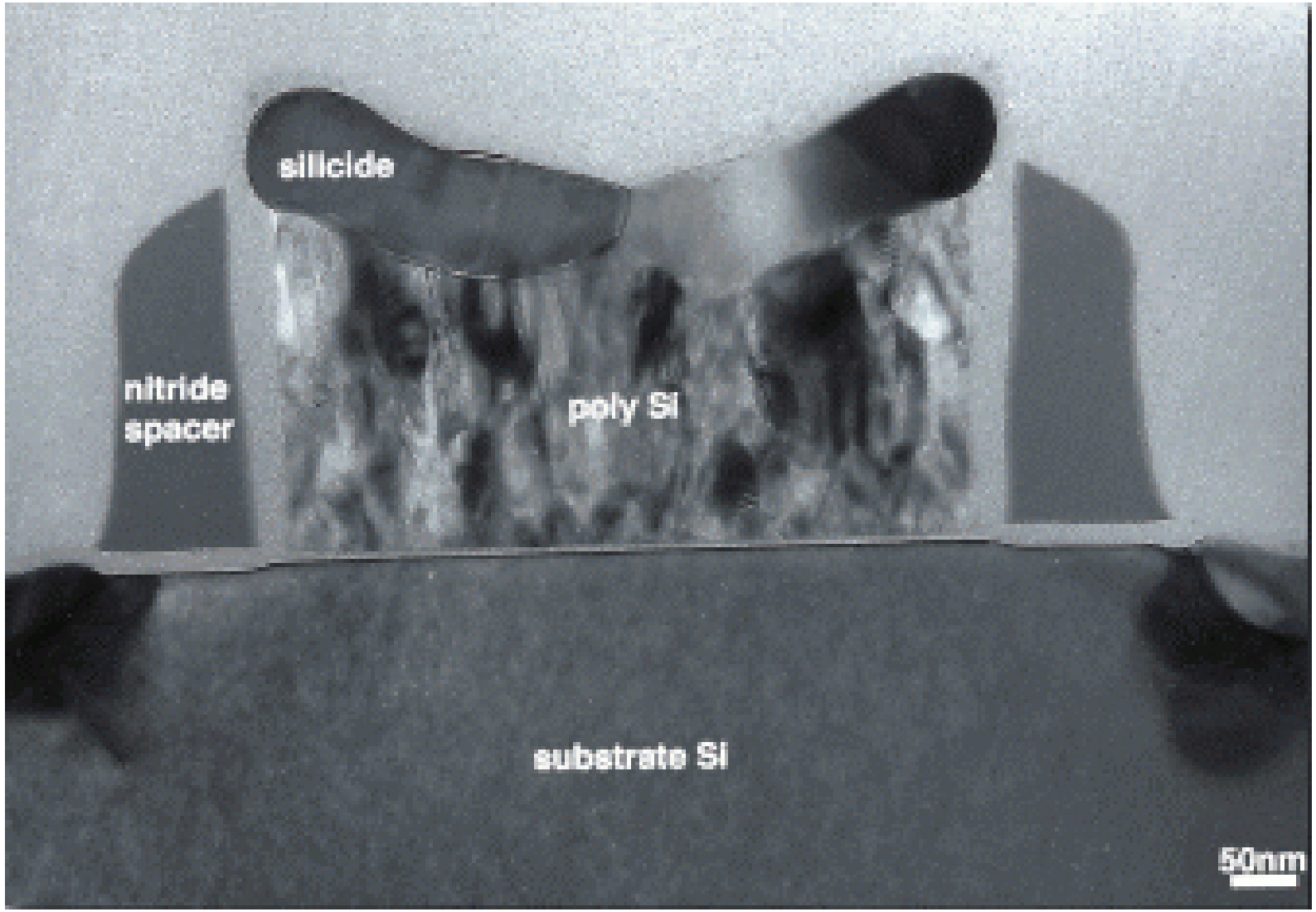
$$Ti + 2Si \rightarrow TiSi_2$$

$$Ti\ will\ not\ react\ with\ SiO_2.$$



Selective etch to remove unreacted Ti only

Salicide Gate TEM

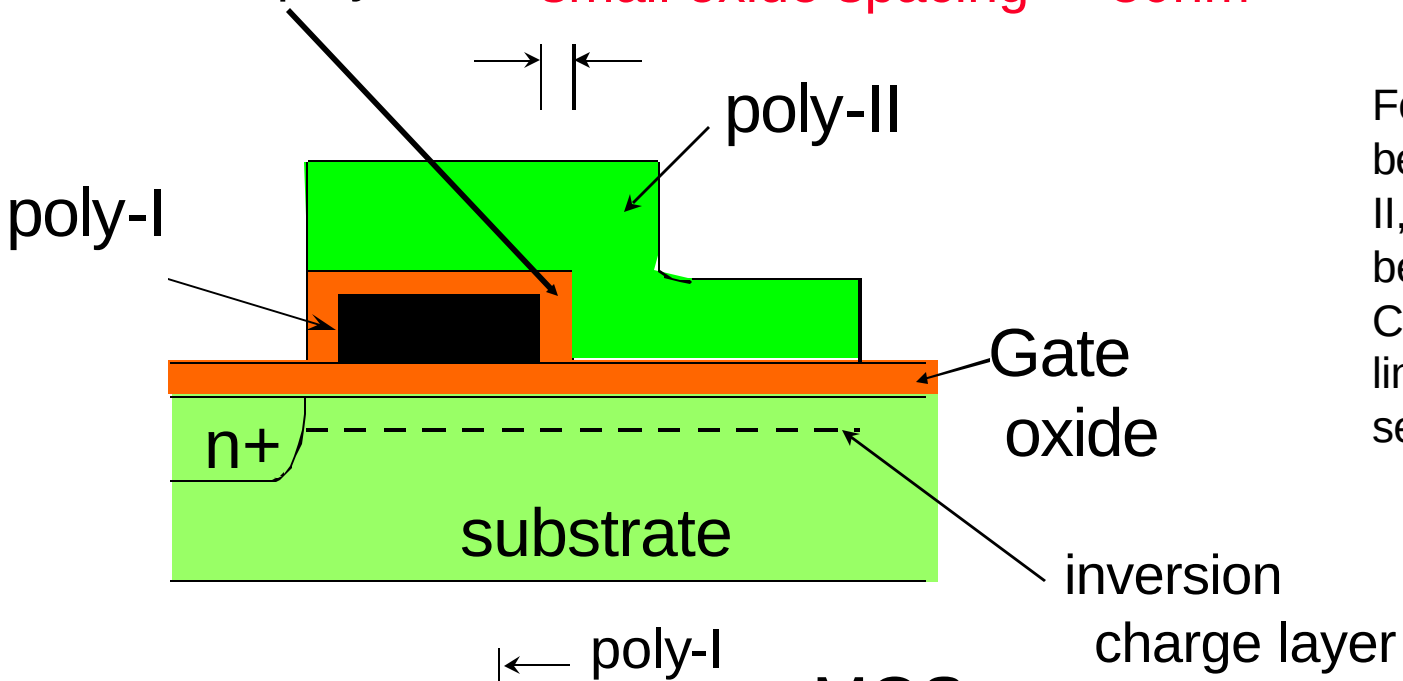


Self-aligned Oxide Gap

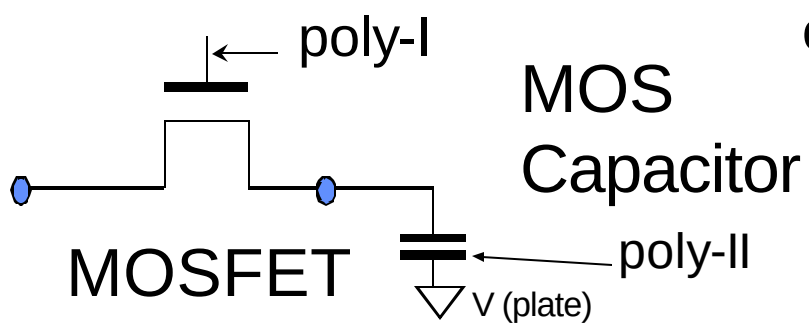
DRAM structure (MOSFET with a capacitor)

Thermal Oxide grown conformal on poly-I

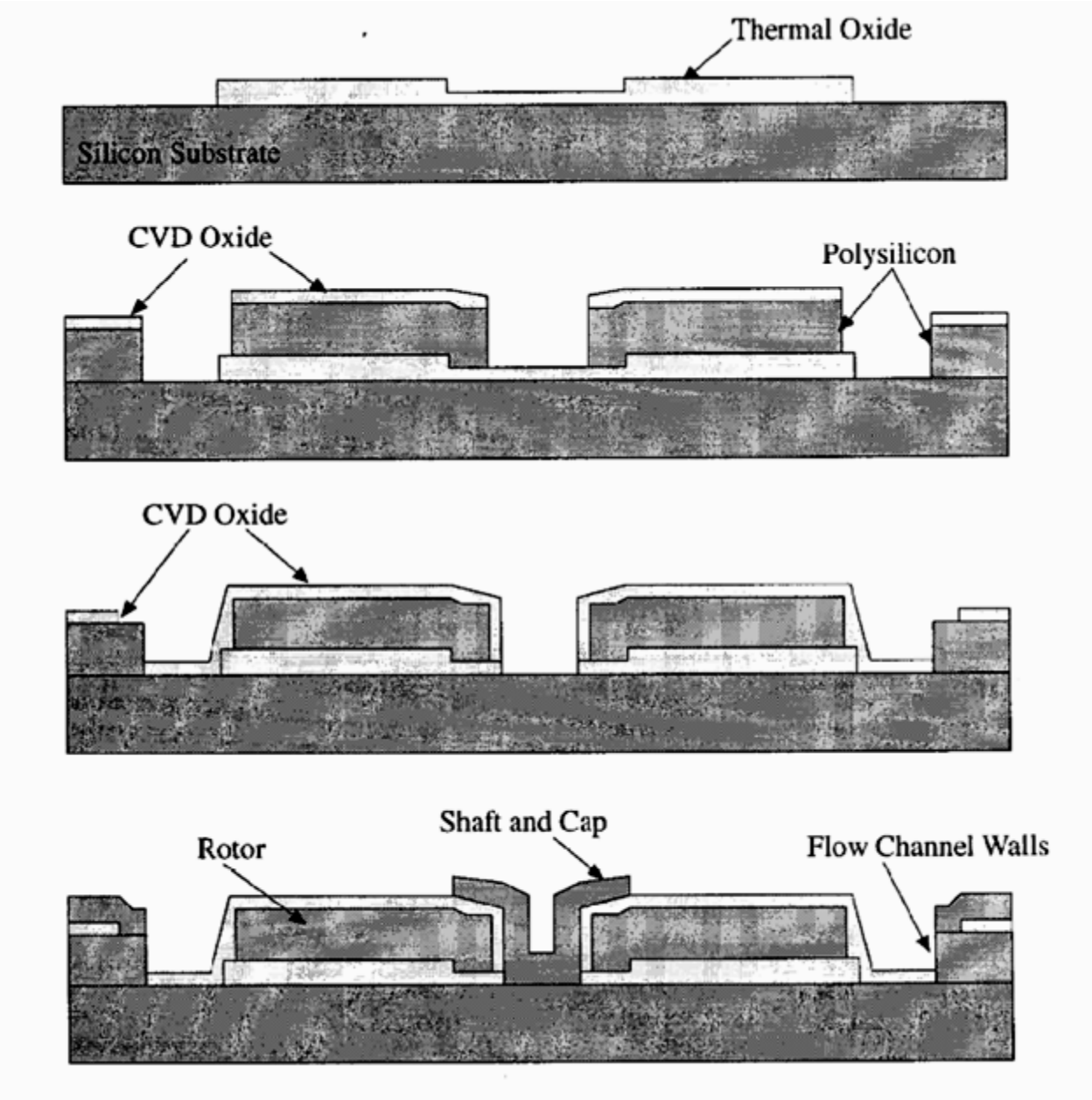
small oxide spacing < 30nm



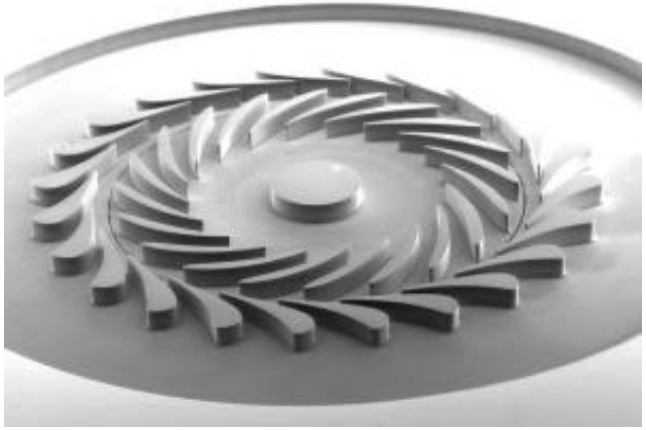
For a small spacing between poly-I and poly-II, inversion charges between MOSFET and Capacitor are electrically linked. No need for a separate n+ island.



Process Flow of MEMS Rotating Mechanisms

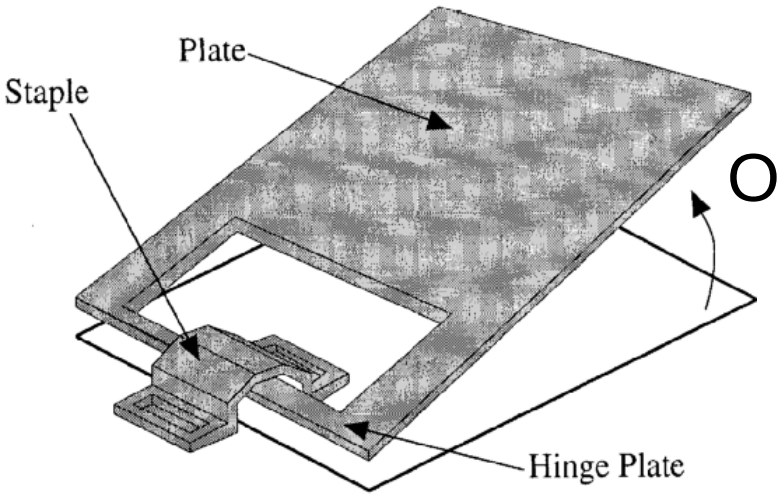


In-Plane Movement

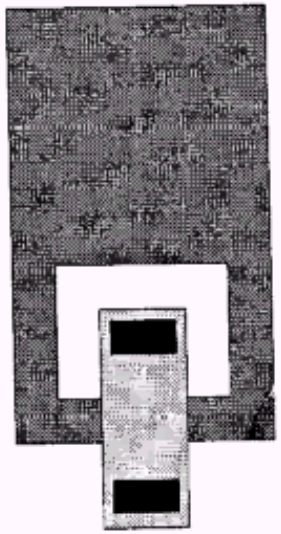


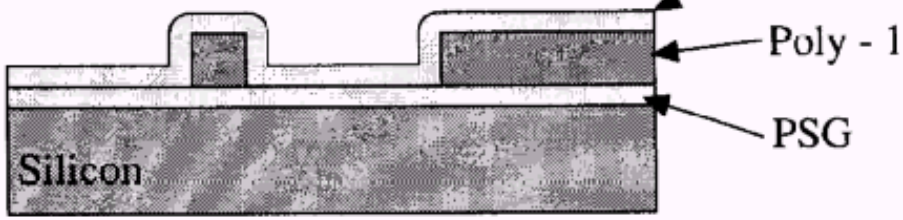
Micro-turbine Engine

Process Flow for a Hinge Structure

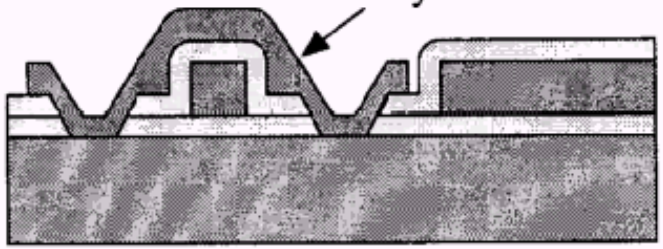


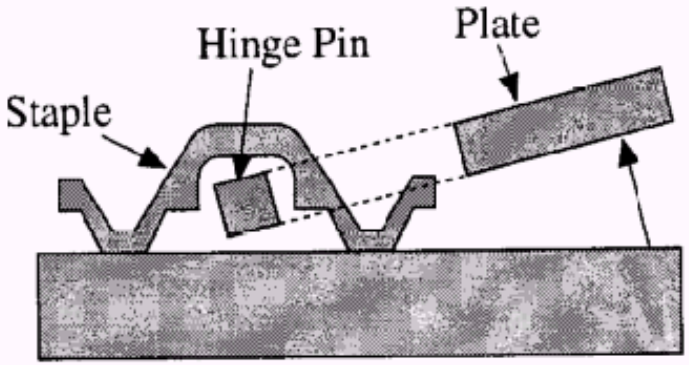
Out-of-plane Movement



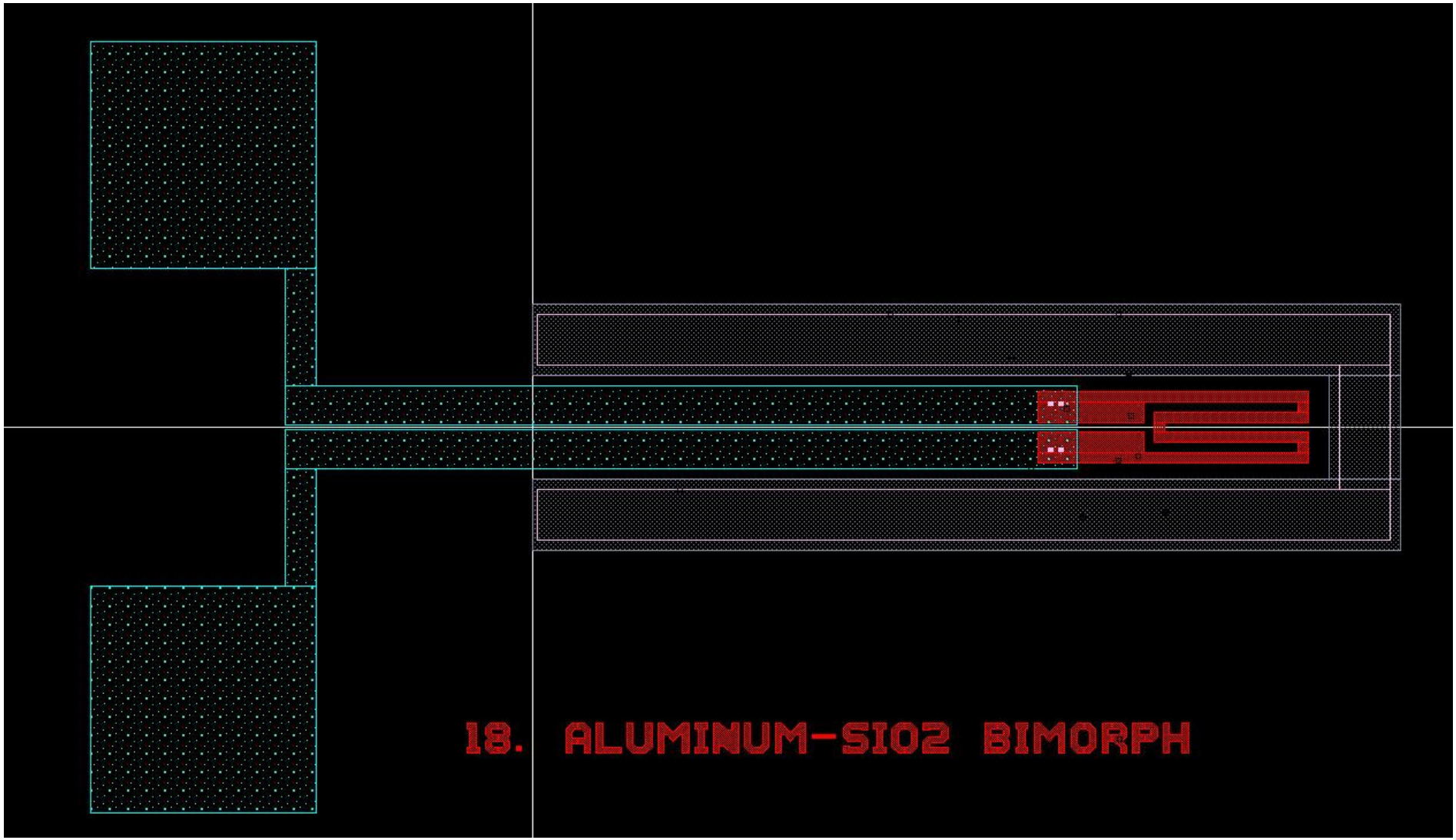


Poly - 1
Poly - 2
Contact



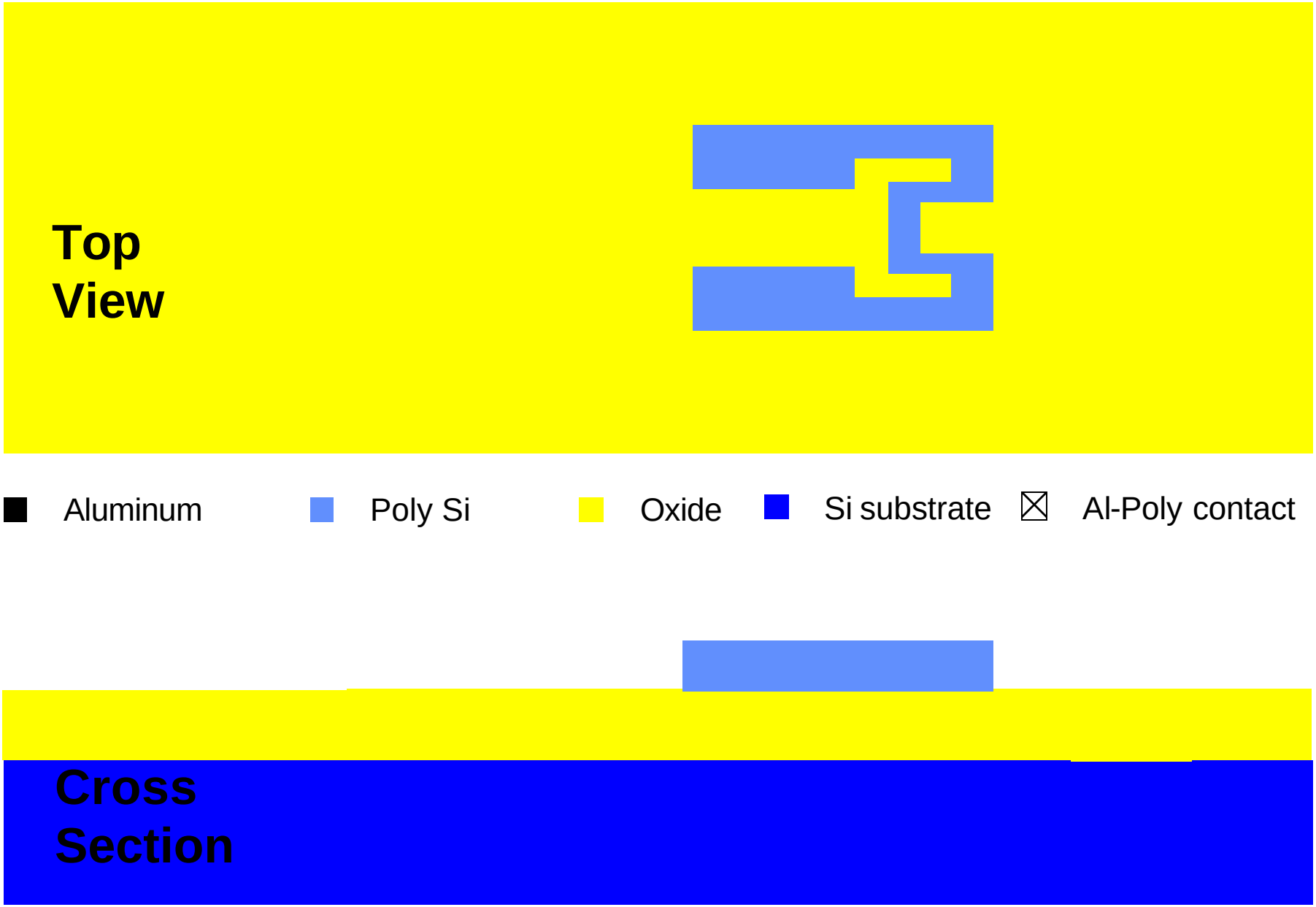


Layout of Thermal Bimorph Actuator



(See 143 Lab Manual for details)

After Patterning Poly-Si (Mask #2)



After Patterning Intermediate Oxide (Mask #3, Contact-Hole Cut)

After Aluminum patterning (Mask #4)

After XeF2 selective etching of Si Substrate (Final Structure)

A Generic NMOS Process Flow

Substrate
Boron doped (100)Si
Resistivity= 20 Ω-cm

→ Thermal Oxidation ~100Å pad oxide

→ CVD Si_3N_4 ~ 0.1 um

→ Lithography Pattern Field Oxide Regions

→ RIE removal of Nitride and pad oxide

→ Channel Stop Implant: $3x10^{12}$ B/cm^2 60keV

→ Thermal Oxidation to grow 0.45um oxide

→ Wet Etch Nitrdie and pad oxide

→ Ion Implant for Threshold Voltage control $8x10^{11}$ B/cm^2 35keV

→ Thermal Oxidation To grow 250Å gate oxide

→ LPCVD Poly-Si ~ 0.35um

→ Dope Poly-Si to n+ with Phosphorus Diffusion source

→

A Generic NMOS Process Flow (cont.)

Lithography
Poly-Si
Gate pattern

→

RIE
Poly-Si
gate

→

Source /Drain
Implantation
~ 10^{16} As/cm^2 80keV

→

Thermal Oxidation
Grow ~0.1um oxide
on poly-Si
And source/drian

→

LPCVD
SiO2
~0.35um

→

Lithography
Contact
Window pattern

→

RIE removal of
CVD oxide and
thermal oxide

→

Sputter Deposit
Al metal
~0.7um

→

Lithography
Al interconnect
pattern

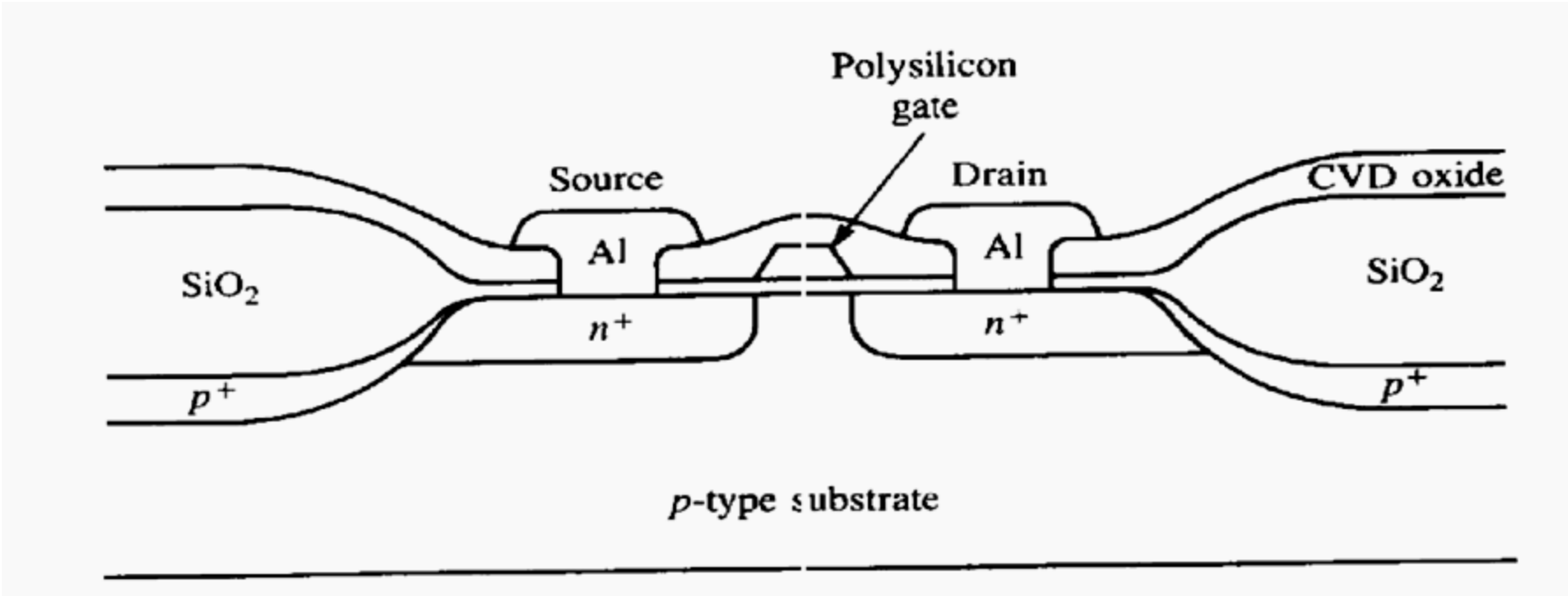
→

RIE etch of
Al metallization

→

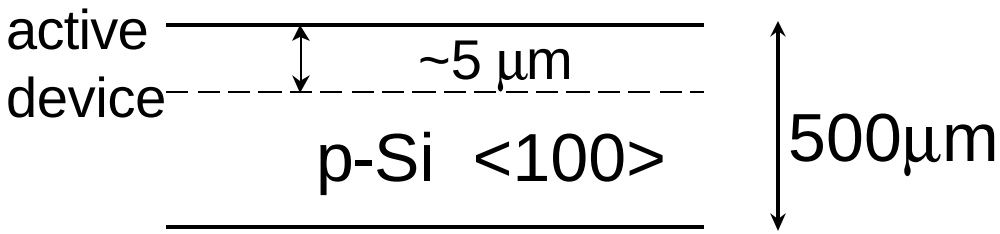
Sintering at ~400ºC in H2 ambient
to improve contact resistance
and to reduce oxide interface charge

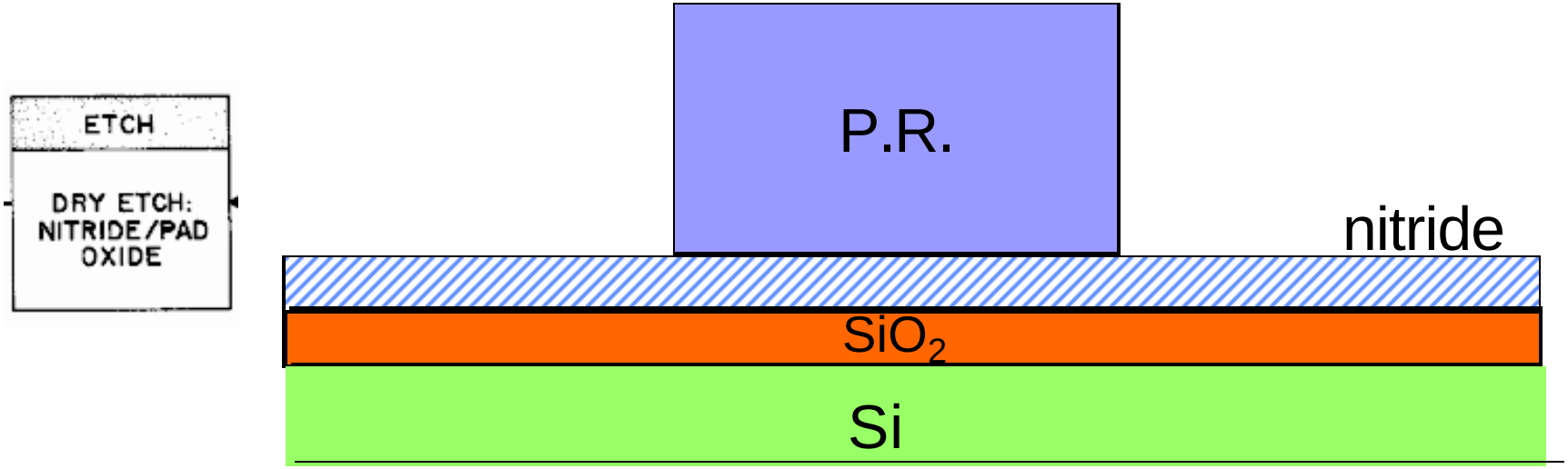
NMOS Structure

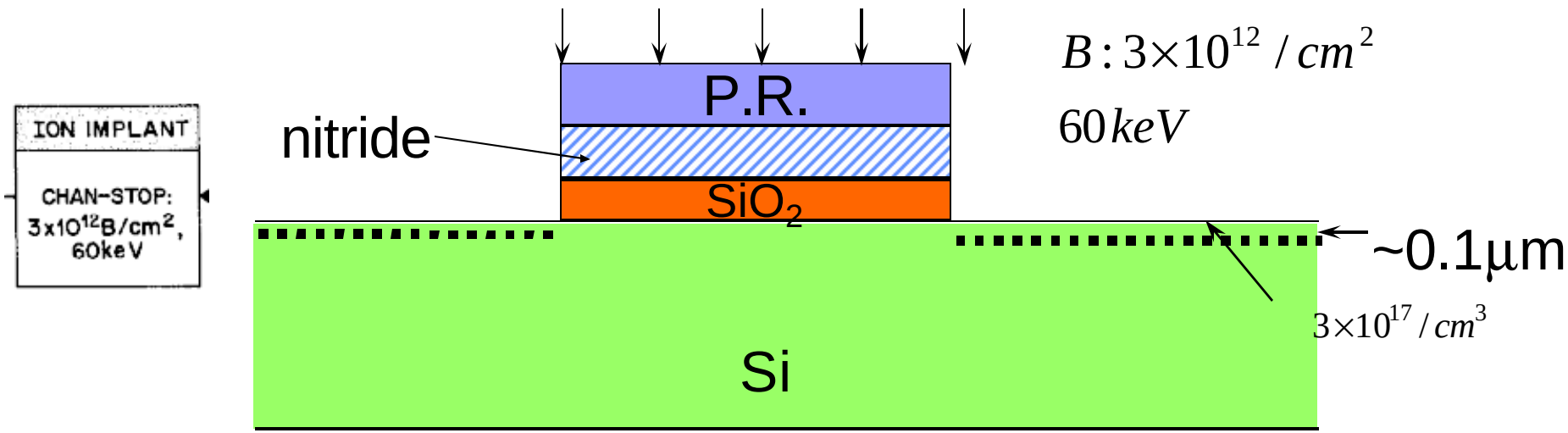


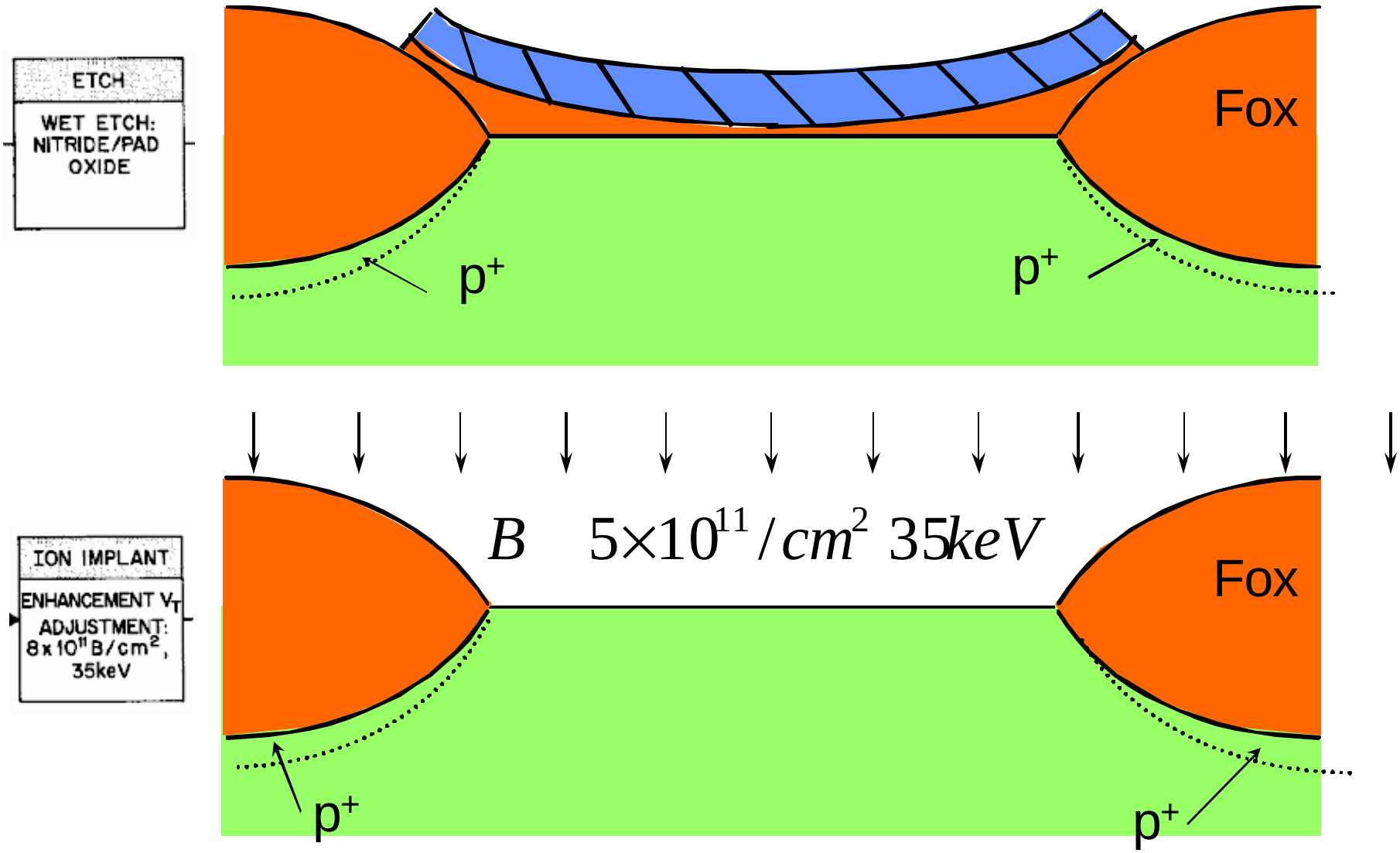
Generic NMOS Process Flow

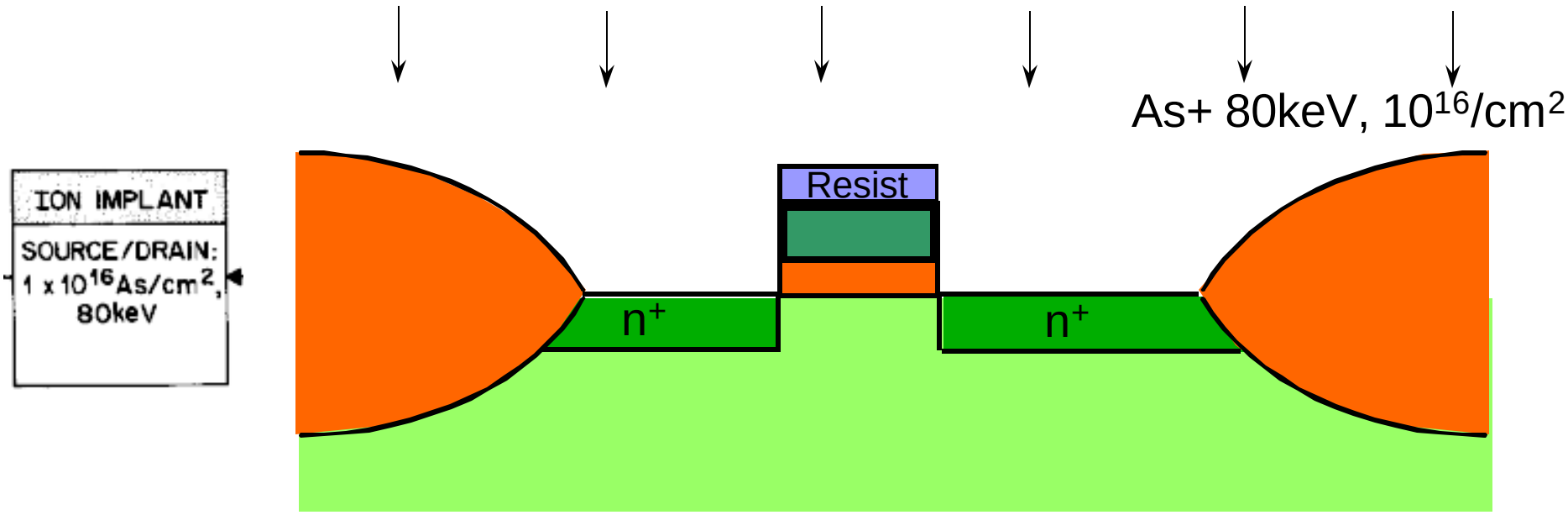
Boron-doped Si
20 Ω-cm
<100>

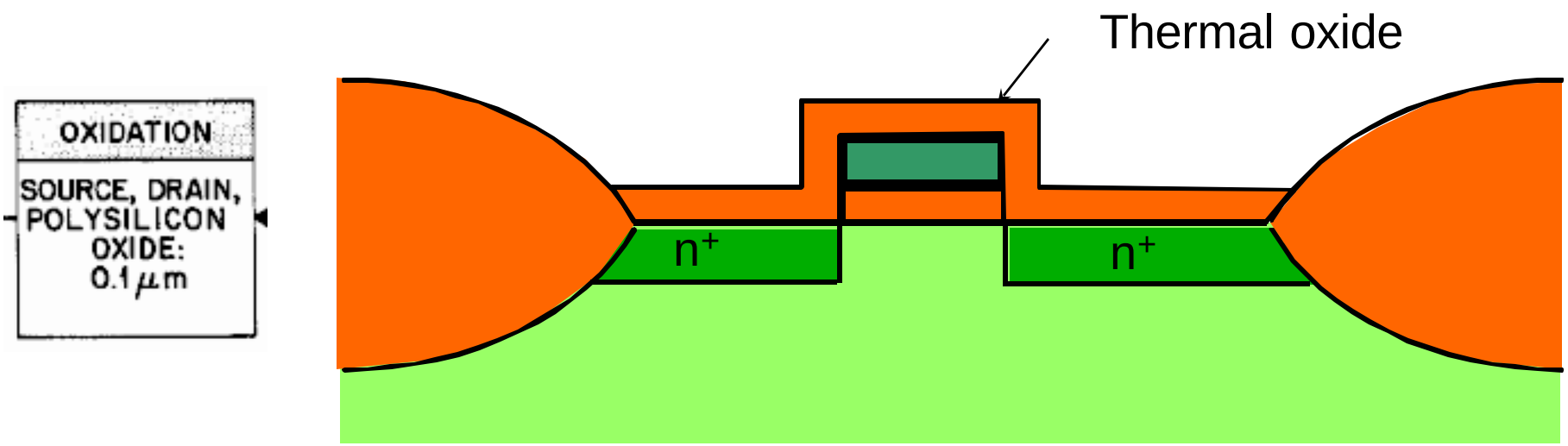


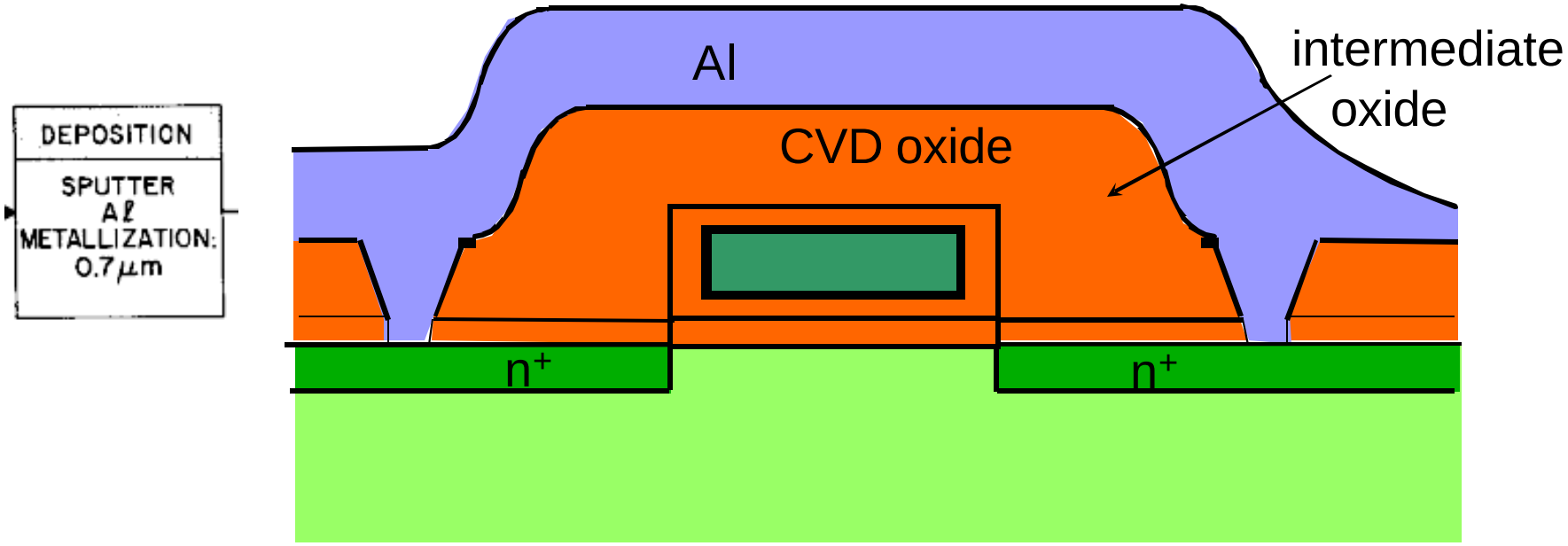

ETCH
DRY ETCH:
NITRIDE/PAD
OXIDE
P.R.
nitride
SiO2
Si

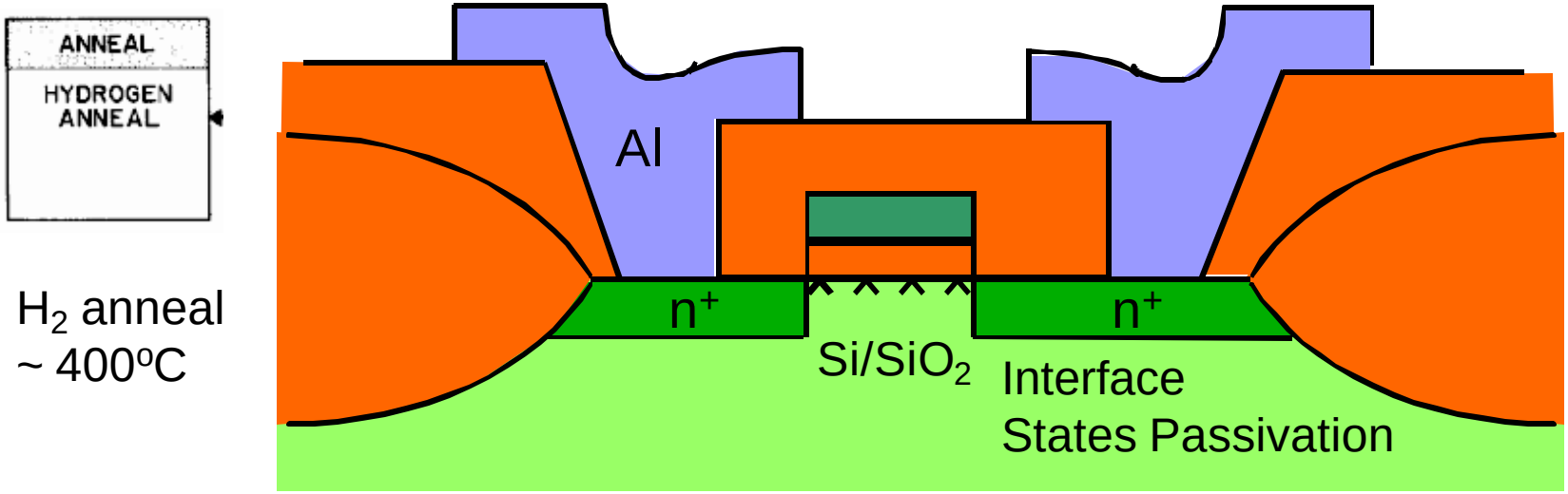

ION IMPLANT
CHAN-STOP:
3x10^12B/cm^2,
60keV
P.R.
nitride
SiO2
Si
$B: 3\times10^{12}/cm^2$
$60\,keV$
~0.1μm
$3\times10^{17}/cm^3$


ETCH
WET ETCH:
NITRIDE/PAD
OXIDE
Fox
p+
p+
ION IMPLANT
ENHANCEMENT V_T
ADJUSTMENT:
8×10^{11} B/cm^2,
35keV
$B \quad 5\times10^{11}/cm^2 \; 35keV$
Fox
p+
p+


As+ 80keV, 10^{16}/cm^2
ION IMPLANT
SOURCE/DRAIN:
1 x 10^{16} As/cm^2,
80keV
Resist
n+
n+


Thermal oxide
OXIDATION
SOURCE, DRAIN,
POLYSILICON
OXIDE:
0.1 μm
n+
n+





H_2 anneal
~ 400°C