Process Integration

Self-aligned Techniques
• LOCOS - self-aligned channel stop
• Self-aligned Source/Drain
• Lightly Doped Drain (LDD)
• Self-aligned silicide (SALICIDE)
• Self-aligned oxide gap

MEMS Release Techniques
• Sacrificial Layer Removal
• Substrate Undercut

Example IC Process Flows
• NMOS - Generic NMOS Process Flow
• CMOS - The MOSIS Process Flow

Advance MOS Techniques
• Twin Well CMOS, Retrograde Wells, SOI CMOS
Self-aligned channel stop with Local Oxidation (LOCOS)

LOCOS Process Flow
B\textsuperscript{+} channel stop implant
dose \sim 10^{13}/cm^{2}

thermal oxidation (high temperature)

Self-aligned channel stop
If poly or metal lines lie on top of the Field Oxide (FOX), they will form a parasitic MOS structure. If these lines carrying a high voltage, they may create an inversion layer of free carriers at the Si substrate and shorts out neighboring devices. The relatively highly doped Si underneath (the “channel stop”) raises the threshold voltage of this parasitic MOS. If this threshold voltage value is higher than the highest circuit voltage, inversion will not occur.
Comments: Non self-aligned alternative:

Disadvantages:
1. Two lithography steps
2. Channel stop doping not FOX aligned
Self-aligned Source and Drain

* The n+ S/D always follows gate

Perfect Alignment

Off Alignment
Comment: Non self-aligned Alternative

Solution: Use gate overlap to avoid offset error.

Disadvantages: Two lithography steps, excess gate overlap capacitance
Lightly Doped Drain (LDD)

LDD
(1E17-to 1E18/cm3)
Lightly Doped Source/Drain MOSFET (LDD)

The n-pockets (LDD) doped to medium conc (~1E18) are used to smear out the strong E-field between the channel and heavily doped n+ S/D, in order to reduce hot-carrier generation.
LDD Process Flow using Ion Implantation

n implant for LDD

CVD conformal deposition SiO$_2$

Directional RIE of CVD Oxide
Spacer left when CVD SiO$_2$ is just cleared on flat region.

0.25µm

0.05µm

n$^+$ implant

n$^+$
Self-Aligned Silicide Process (SALICIDE) using Ion Implantation and Metal-Si reaction

Metal silicides are metallic.
They lower the sheet resistance of S/D and the poly-gate
SALICIDE Process Flow

oxide spacer

SiO₂

n⁺
Ti deposition

heat treatment (> 700° C)

\[ Ti + 2Si \rightarrow TiSi_2 \]

\( Ti \) will not react with \( SiO_2 \).

Selective etch to remove unreacted Ti only
Salicide Gate TEM
Self-aligned Oxide Gap

DRAM structure (MOSFET with a capacitor)

For a small spacing between poly-I and poly-II, inversion charges between MOSFET and Capacitor are electrically linked. No need for a separate n+ island.
Process Flow of MEMS Rotating Mechanisms

In-Plane Movement

Micro-turbine Engine
Process Flow for a Hinge Structure

Out-of-plane Movement

Poly - 1
Poly - 2
Contact

Silicon
PSG
Poly - 1
PSG
Poly - 2

Staple
Hinge Pin
Plate
Layout of Thermal Bimorph Actuator

(See 143 Lab Manual for details)
After Patterning Poly-Si (Mask #2)

Top View

- Aluminum
- Poly Si
- Oxide
- Si substrate
- Al-Poly contact

Cross Section
After Patterning Intermediate Oxide (Mask #3, Contact-Hole Cut)
After Aluminum patterning (Mask #4)

Top View

Cross Section

Legend:
- Black: Aluminum
- Light Blue: Poly Si
- Yellow: Oxide
- Blue: Si substrate
- Red: Al-Poly contact
After XeF2 selective etching of Si Substrate (Final Structure)
A Generic NMOS Process Flow

Substrate
Boron doped (100)Si
Resistivity= 20 Ω-cm

Thermal Oxidation
~100Å pad oxide

CVD Si₃N₄
~ 0.1 um

Lithography
Pattern Field Oxide Regions

RIE removal of Nitride and pad oxide

Channel Stop Implant:
3x10¹² B/cm²
60keV

Thermal Oxidation
to grow 0.45um oxide

Wet Etch Nitride and pad oxide

Ion Implant for Threshold Voltage control
8x10¹¹ B/cm² 35keV

Thermal Oxidation
To grow 250Å gate oxide

LPCVD Poly-Si
~ 0.35um

Dope Poly-Si to n+
with Phosphorus Diffusion source
A Generic NMOS Process Flow (cont.)

Lithography
Poly-Si
Gate pattern

RIE
Poly-Si
gate

Source /Drain
Implantation
~ $10^{16}$ As/cm$^2$ 80keV

Thermal Oxidation
Grow ~0.1um oxide
on poly-Si
And source/drain

LPCVD
SiO2
~0.35um

Lithography
Contact
Window pattern

RIE removal of
CVD oxide and
thermal oxide

Sputter Deposit
Al metal
~0.7um

Lithography
Al interconnect
pattern

RIE etch of
Al metallization

Sintering at ~400$^\circ$C in H2 ambient
to improve contact resistance
and to reduce oxide interface charge
NMOS Structure

Generic NMOS Process Flow

Boron-doped Si
20 Ω-cm
<100>

active device
~5 μm

p-Si <100>
500 μm
Nitride SiO$_2$

P.R. n$itride$

SiO$_2$

Si

ETCH

DRY ETCH: NITRIDE/PAD OXIDE

ION IMPLANT

CHAN-STOP: $3\times10^{12}$B/cm$^2$, 60keV

B : $3\times10^{12}$ / cm$^2$

60 keV

~0.1µm

$3\times10^{17}$ / cm$^3$
As+ 80keV, $10^{16}$/cm$^2$

Ion Implant:
- Source/Drain: $1 \times 10^{16}$ As/cm$^2$, 80keV

Oxidation:
- Source, Drain, Polysilicon Oxide: 0.1 $\mu$m

Thermal oxide
Al CVD oxide intermediate oxide

n⁺

H₂ anneal ~ 400°C

Si/SiO₂

Interface States Passivation