EE143, S2006 **N.CHEUNG**

Homework Assignment # 12 Solutions

Problem 1

Upon release, the SiO2 layer will expand because it was originally in compressive stress, while the Al layer will contract because it was originally in tensile stress. The cantilever beam will therefore bend **up** at the tip upon release.

As the beam is heated, both the Al and SiO2 layers will expand. Since the coefficient of thermal expansion is much larger for Al (25×10^{-6} /K) than for SiO2 (0.35×10^{-6} /K), the Al layer will expand at a greater rate than the SiO2 layer, so the beam tip will move **downward** until it touches the Si substrate (if it does not fracture first).

Problem 2

(a) $\varepsilon_f = (\alpha_f - \alpha_s)\Delta T = (24.6\text{-}2.6)\times10^{-6}\times100 = 2.2\times10^{-3}$

$\sigma_f = E_f \times \varepsilon_f = 2.2\times10^{-3}\times0.7\times10^{11}$ N/m^2 $= 1.54\times10^{8}$ N/m^2

(b) $t_f = 1\ \mu m = 10^{-6}$ m

$t_s = 50\ \mu m = 5\times10^{-5}$ m

$$r = \frac{E_s \times t_s^2}{(1-\nu)_s \times 6 \times \sigma_f \times t_f} = 0.7 \text{ meters}$$

Problem 3

a) ρ = applied force/unit length = $w \times t \times d \times g$ with density $d = 2.3\times10^3$ kg/m^3

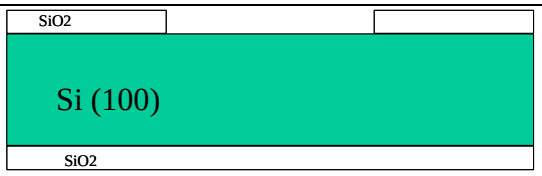
$$Y(\text{at L}) = \frac{3\rho L^4}{2Ewt^3} = \frac{3dgL^4}{2E\,t^2} = 52\text{nm}$$

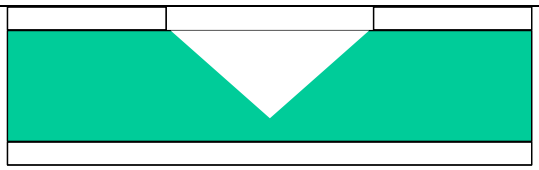
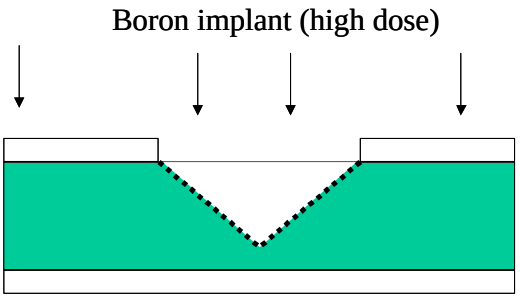
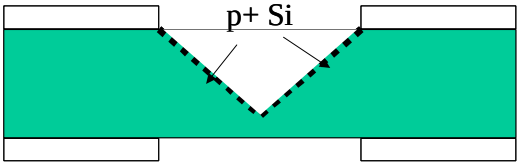
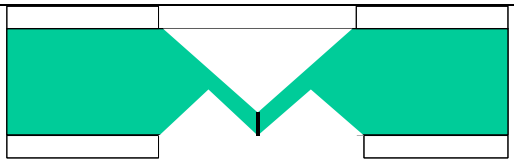
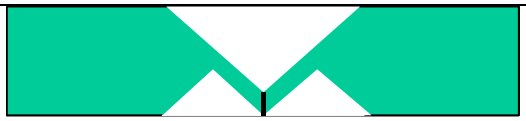
b) $F_o = 0.216 \dfrac{t}{L^2} (E/d)^{1/2} = 3.6$ kHz

c) A 2% increase in density d will increase Y(at L) by 2% and decrease F_o by 1%

d) The 0.52nm change in Y(at L) is difficult to measure using optical means [maybe do-able with atomic force microscopy]. It is probably easier to measure the 16Hz change of resonant frequency electrically.

Problem 4

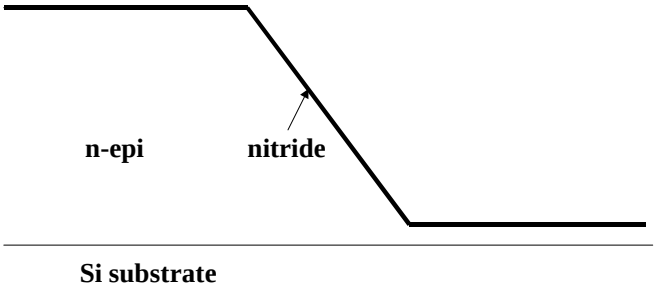
1) Grow thermal oxide on both sides of Si(100) wafer	

2) Pattern oxide opening on top oxide and KOH etch of Si to bottom of wafer	
3) Boron implant (high dose) and activate doping (with drive-in) to form p+ Si on sidewalls	
4) Pattern bottom oxide.	
5) KOH etch Si. For the top side, the p+ layer will act as an etch stop. For the bottom side, etching will proceed but etching rate will slow down when approaching the p+ junction depth . A slit will form at the bottom because (1) this part is exposed to the etching solution for the longest time , and (2) this part has the lowest boron concentration with the implant and drive-in process.	
6) Strip oxide	

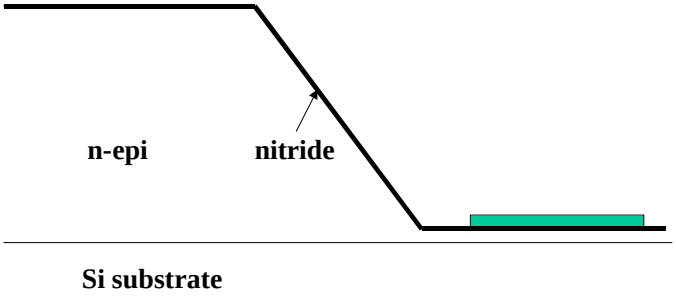
Problem 5

This structure is a **MEMS-before-CMOS** process. The key idea is to etch the recessed area first, followed by typical poly MEMS process. The surface is planarized with CMP, and continued with standard CMOS process. After completion, the MEMS part is released by selectively etching of the scarificial oxide. The following process flow is just one example. There can be several variations which can accomplish the final structure.

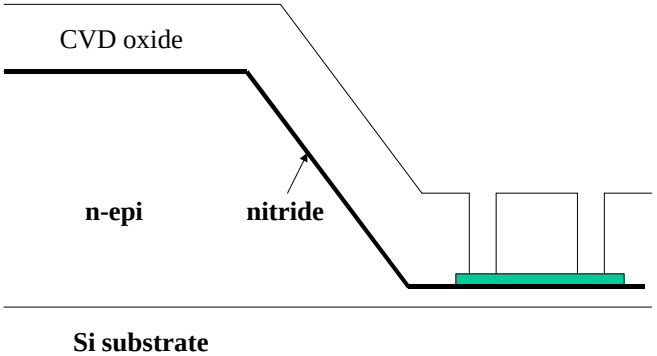
Starting material : n-epi on Si. **Pattern MEMS area**, use KOH to etch into epi Si, leaving tapered slope. CVD silicn nitride



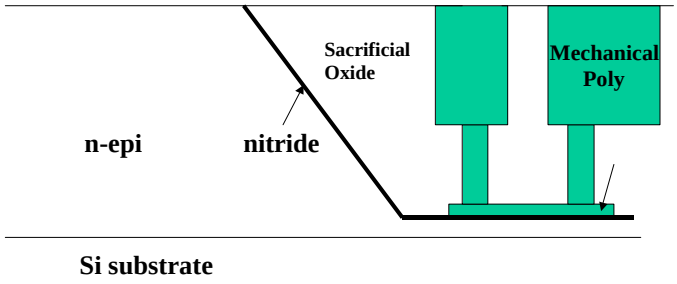
CVD base polysilicon, **pattern base poly**



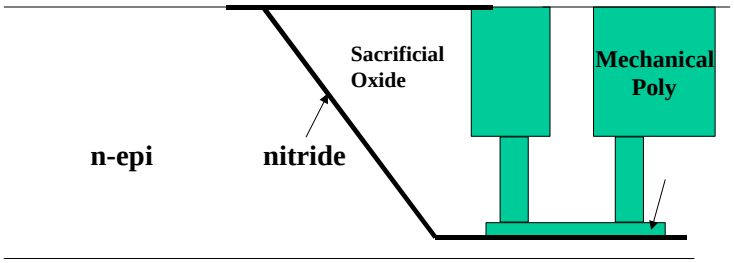
CVD sacrificial oxide 1 , **pattern contact hole** to sacrificial oxide 1.



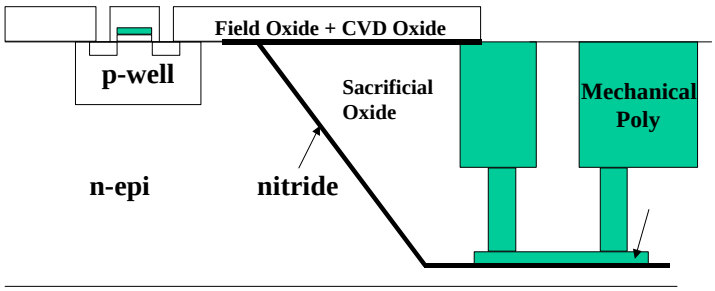
CVD mechanical poly which can also fill up contact hole.Pattern mechanical poly .CVD sacrificial oxide 2 over mechanical poly. CMP whole structure till planarized



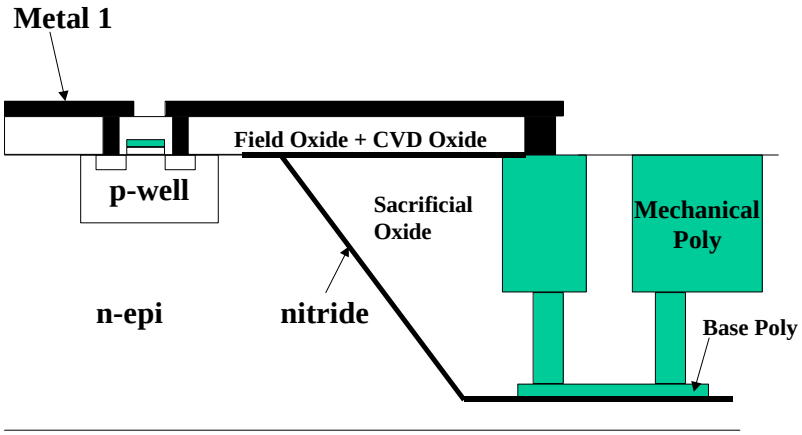
CVD thin nitride and pattern over the n-epi and MEMS poly. This nitride is to protect Field Oxide from etching during MEMS release.



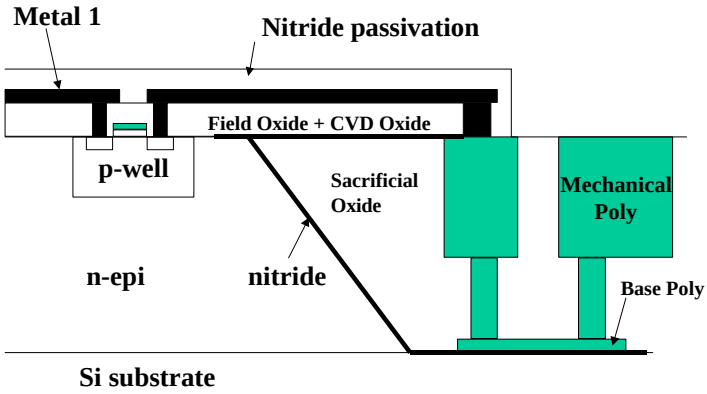
The following is an example CMOS process (variations are possible):
Pattern well, p-well implant and drive-in
Field oxidation (masking step here)
Gate oxidation
Poly gate deposition and patterning
n+ S/D implant
Protect NMOS (masking step here), p+ S/D implant for PMOS
CVD oxide .Open contact holes to CVD oxide



Metal 1 deposition and pattern Metal 1



CVD nitride layer for deposition. Pattern nitride openings



Selectively etch sacrificial oxide in MEMS area to release poly structures