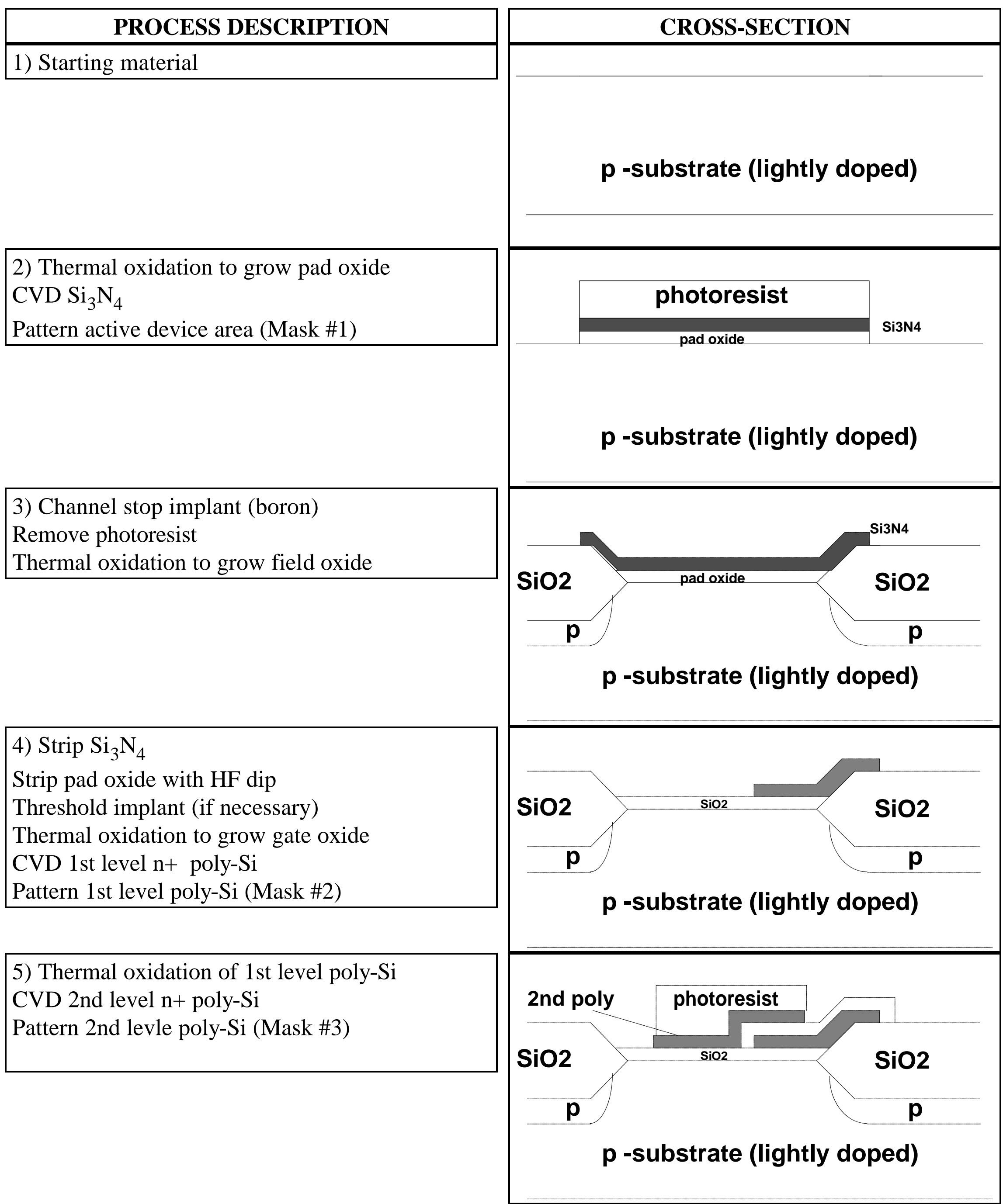
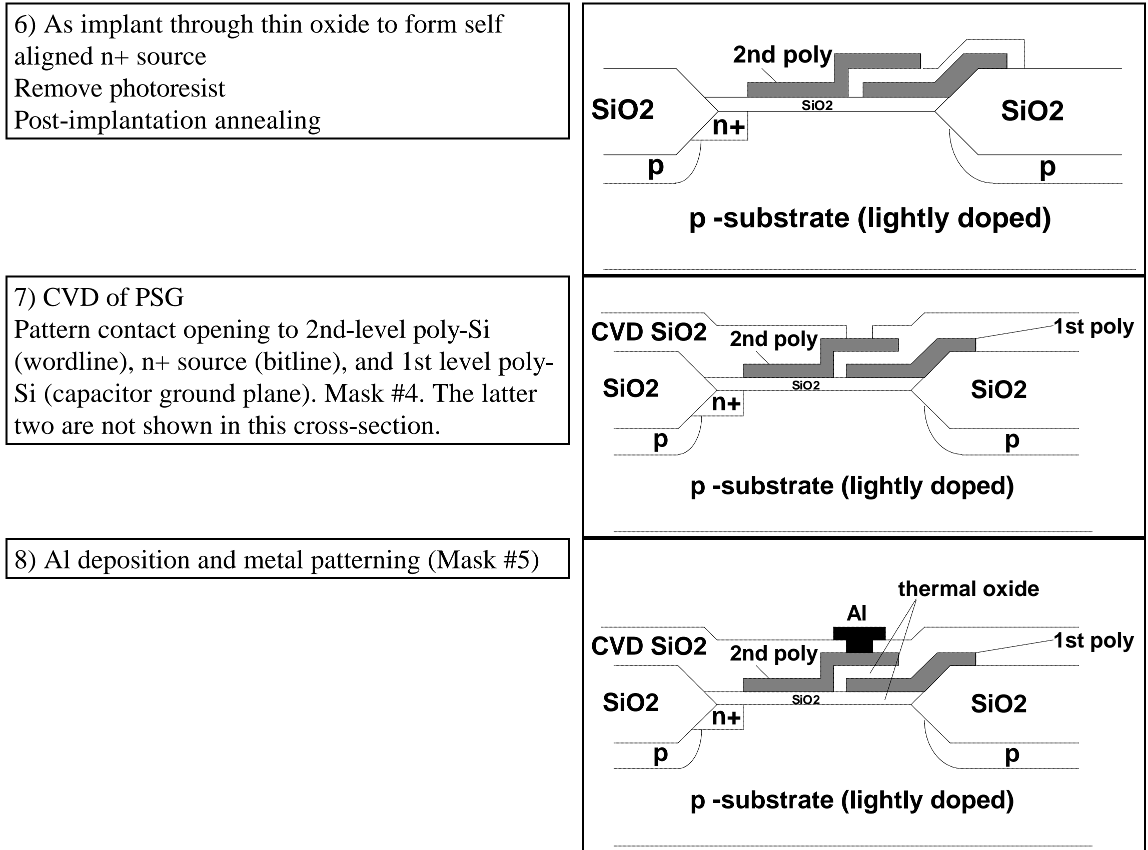
**EE143 Sp2006**

**Homework Assignment #10 Solutions**

* It is understood photoresist has to be removed prior to high-temperature processing steps. This is stated explicitly in the process flow only if the photoresist is used as an implantation mask.

**Problem 1**

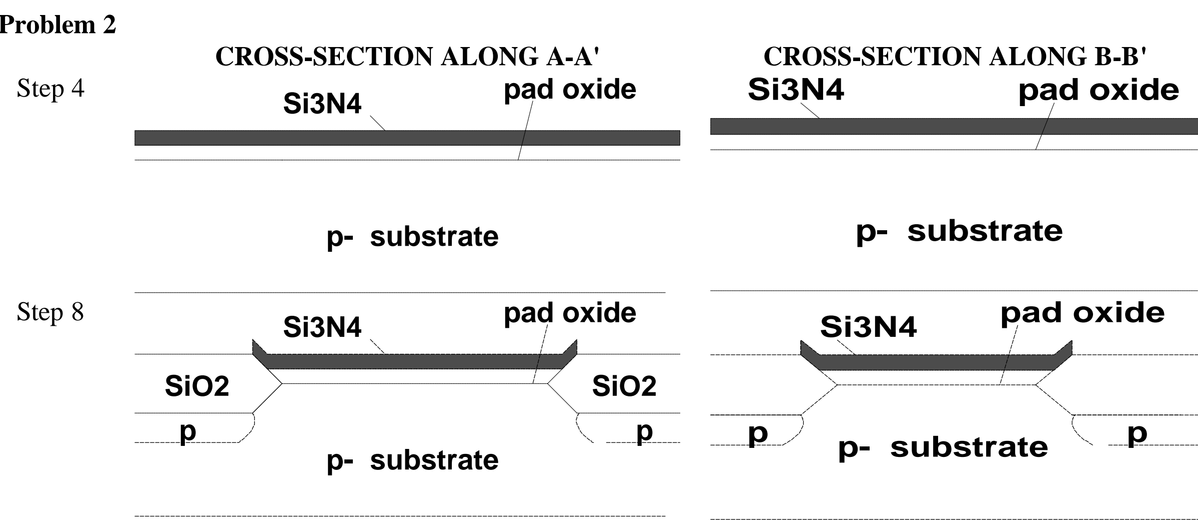


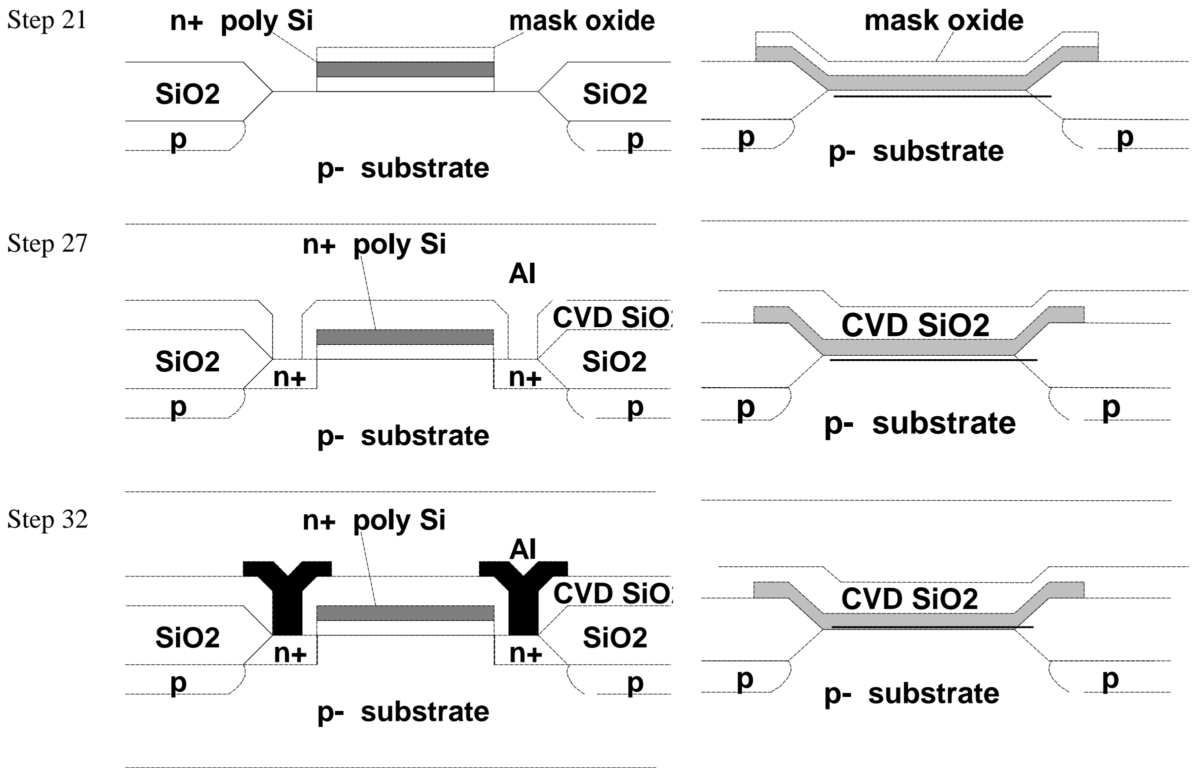



**Comments**

It is extremely difficult to pattern the narrow spacing (<30nm) using lithography because of alignment error and minimum resolution issues. This example use the controllable thermal oxididation process to fabricate this gap spacing.

**Problem 2**

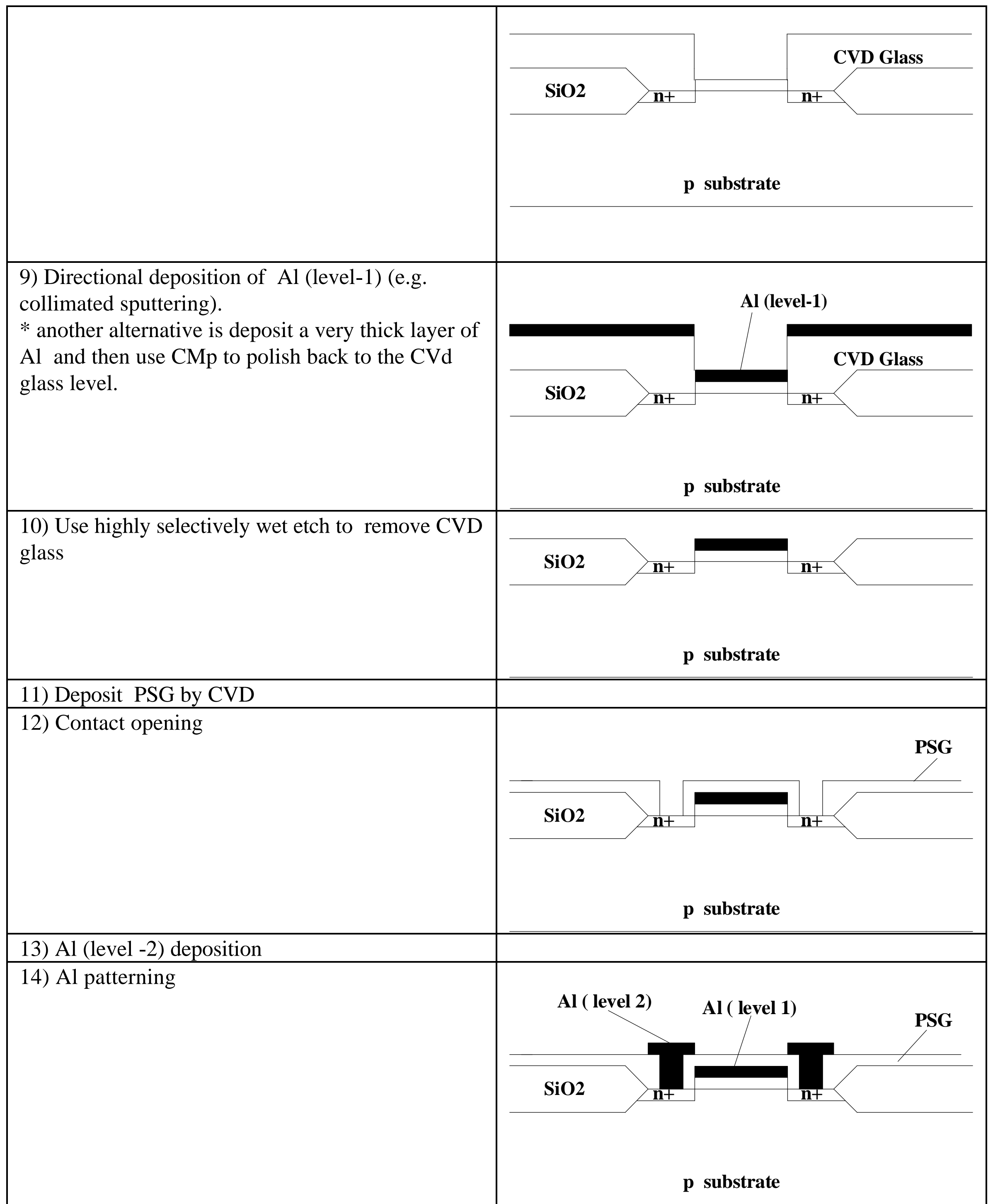





**Problem 3**

The following is a solution based on a "**dummy gate**" concept. Other variations are possible.

| Staring material: p-Si | |
|---|---|
| 1) LOCOS | |
| 2) Deposit 0.5 µm poly-Si or other high-melting point material (e.g. $Si_3N_4$ ,silicides etc) | |
| 3) Pattern poly-Si to gate dimension | |
| 4) Blanket As implantation. Post-implantation annealing | poly-Si<br>SiO2<br>n+<br>n+<br>p substrate |
| 5) Deposit spin-on-glass or PSG to planarize surface | |
| 6) Etch back to top of poly-Si | poly-Si<br>CVD Glass<br>SiO2<br>n+<br>n+<br>p substrate |
| 7) Selectively etch poly-Si | |
| 8) Grow gate oxide | |




| Step | |
|---|---|
| | |
| 9) Directional deposition of Al (level-1) (e.g. collimated sputtering).<br>* another alternative is deposit a very thick layer of Al and then use CMp to polish back to the CVd glass level. | |
| 10) Use highly selectively wet etch to remove CVD glass | |
| 11) Deposit PSG by CVD | |
| 12) Contact opening | |
| 13) Al (level -2) deposition | |
| 14) Al patterning | |

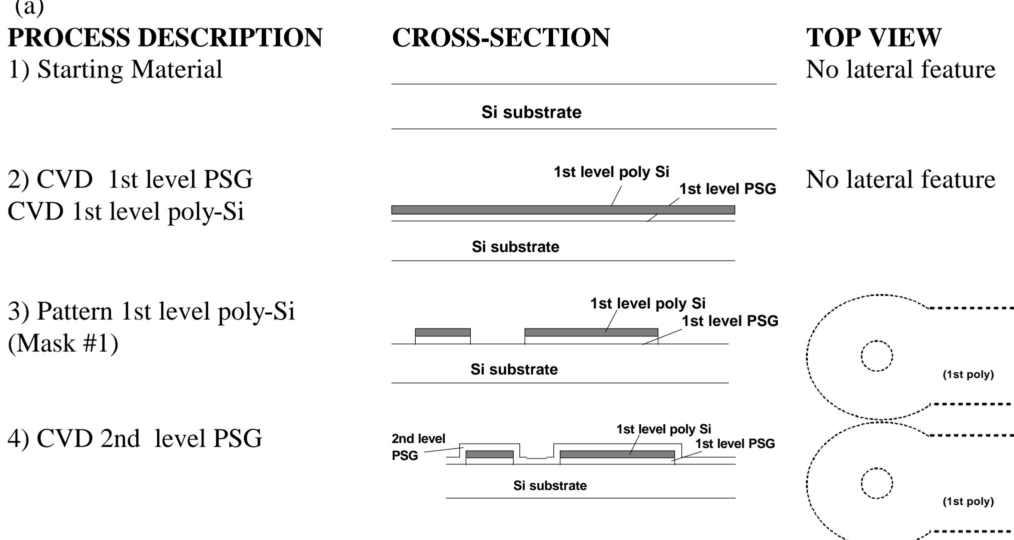
**[Comment]** If implantation is not required, we can also for the self-aligned S/D by diffusion. the following is an alternative :

| Use n+ PSG as doping source to form source/drain | |
|---|---|

| | |
|---|---|
| | n+ CVD Glass<br>SiO2<br>n+<br>n+<br>p substrate |
| Gate oxide growth | CVD Glass<br>SiO2<br>n+<br>n+<br>p substrate |
| Directional Al gate deposition (e.g. collimated sputtering) | Al (level-1)<br>CVD Glass<br>SiO2<br>n+<br>n+<br>p substrate |
| Strip PSG | |
| .... continue as above process | |
| | |

**Problem 4**

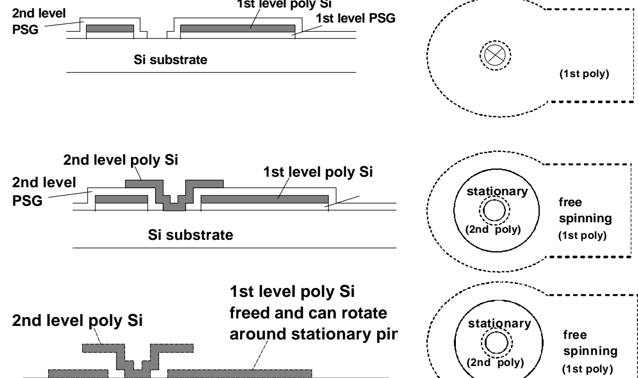
(a)



5) Pattern opening for fixed pin (Mask #2)

6)
CVD 2nd level poly-Si
Pattern 2nd level poly-Si (Mask #3)

7) Selectively etch away 1st level and 2nd level PSG with HF. Final Structure

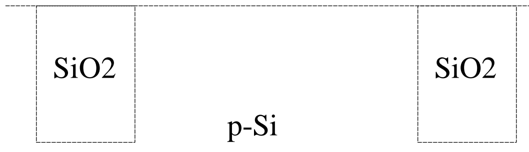



(b) (I) If photoresist is used to replace poly-1 as the rotor material, it cannot withstand the processing temperature (300-600 $^oC$)of the subsequent CVD steps.

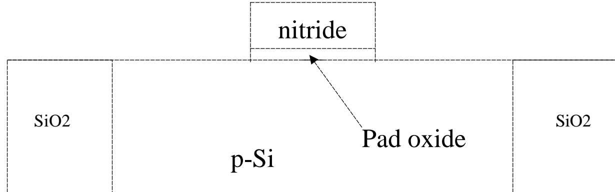
(II) **In principle , yes.**
Thermal oxide will be grown conformally on all surfaces and sidewalls of the poly-1 rotor and the open hole of the Si susbstrate. After fix pin contact opening, poly-2 deposition and patterning, HF can still penetrate all sacrificial oxides (thermal oxide and PSG) surrounding the poly-1 rotor and release it.
**In practice, not a desirable process**.
Thermal oxide growth rate is too slow and requires a high temperature. The oxide grown will also consume poly-Si. Thickness of poly-Si will be reduced and final dimension of the rotor inner hole will be distorted (larger). Uneven poly-Si oxidation rates along grain boundaries may leave a rougher edge which may increase the friction between rotor and pin.

(III) **NO with the present process methodology**.
The top of the pin has to be larger than the inner hole of the rotor to keep the rotor from falling off the wafer. The pin dimension has to be patterned with a separate lithography step.
[ Comment: If one opens a hole in PSG-1 , deposit poly-1, and pattern poly-1 for both rotor and pin with same lithography step, the pin and rotor will not be connected. However, the rotor will fall out of the wafer after etching the sacrificial oxide.]

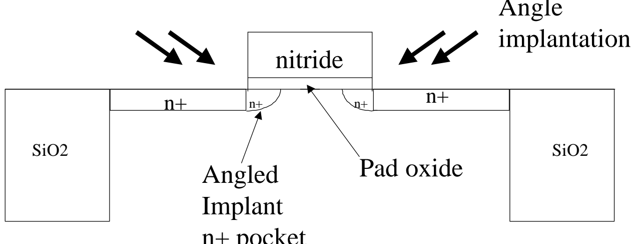
**Problem 5**
1) Starting structure ( oxide trench isolation)



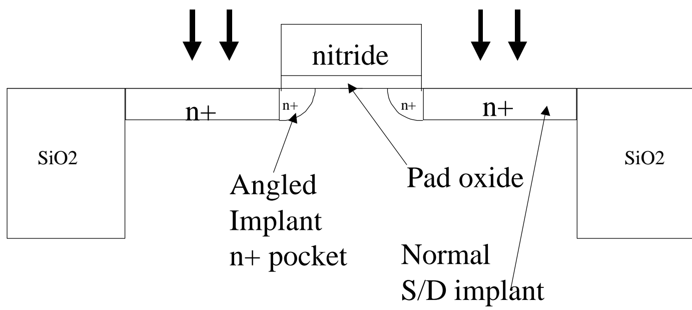

2) Pad oxide growth. CVD nitride.
Pattern to smallest feature allowed by Optical lithography. Etch stack.



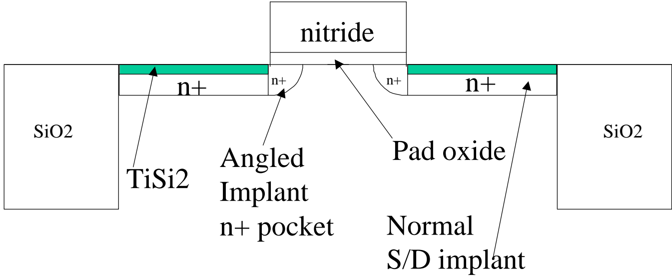

3) Angle implant of As to form
n+ pockets.



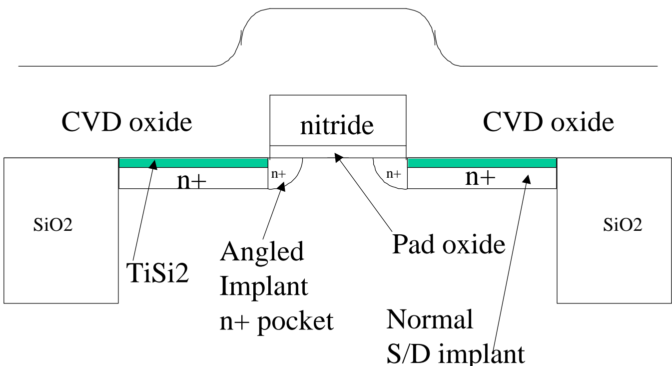

4) Vertical implant of As to form normal S/D



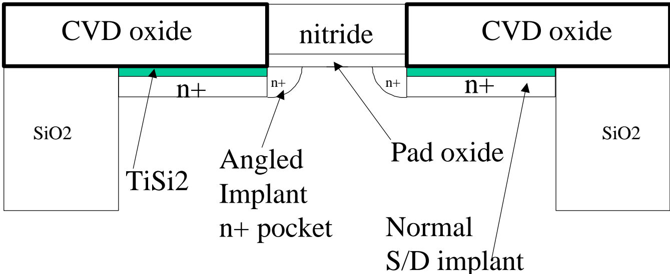

5) Blanket deposition of pure Ti.
Anneal at 750C to form $TiSi_2$.
Remove unreacted Ti on oxide and nitride.
Additional anneal (900C)
to activate S/D implant.



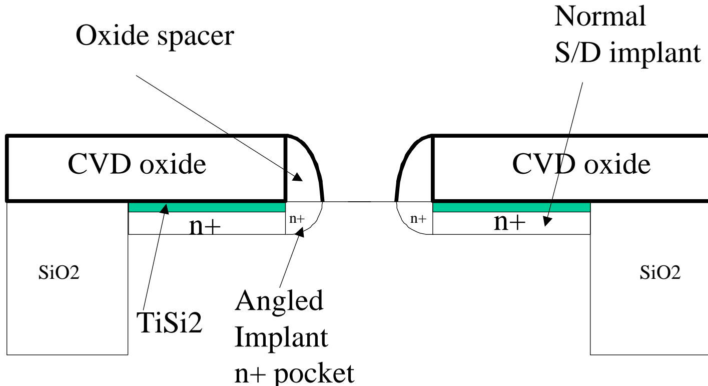

6) Blanket CVD oxide



7) Planarize structure to nitride surface with CMP.




8) Selective etch of nitride.
Slight dip in HF to remove pad oxide.
Blanket CVD oxide.
Use anisotropic RIE to form oxide spacer.




9) Grow thermal gate oxide.
Deposit doped poly-Si by CVD
Pattern poly-Gate.