EE143 **S2006**

Homework Assignment # 9 (Due April 6, 8am)

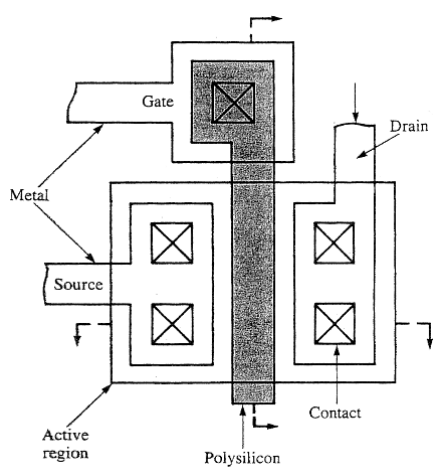
Week of 3/27 is Spring Recess
Midterm Exam #2 will be on April 5 (Wed) 6:00-7:30pm, GPB Room 100, closed book exam, 8 sheets of handwritten notes allowed. Topics of HW#1-HW#8 will be included.

Reading Assignment
1)Jaeger, pp.212-221
2)Summary sheet of EE143 layout rules (attached)
3) EE143 Reader ("Design Rule Basics" from *Physical Design of CMOS IC Using L-Edit*, J.P. Uyemura). This general reading provides bakground info on why different rules are needed.

Read here before you start your homework :
The layout schematics shown below are not to scale. The exact layout may depend on the constraints imposed by the design rules. You have to do all layouts with a scale of **0.2" to 1**l**.** A graph paper with such a scale is attached is also posted on the web. You can photocopy/print it for your homework problems. ***The reader will not grade any homework turned in with other arbitrary scales. You have to draw the layout and specify which design rules are used. If you wish, you can also use color pencils to distinguish the different boundaries.***
Suggestions: Start wih a smallest feature first (e.g. contact hole, poly-Gate length) and then sketch outward.
Note: 1) Active device region is also called Thin oxide region; 2) The S/D area is also called the diffusion region although it is doped by ion implantation.

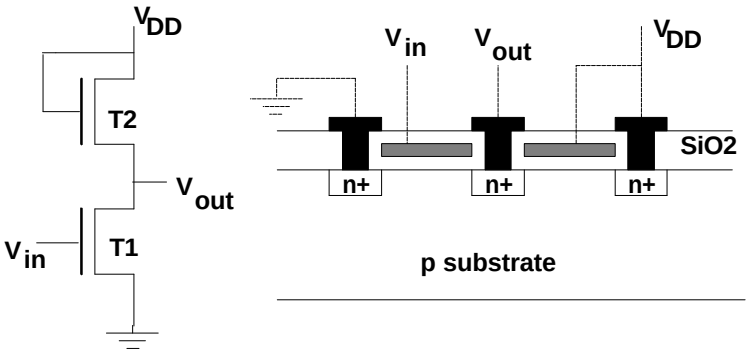
Problem 1 MOS Transistor – a warmup exercise

Your textbook shows the schematic layout of a MOSFET (not drawn to scale) with two contact holes for the source/drain. Use our EE143 layout design rules to do a **minimum** geometry layout which can accommodate **two** contact holes for the source and the drain.
Given: The transistor channel length L = 4 l ***and channel width W =8*** l

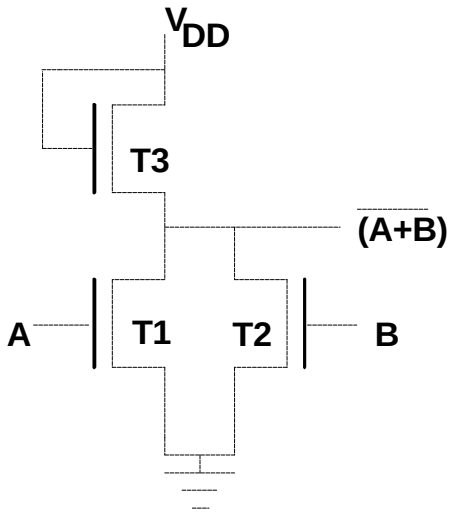


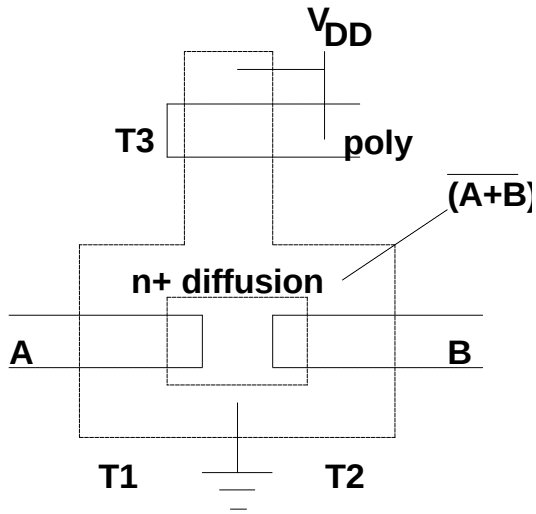
Problem 2 NMOS Inverter
Layout a minimum geometry NMOS (poly-gate) inverter with the EE143 design rules in the graph paper provided. The circuit diagram and the schematic cross-section are shown below. V_{in}, V_{out} and V_{DD} are the

input voltage line, output voltage line, and supply voltage line respectively. All interconnects are aluminum lines.
Both transistors have W=4 μm (2λ) and L=4 μm (2λ). The poly-gate of transistor T2 is electrically connected to its drain with an aluminum line.Dash lines indicate contact cut to the poly-Si is to the



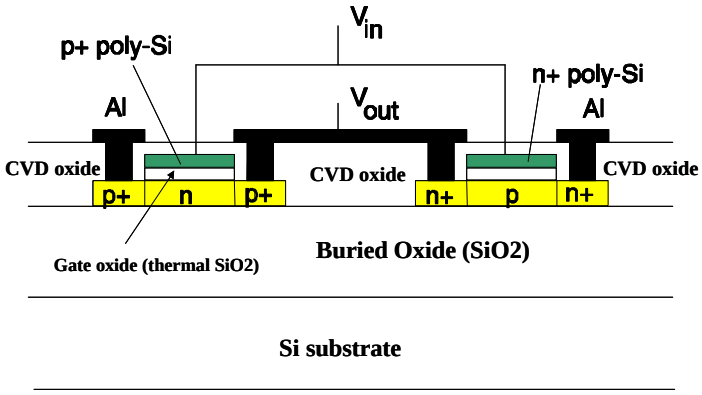
Problem 3 NOR Gate
Use our EECS143 design rules to draw a minimum-geometry two-input NMOS NOR gate using poly-Si gate transistors. V_{DD} is connected to the gate of T3 with Al line. To conserve space and to minimize the number of contact holes, the n+ diffusion regions are merged wherever possible.
GIVEN : T1 and T2 : W/L = 10 μm / 4μm ; T3: W/L = 4 μm / 10μm . To help you started , an unfinished (not-to-scale) sketch of the top-view is provided. Any reasonable deviation from this sketch is acceptable. Draw the composite layout (including metal lines) and state the design rule used.





Problem 4 How design rules can be changed

The following cross-section shows a CMOS inverter fabricated with silicon-on-insulator (SOI) technology. Note that the buried oxide (SiO2) is a perfect electrical insulator. If we choose to use this technology. Explain how **three** of our EE143 MOS layout design rules can be changed (i.e., larger or smaller). Justify your explanations.



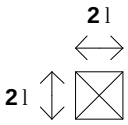
EE143 Standard Layout symbols and Design Rules for MOS

1. Background

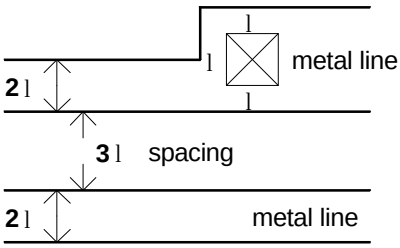
1.1 Lithography/etching limit on minimum feature or spacing = 2λ
1.2 Alignment limit (overlay accuracy) = λ
1.3 Unless specified, default value: λ = 2 μm

2. Symbols and Rules

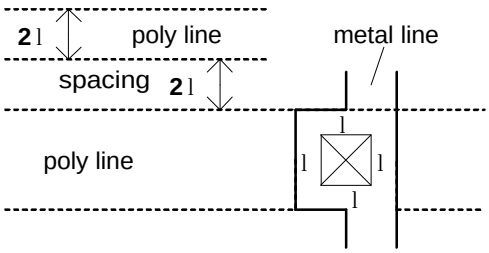
2.1 Contacts (metal to silicon)
minimum size 2λ x 2λ



2.2 Metal
minimum width: 2λ
minimum spacing: 3λ
minimum underlap of contact: λ



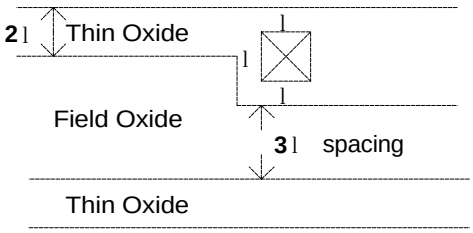
2.3 Polysilicon
minimum width: 2λ
minimum spacing: 2λ
minimum underlap of contact: λ



3. MOS Devices

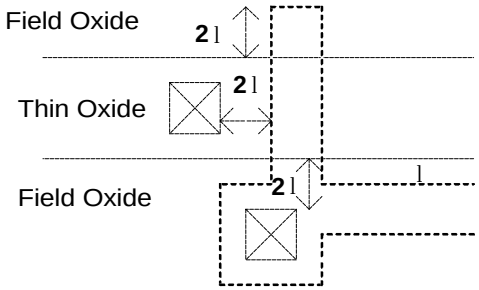
3.1 Thin oxide of MOS
minimum width: 2λ
minimum space: 3λ
minimum underlap of contact: λ

[The thin oxide region is also known as diffusion region. The field oxide region is also called the thick oxide region]



3.2 Si Gate of MOS

Minimum gate overlap of field =2λ
Minimum contact to gate spacing =2λ
Contacts to polysilicon allowed on thick oxide only. Minimum spacing to thin oxide = 2λ
Minimum poly to thin oxide spacing = λ



Graph paper for EE143 Layout problems