Problem 1

[1] Minimum size contact = 2\(\lambda\) x 2\(\lambda\)
[2] Minimum contact-contact spacing (lithography limit) = 2\(\lambda\)
[3] Minimum thin-oxide-region underlap of contact = \(\lambda\)
[4] Minimum source/drain contact to gate spacing = 2\(\lambda\)
[5] Minimum poly-Si width (L) = 4\(\lambda\) [This is given]
[6] Minimum gate overlap of field-oxide region = 2\(\lambda\)
[7] Minimum metal-metal spacing = 3\(\lambda\)
[8] Minimum metal overlap of contact = \(\lambda\)
[9] Minimum metal width (lithography limit) = 2\(\lambda\)
1. Min contact hole = $2\lambda$
2. Min contact overlap = $\lambda$
3. Min contact to gate = $2\lambda$
4. Min gate length = $2\lambda$
5. Min gate width = $2\lambda$
6. Min gate overlap of field oxide = $2\lambda$
7. Min poly to diffusion = $\lambda$
8. Min poly contact to thin oxide = $2\lambda$
9. Min metal to metal = $3\lambda$
1. poly-poly spacing = $2\lambda$
2. gate overlap of thick oxide = $2\lambda$
3. poly-thin oxide spacing = $\lambda$
4. min feature = $2\lambda$
5. contact underlap = $\lambda$
6. metal overlap contact = $\lambda$
7. poly contact to thin oxide = $2\lambda$
8. min metal-metal spacing = $5\lambda$
Problem 4

The following changes are possible. There can be other acceptable changes.

Rule 1  Min thin-oxide to thin-oxide spacing can be reduced because the substrate is electrically insulating SiO2. No field oxide is required for device isolation.

Rule 2  Minimum underlap of contact in thin oxide can be reduced because the substrate is insulating. Misalignment of the contact hole will not create an ohmic shorting path to the buried oxide substrate. [Note: For the case of a p-type Si substrate, Al touching p-Si will create a Schottky ohmic contact.]

Rule 3  Minimum metal - metal spacing can be reduced. The wafer surface topography is flatter. There is no thick LOCOS field oxide and the MOS islands can be made very thin.