Homework Assignment # 8 Solutions

Problem 1 Simple resistance and capacitance calculations

(a) $R_S = \rho / t = 3.2 \times 10^{-6}\ \Omega\text{-cm} / 10^{-4}\text{cm} = 0.032\ \Omega$ /square

(b) $R = R_S (L/W) = 0.032 \times 50 = 1.6\ \Omega$

(c) $C_{ox} = 3.9 \times 8.854 \times 10^{-14} / 10^{-4} = 3.5 \times 10^{-9}$ F/ cm^2

$C = C_{ox}(WL) = 3.5 \times 10^{-9}$ F/cm$^2 \times 0.05\text{cm} \times 0.001\text{cm} = 0.175$ pF

(d) $RC = 1.6 \times (0.175 \times 10^{-12}) = 0.28$ psec.

(e) RC = 0.28 psec/3.9 = 0.07 psec.

Problem 2 Electromigration failure

(a) $MTF_2 / MTF_1 = \exp [-0.5\text{eV} / k) (1/T_2 - 1/T_1)$

For $T_2 = 300$K and $T_1 = 400$K, the ratio is about 125.

Note: MTF of electromigration failure degrades rapidly with elevated operating temperature.

(b) I (max) = cross-sectional area x J (max) = 10^{-4} cm x 10^{-4} cm x 5 x 10^5A/cm^2

= 5 mA.

Comment: With future scaling of device dimensions, interconnect width has to scaled also to maintain the same pitch. Height of interconnect will also be reduced to maintain a reasonable aspect ratio from thin-film deposition and etching considerations. With a design rule of J(max) ~ 5E5A/cm^2, I(max) will be limited to 1mA per interconnect if the cross-sectional area is reduced to 0.5 um^2. However, circuit designers would like to keep I(max) as high as possible for high-speed operations.

Problem 3

(a)Hillock and void formation. Electron flux will transfer momentum to interconnect lattice atoms, creating atomic motions along direction of electron low. When there is a local divergence of the atomic flux (e.g. unequal grain boundary diffusion paths) , mass accumulation (formation of hillocks) or mass depletion (formation of voids) can occur. There can lead to shorting of neighboring interconnects or complete open of an interconnect. The common practice to improve interconnect reliability is to create alloying precipitates (e.g. Al-Cu) along the grain boundaries which block grain boundary diffusion.

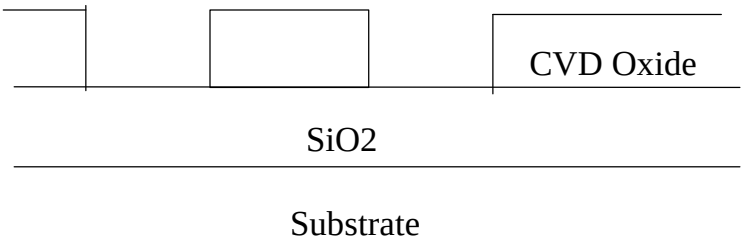
(b) Aluminum spiking. A sintering step around 400-450 ^{o}C in a forming gas ambient is used after metallization (to ensure better metal-Si contact and also to reduce Si/SiO2 interface states) . Substrate Si atoms dissolved in Al during sintering step, leaving voids behind. Al diffuses in to fill up the void, forming spiking. Solution is to saturate the Al with ~2% Si as the metal material.

(c) Step Coverage. Al or alloys are usually deposited by sputtering. Due to self-shadowing and geometrical shadowing, sidewalls and corner of steps will receive less flux, creating thinner deposition at sidewall and bottom corners. Solutions to minimize step coverage is to use a higher substrate temperature to enhance surface diffusion during Al deposition , or tilt and rotate substarte during deposition. A better approach is to use a W-plug (deposited by CVD) to fill up the contact hole before Al deposition.

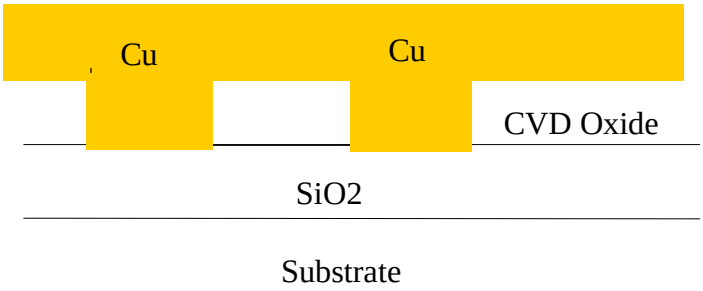
Problem 4

1) Starting material : Oxide on Si substrate

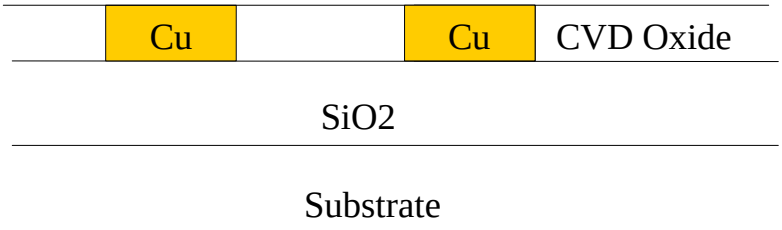
2) Deposit CVD oxide, pattern oxide trenches (RIE for vertical sidewalls)



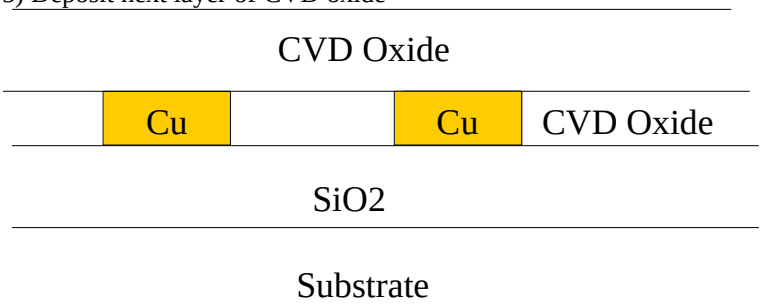
3) Deposit Cu by platimg or CVD



4) Planarize Cu surface by CMP



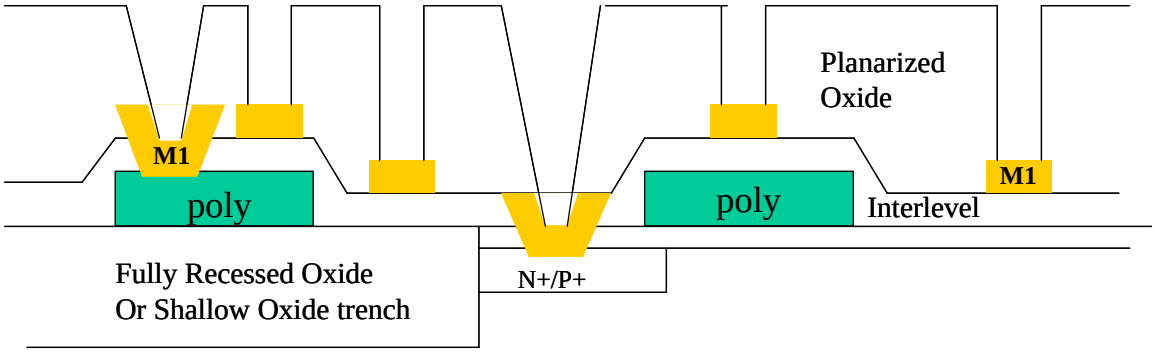
5) Deposit next layer of CVD oxide



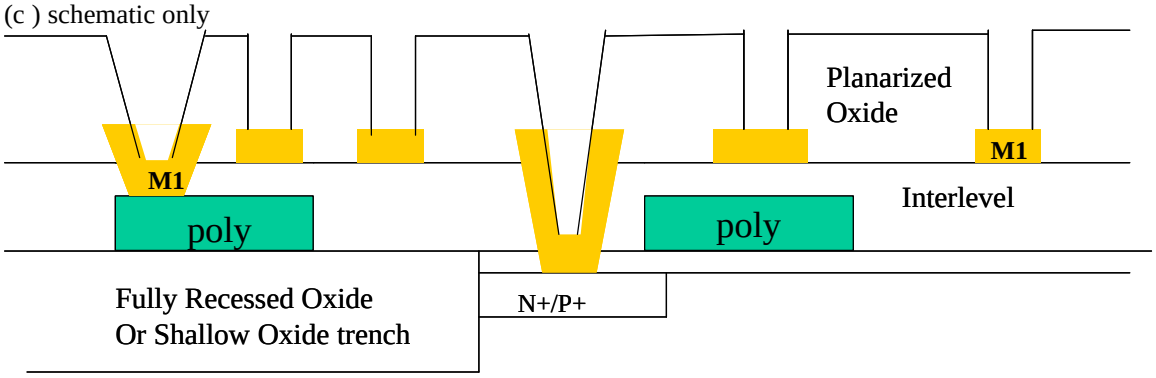
Problem 5

(a) The contact holes will have different depths to reach from planarized surface to M1 surface. We need very highly selectivity between metal and oxide etch to avoid excessive M1 etching. We also need very high degree of anisotropy for oxide etch to ensure consistent contact hole area on M1 surface.

(b) schematic only



(c) schematic only



(d) schematic only