Homework Assignment # 1 Solutions

Problem 1 Processing Module Terminologies

(a)

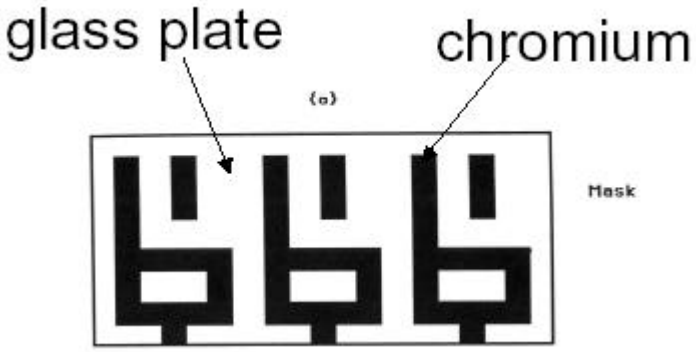
"Growing" an oxide layer: Thermal oxidation is used to form SiO_2 by reacting the Si substrate atoms with oxygen or steam. Si substrate atoms will be consumed using this process.

"Depositing" an oxide: The SiO_2 material is deposited from external sources (e.g. by chemical vapor deposition or sputtering deposition methods). No Si substrate atoms will be consumed to form the SiO2.

(b)

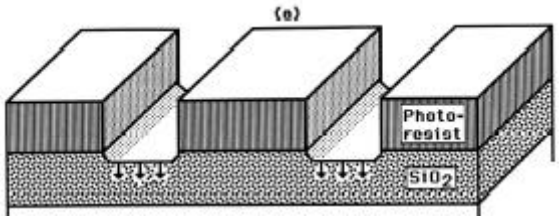
(i) What is a photomask?

The glass plate with chromium patterns used in optical lithography. Chrome regions will block out the light and will not expose the photoresist.



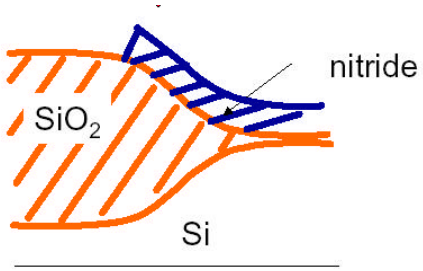
(ii) What is an etching mask ? Quote one example.

Patterns of materials on the wafer which protects the regions underneath from being etched. Example: photoresist patterns on an oxide layer.



(iii) What is an oxidation mask? Quote one example.

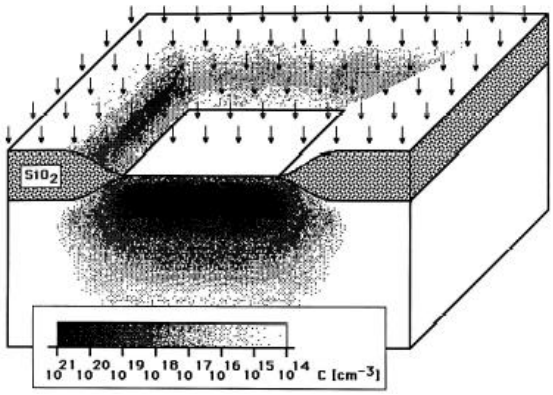
Patterns of materials on the wafer which protects the regions underneath from being oxidized during a thermal oxidation step. Example: Si_3N_4 patterns on top of Si wafer



(iv) What is an implantation mask? Quote one example.

Patterns of materials on the wafer with sufficient physical thickness to block the penetration of ions during the implantation step.

Example: Thick photoresist or thick oxide patterns on top of wafer.



Problem 2

1) A total of 4 lithography steps are used in this Al-gate process

Mask 1 . Pattern thick oxide to define the source/drain area
Mask 2 Pattern gate area
Mask 3 Pattern contact holes for Al contact to source/drain
Mask 4 Pattern Al interconnects

2) The photoresist cannot withstand processing temperature higher than ~180^{o}C .Photoresist patterns will be distorted by reflow at moderate temperature and the resist material will be carbonized at high temperature. Because the source/drain diffusion step is at ~ 1000 ^{o}C, photoresist has to be stripped prior to the diffusion step.

Problem 3

(i) **Three lithography steps** are used in this process flow.
Mask 1: Pattern Poly-1 hinge plate
Mask 2: Pattern the staple anchor openings through bottom PSG
Mask 3: Pattern the Poly-2 staple

(ii) **Four CVD steps** are used:
CVD1- bottom PSG deposition
CVD2- poly-1 deposition
CVD3- top PSG deposition
CVD4- poly-2 deposition

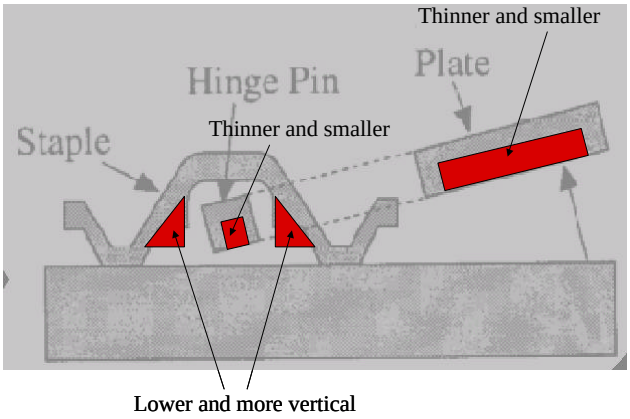
(iii) **Four thin-film etching steps** are used:
Etch 1: Etch Poly-1(hinge plate)
Etch 2: Etch staple anchor openings through bottom PSG
Etch 3: Etch Poly-2 (staple)
Etch 4: Etch all PSG sacrificial layers to release hinge

(iv) NO. Part of the hinge structure is **underneath** the staple structure. If staple is formed first, there is no way to pattern the hinge outline (litho and etch) AND no way to deposit the part of poly-1 which is underneath the staple structure.

(v) AGREE. There is no high-temperature processing steps used after Al deposition, Al melting is a non-issue.
[Optional answer: DISAGREE. One has to find a proper wet/plasma etching recipe with the right selectivity to etch PSG without attacking Al.]

(vi) Major differences (schematic shown below: red is structure using poly-1 oxidation) :

(1) poly-1 plate thinner (poly-Si is consumed during thermal oxidation)
(2) cross-section of poly-1 under staple area is smaller (affects poly-1 & poly-2 gap spacing under staple)
(3) staple cross-section has more vertical sidewalls because there is no PSG (layer 1).



Problem 4

Mobility values are taken from curve reading, your numerical answers may vary slightly from this solution.

(a) The original Si crystal is n-type with an electron concentration of $\approx 2\times 10^{17}/cm^3$. We can safety claim "≈" because n_i ($\sim 1.5\times 10^{10}/cm^3$) is << the net dopant concentration ($|N_A-N_D|$) .

After adding the second impurity, the hole concentration p is $2 \times 10^{17}/cm^3$.

From $np = n_i^2$, $n = 2.25\times 10^{20} / 2\times 10^{17} = 1.13\times 10^3/cm^3$

Since p >> n, the Si is p-type (holes being the majority carrier.) with the **minority carrier being electrons [concentration = $1.13 \times 10^3/cm^3$]**

(b) Boron is a p-type dopant (acceptor) while arsenic is an n-type dopant (donor) . So the second **impurity added is boron.**

Since $p \approx [N_A - N_D] = 2 \times 10^{17}$, N_A (Boron) = $2 \times 10^{17} + 2 \times 10^{17} =$ **$4 \times 10^{17}/cm^3$**.

(b) $n \approx [N_D - N_A] = 10^{18}$ (As) + 2×10^{17} (P) - 4×10^{17} (B) = 8×10^{17} /cm3

For a **TOTAL** impurity concentration = 10^{18} (As) + 4×10^{17} (B) + 2×10^{17} (P) = $1.6 \times 10^{18}/cm^3$, the electron mobility μ_n from the electron mobility curve is ~ 250 cm^2/volt-sec.

Resistivity = $1/ (q \times n \times \mu_n) = 1/ (1.6 \times 10^{-19} \times 8 \times 10^{17} \times 250) =$ **0.03 ohm-cm**

Problem 5

Mobility values are taken from curve reading, your numerical answers may vary slightly from this solution.

(a) The p-type bulk is isolated from the top layer by the PN junction, thus it gives no contribution to the sheet resistance measured by the four-point probe method.

For the top doping layer, **TOTAL** impurity concentration = 2 x 10^{17} (B) + 3× 10^{17} (As) = 5 ×10^{17}/cm^3, Electron concentration $n \approx [N_D - N_A] = 1 \times 10^{17}$, the electron mobility μ_n from the electron mobility curve is ~350 cm^2/volt-sec.

Resistivity ρ of top layer = $1/(q \times n \times \mu_n) = 1/(1.6 \times 10^{-19} \times 1 \times 10^{17} \times 350)$ = 0.179 ohm-cm

R_S (top) = ρ / thickness = 0.179 ohm-cm / 2×10^{-4} cm = **895 ohm/square**

(b) The layout have 10um/2 um + 8um/2 um = 9 squares PLUS 1 corner square.
Therefore total layout has 9.6 squares
Resistance = R_S ´ 9.6 ~ 8592 ohm.