1. **Lab2**
   a) Run through lab 2 and answer all the questions as the first problem for this homework (all questions are prefixed by a “Q:”). There are 5 questions.

2. **Delays**
   Consider an inverter driving a capacitive load in 28nm bulk-CMOS technology.

   All transistors are minimum length and $W_n = 0.5\mu m$, $W_p = 1\mu m$, $V_{DD} = 1V$. In this technology, $C_g = C_d = 2fF/\mu m$, transistor thresholds are 0.25V and fanout-of-4 inverter delay is 15ps.

   a) For what range of sizes of the load capacitor, $C_L$, adding another inverter to drive the load reduces the delay?

   b) If the input capacitance of the first inverter in figure below is set to $C_1 = 3fF$, the wire capacitance $C_w$ is 6fF, how would you size the second inverter that is driving 13.5fF load to minimize the overall delay from In to Out? Is this result intuitive?

3. **Latch Timing**
   A timing path with a single register driving a latch-based system is shown in Figure 2. R0 is a rising-edge triggered register, while R1, R2, and R3 are level sensitive. There are two 50% duty cycle clock phases available, with clkb offset from clk by half a period. Both registers and latches have zero hold time, and there is no clock skew in the system. Registers have $t_{clk-Q} = 100$ ps. Latches have $t_{clk-Q} = t_{D-Q} = t_{su} = 100$ ps.
a) The critical path of S1 is 400 ps, the critical path of S2 is 500 ps, and the critical path of S3 is 1.3 ns. Compute the minimum clock period.

b) Assume that we can model the on current with $I_{on} = K(V_{DD} - V_{thz})$, with $K = 0.002$, $V_{DD} = 1$ V, and $V_{thz} = 0.25$ V. There is a systematic variation on $V_{thz}$. What is the maximum value of $V_{thz}$ that only leads to a 10% increase in delay?

c) The systematic variation of $V_{thz}$ is normally distributed with $\sigma = 0.03$ V. What would be the yield in terms of timing if you are allowed a 10% margin on the clock period?