Announcements
• Quiz today!

• Final on Thursday, April 30, 9:30-11 am
• Project presentations on Monday, May 4
• Course surveys:
  * [https://drive.google.com/file/d/1saRVPwUtLIRBApUzZ0Y9XR9AgvANFzdV/view](https://drive.google.com/file/d/1saRVPwUtLIRBApUzZ0Y9XR9AgvANFzdV/view)

Outline
* Module 6
  * Supply distribution

Phase-Locked Loop
* PLL is locked when the phase difference is zero
* Second/third order loop
* $\pm N$ for frequency synthesis (and $x M$)
* Filters input jitter
* Accumulates phase error

Voltage-Controlled Oscillator
* Oscillation frequency controlled by voltage

![ PLL vs. DLL Dynamics](https://inst.eecs.berkeley.edu/~ee241b/lectures/wp_lecture25.png)

- The key difference is in the VCDL vs. VCO transfer characteristics
- VCO integrates (accumulates) phase

$$H_{VCO}(s) = K_{VCO}/s$$
Charge Pump

- Push/pull current source operation

![Charge Pump Diagram]

Charge Pump PLL

- Phase transfer function

\[ H(s) = \frac{K_{PFD} K_{VCO}}{s + \frac{1}{\zeta \omega_n}} \]

- PFD
- VCO
- \( C_p \)
- \( s \)
- \( \zeta \)
- \( \omega_n \)
- \( s + \frac{1}{\zeta \omega_n} \)

Charge Pump PLL with a Zero

- Charge pump PLL has a stability problem
- Compensation by adding a zero

![Charge Pump PLL with a Zero Diagram]

Higher Order Loops

- Another pole naturally exists
- Filters the control voltage \( V_{CTRL} \)
- Lowers phase margin
- Reduces the lock range

![Higher Order Loops Diagram]

Phase Noise at the PLL Input

- Low-pass characteristic

\[ H(s) = \frac{\phi_{out}(s)}{\phi_{in}} = \frac{\omega_n^2}{s^2 + 2\zeta \omega_n s + \omega_n^2} \]

VCO Phase Noise

- High-pass characteristic

\[ \frac{\phi_{out}(s)}{\phi_{VCO}(s)} = \frac{s(s + \omega_n \omega_{PF})}{s^2 + 2\zeta \omega_n s + \omega_n^2} \]

6.D Interaction with Supply
Power Delivery

- Decoupling in Core i7

Andreas Hopf/Flickr

Skylake-SP, ISSCC'18

EECS241B L25 SUPPLY

Inside Haswell

Review: Power Cell Architecture

- Each power cell = Mini VR
  - Up to 25A current - tested
  - Programmable switching frequency (60Hz to 1.4MHz)
  - Regulated inductor topology
  - 16 phases per power cell, 320 phases per chip
  - High-phase count reduces noise, ripple
  - High scalability
  - Cell shedding
  - Bridge shedding
  - BST
    - Self-load and characterization system

EECS241B L25 SUPPLY

Power Delivery

- Typical model

Wong, JSSC'06

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Supply Resonances

- First droop
  - Package L + on-die C
- Second droop
  - Motherboard + package decoupling
- Third droop
  - Board capacitors

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Inside Intel Broadwell

- Inductors moved to a small PCB

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How to model

- Abstracted delay line

Wong, JSSC'06
This Class
- Put design choices in technology perspective
- The design constraints have changed and will be changing
  - Cost, energy, (power, leakage, ...), performance
- Focused on variability, power-performance tradeoffs, power management
- Did not cover arithmetic, domino, I/O, supply generation, packaging, ...

This Field
- Moore’s law will end sometime during your (my?) career
  - 5nm in 2020 scales to 0.1nm by 2050 with 2-yr cycles (or to 1nm with 4-yr cycles)
- Physics will stop CMOS somewhere ~3nm (?)
  - Will we see a different CMOS device in the meantime
- Economics will likely stop it somewhere while still in single digits
  - And the nodes will be stretched out
- We will see multi-chip/packaging solutions
- Don’t worry: Creativity is unlimited!
  - What can you build with 10B/100B/1 trillion transistors?
  - Even filling 10B-transistor chips with SRAM is not trivial!

Technology Strategy / Roadmap

- Plan A: Extending Si CMOS
- Plan B: Subsystem Integration
- Plan C: Post Si CMOS Options
- Plan Q: Quantum Computing

Reference: T.C. Chen, Where Si-CMOS is going: Trendy Hype vs. Real Technology, ISSCC’06