March 16, hpcwire.com: Folding@home Turns Its Massive Crowdsourced Computer Network Against COVID-19
Announcements

• Project midterm reports postponed until Tuesday, March 31

• Assignment 3 postponed until Thursday, April 2.

• Reading – req’d


• Recommended

Outline

- **Module 4**
  - SRAM alternatives

- **Module 5**
  - Low-power design
  - Power-performance tradeoffs
4.J SRAM Alternatives
eDRAM

- Process cost: Added trench capacitor
Crosspoint Memories


Fig. 2—Memory structure. $I_1$ and $I_2$ are access drive currents to core-selection switch. Presence or absence of a magnet over a twistor-strip solenoid crosspoint yields a “zero” or “one.” Signals observed between twistor and return wire.
Crosspoint Memories

- Neale, Nelson, Moore, Electronics’70
  - 16 x 16 array (256b) of ‘read-mostly memory’
Crosspoint Memory

- Four modes
  - Form
  - Set
  - Reset
  - Read

> Endurance
3D Crosspoint Arrays

- Kau, IEDM’09
- Yeh, JSSC’15
- Ou, JSSC’11
Crosspoint Arrays

• Read and sneak currents

Bae, TED 4/17
In the News...

• Intel Optane = 3D XPoint

**DDR-T Protocol**
- Protocol on top of electrical/mechanical interface for DDR4
- Allows for asynchronous command/data timing
  - Controller uses request/grant scheme to communicate with host controller
  - Data bus direction and timing controlled by host
  - Command packet per request sent from host to Intel® Optane™ DC persistent memory controller
- Transaction can be re-ordered in the Intel Optane DC persistent memory controller
- 64B cache line access granularity (similar to DDR4)
Optane DDR

- **PMIC**: Generates all the rails for Media and controller
- **SPI Flash**: Where FW is saved
- **Intel® Optane™ media**: 11 parallel devices for data + ECC+ spare
- **DQ buffers**: Need for high bit rate signal integrity
- **AIT DRAM**: Where address indirection table lies
- **Energy store caps**: Ensures flushing of all module queues at power fail

![Diagram of Optane DDR architecture](image)

**Intel® Optane™ DC persistent memory controller**

- **AES-XTS 256 encryption**
- **ECC engine**
- **Power and thermal control**
- **DDR-T agent**
- **SMBus, SPI GPIO**

**Connections**

- 256B transfers
- 64B transfers
- C&A Bus
- DRAM
- PMIC
- Power rails
5. Low-Power Design
Importance of Power Awareness

• Energy: Crucial for Portable Applications
  • Determines battery lifetime
  • Amount of computation that can be performed
  • Performance is what sells products

• Power: Crucial for High-Performance Applications
  • Determines cooling and energy costs
  • Most designs today are power limited
  • Still need maximum performance
The Old Design Philosophy

• Maximum performance is primary goal
  • Minimum delay at circuit level

• Architecture implements the required function with target throughput, latency

• At circuit level, supplies, thresholds set to achieve maximum performance, subject to reliability constraints

• Performance achieved through optimum sizing, logic mapping, architectural transformations
Constant Field Scaling Model

Traditional scaling model

If $V_{DD} = 0.7$, and $Freq = \left(\frac{1}{0.7}\right)$,

$$Power = CV_{DD}^2f = \left(\frac{1}{0.7} \times 1.14^2\right) \times (0.7^2) \times \left(\frac{1}{0.7}\right) = 1.3$$

Maintaining the frequency scaling model of 1990s

If $V_{DD} = 0.7$, and $Freq = 2$,

$$Power = CV_{DD}^2f = \left(\frac{1}{0.7} \times 1.14^2\right) \times (0.7^2) \times (2) = 1.8$$

While slowing down voltage scaling

If $V_{DD} = 0.85$, and $Freq = 2$,

$$Power = CV_{DD}^2f = \left(\frac{1}{0.7} \times 1.14^2\right) \times (0.85^2) \times (2) = 2.7$$
Power delivery and dissipation will be prohibitive

2001 Picture: Power As a Problem

S. Borkar
The New Design Philosophy

• Maximum performance is too power-hungry, and/or not even practically achievable
• Extract maximum performance under a power/energy envelope
• Excess performance (as offered by technology) to be used for energy/power reduction

Trading off speed for power
5.A Power and Energy Basics
Portability: Battery Limits

• Little change in basic technology
  • store energy using a chemical reaction

• Battery capacity doubles every 10 years
  • Has slowed down

• Energy density/size, safe handling are limiting factor

<table>
<thead>
<tr>
<th>Energy density of material</th>
<th>KWH/kg</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gasoline</td>
<td>14</td>
</tr>
<tr>
<td>Lead-Acid</td>
<td>0.04</td>
</tr>
<tr>
<td>Li polymer</td>
<td>0.15</td>
</tr>
</tbody>
</table>
Battery Progress

First Commercial Use

- NiCd
- SLA
- NiMH
- Li-Ion
- Reusable Alkaline
- Li-Polymer

Energy Density (Wh/kg)

Trend Line
Comparison of Energy Densities for Various Battery Chemistries

- Li-P, Li-Ion: Ref: 18650; 4.0Ah
- Li-Ion: Ref: 18650; 3.6Ah
- Li-Polymer: Ref: 454261 Polymer
- Li-Metal: Ref: 933450 Prismatic Cell
- Zn/Air

Characteristics:
- Smaller
- Wh/kg
- Lighter

Technology Types:
- Emerging Technologies
- Established Technologies
Battery Technology Saturating

Battery capacity naturally plateaus as systems develop

[Courtesy: M. Doyle, Dupont]
5.B Power-Performance Tradeoffs
Know Your Enemy

• Where does power go in CMOS?
  • Switching (dynamic) power
    • Charging capacitors
  • Leakage power
    • Transistors are imperfect switches
  • Short-circuit power
    • Both pull-up and pull-down on during transition
• Static currents
  • Biasing currents
Summary of Power Dissipation Sources

\[ P \sim \alpha \cdot (C_L + C_{CS}) \cdot V_{\text{swing}} \cdot V_{DD} \cdot f + (I_{DC} + I_{\text{Leak}}) \cdot V_{DD} \]

- \( \alpha \) – switching activity
- \( C_L \) – load capacitance
- \( C_{CS} \) – short-circuit “capacitance”
- \( V_{\text{swing}} \) – voltage swing
- \( f \) – frequency

- \( I_{DC} \) – static current
- \( I_{\text{Leak}} \) – leakage current

\[ P = \frac{\text{energy}}{\text{operation}} \times \text{rate} + \text{static power} \]
CMOS Performance Optimization

- Reminder - sizing: Optimal performance with equal fanout per stage
- Extendable to general logic cone through ‘logical effort’
- Equal effective fanouts \( (g_i C_{i+1}/C_i) \) per stage
- Optimal fanout is around 4

![Diagram of CMOS logic circuit](https://via.placeholder.com/150)

[Ref: I. Sutherland, Morgan-Kaufman'98]
Increasing performance increases power!
Performance Optimization

Energy

Mircoarchitecture A

Mircoarchitecture B

Delay = 1/Performance
Next Lecture

• Spring break
• Low-power design
  • Power-performance tradeoffs