EE241B : Advanced Digital Circuits

Lecture 16 – SRAM Options

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Announcements

• Project midterm reports postponed until Tuesday, March 31
• Assignment 3 postponed until Thursday, April 2.
• Reading – req’d
• Recommended
Outline

• Module 4
  • Sense amp timing
  • Redundancy and ECC
4.G Sense-Amp Timing
SRAM Periphery Design

• SRAM periphery:
  • Decoders (covered in EECS251A)
  • Bitline design and sense-amps
Sense-Amp Triggering

- Some older techniques
Sense-Amp Triggering

- Replica bitline

Amrutur, JSSC’98
Multiplicative Replica Bitline

- Conventional replica

Niki, JSSC’11
4.H Redundancy and ECC
Redundancy and ECC

• Redundancy
  • Spare columns (or rows)
  • Selected at test via eFuse
  • Possible to dynamically program redundancy

• ECC
  • Error detection/correction codes
  • Parity
  • SECDED
  • DECTED
Redundancy

- **Principle**

- **Rows**

- **Columns**


McPartland, CICC’00.
Redundancy

- Effectiveness (Bickford, 2008)

Figure 1: Modeled Yield impact comparison for 65 nm SRAM complier. Vmin cell fail rate used in analysis shown in the left chart is 5.10 sigma. Vmin cell fail rate used in the analysis shown in the right chart is 5.20 sigma. 147 Kbit segment is a standardized array size block segment used for comparison purposes.
Error Correction

• Parity (SED)

• SECDED

• DECTED
Multi-bit Errors


Model used in circuit simulation

Model used in device simulation

Kawahara, ISSCC’07 tutorial
Soft Errors

• From packaging and cosmic rays

• Packaging:
  • Lead contains Po-210 -> (5 days) -> Bi-210 -> (22.3 years) -> Pb-210
  • Or Po-210 -> (138.4 days) -> Pb-210
  • Need ‘old lead’

• Cosmic rays
  • Large particles collide with Earth’s atmosphere to produce alpha (and other) particles
Multi-bit Errors

Kawahara, ISSCC'07 tutorial

Ref.: K. Osada et al., [11]
Multi-bit Errors

Equivalent circuits of 16 SRAM cells between well tap

Ref.: K. Osada et. al., [11]

SRAM cell with parasitic bipolar

Well tap/16 cells
Parasitic bipolar effect

Measured
Peak neutron energy: 63.5 MeV

Well tap/cell

Max. no. of errors per cosmic-ray strike

Ratio of multiple to single errors (%)
Multi-bit Errors: Interleaving

Placement at alternate addresses

Multi-error B
Word<0> A0 A1 A0 A1 A0 A1
Word<1> A2 A3 A2 A3 A2 A3
Word<2> A4 A5 A4 A5 A4 A5
Word<3> A6 A7 A6 A7 A6 A7
Word<4> A8 A9 A8 A9 A8 A9

Multi-error A
2 to 1 2 to 1 2 to 1 2 to 1
S.A. S.A. S.A. S.A.

Data: 128 bit Parity: 10 bit

Ref.: K. Osada et al., [12].

Cell

Data is not corrected
All data is corrected

Neutron peak energy: 63.5 MeV
Total fluency: \(6.14 \times 10^6\)/cm²

w/o ECC

This work

SER (arbitrary unit)
4.1 Options for Scaling
SRAM Scaling

• Approaching fundamental limits:
  • Don’t scale cell size
  • Increase transistor count (from 6)
  • Change technology (e.g. channel material)
  • eDRAM
  • NVRAM
  • Or something else…

![Graph showing cell size vs. technology node](image)
Vmin Scaling Projections

- Itoh, ISSCC’09
8-SRAM

- Dual-port read/write capability (register-file-like cells)
- N0, N1 separates read and write
  - No Read SNM constraint
  - Half-selected cells still undergo read
- Stacked transistors reduce leakage

Read circuit?
Interleaving?
4.J SRAM Alternatives
eDRAM

- Process cost: Added trench capacitor

Barth, ISSCC'07, Wang, IEDM'06
Crosspoint Memories


Fig. 2—Memory structure. $I_1$ and $I_2$ are access drive currents to core-selection switch. Presence or absence of a magnet over a twistor-strip solenoid crosspoint yields a “zero” or “one.” Signals observed between twistor and return wire.
Crosspoint Memories

- Neale, Nelson, Moore, Electronics’70
- 16 x 16 array (256b) of ‘read-mostly memory’
Crosspoint Memory

- Four modes
  - Form
  - Set
  - Reset
  - Read

Endurance

![Graph showing endurance](image-url)
3D Crosspoint Arrays

- Kau, IEDM’09
- Yeh, JSSC’15
- Ou, JSSC’11
Crosspoint Arrays

• Read and sneak currents

Bae, TED 4/17
Next Lecture

• Low-power design
  • Power-performance tradeoffs