Broadband Microwave Distributed Amplifier

KEVIN BOWERS and PATRICK RIEHL

Abstract—We present an analysis of distributed amplifiers suitable for use in the microwave regime. From this we evaluate several designs using ideal components and the UC-Berkeley 217 GaAs FET. Alterations to the basic design including the use of CASCODE and CASCODE gain cells and the use of series capacitors on the gate lines are discussed. We implement a final design using microstrip components. The 5-stage design achieves 19.4 dB of power gain (+/- 1.2 dB) from 0.1 to 14.3 GHz. Reflected power at the input and output from loads matched to 50 Ohms are all below –20 dB over the bandwidth of the device, as is power transmitted from the output to the input. The device is stable for broad range of input and output loads. A novel matching network has been designed to minimize reflections along the gate and drain lines over all frequencies and eliminate resonant peaks that are a potential cause of instability externally. Measurements suggest the design is internally stable as well.

Index Terms—distributed amplifier, broadband amplifier, microwave circuits

I. Introduction

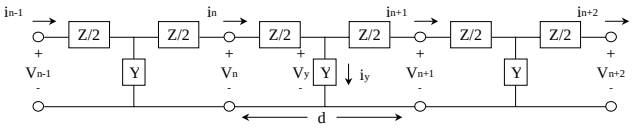
The principal of distributed amplification was originally applied to vacuum tubes structures[1]. The principle has been applied in many other devices, including lasers, traveling wave tubes and, most relevant to us, microwave amplifiers. Because of its broad range of applications, extensive literature exists on the subject. [2],[3] contain many references to this literature.

In a common source microwave FET distributed amplifier, a discrete component transmission line is constructed out of the gate - source input admittance - the gate line. Another (ideally) identical transmission structure is drain - source input admittance – the drain line. If the transmission structures are identical, a wave can be launched on the gate line and be coherently amplified onto the drain line. It is a simple matter to construct transmission lines with identical properties on the gate and drain lines assuming a unilateral transistor over a very wide range of frequencies. Thus these devices are naturally broadband. Also, by using FET parasitics as a part of the transmission lines, some FET limitations can be avoided.

In this report, we evaluate several designs subject to the design goal of maximizing gain bandwidth product. The designs attempt to match the impedance of the input and output ports to 50 Ohms over the bandwidth of the device. We also try to achieve as much gain flatness as possible. The designs only use the UC-Berkeley 217 GaAs FET and are easily implemented using microstrip components; undesirable components such as spiral inductors are avoided.

II. Discrete Transmission Lines

In order to derive design formulae for a FET DA, we must first consider propagation of waves on discrete transmission structures. Alternative treatements can be found (Pozar, *op. cit.* and in [4]). Consider the following circuit (Z and Y are arbitrary complex impedances and all voltages and currents are phasors):



Applying Kirchoff's laws to the circuit we arrive at the following equations:

$$\left.\begin{aligned} i_y &= Yv_y \\ i_n &= i_{n+1} + i_y \\ v_n - v_y &= \tfrac{1}{2}Zi_n \\ v_y - v_{n+1} &= \tfrac{1}{2}Zi_{n+1} \end{aligned}\right\} \Rightarrow \begin{cases} i_{n-1} - (ZY+2)i_n + i_{n+1} = 0 \\ v_n - v_{n+1} - \tfrac{1}{2}Z(i_n + i_{n+1}) = 0 \end{cases}$$

Assuming traveling waves on the circuit of the form, $v_n = Ve^{-j\theta n}, i_n = Ie^{-j\theta n}$, we obtain the following expressions for the wave impedance and phase shift per segment:

$$\theta = \cos^{-1}(1+\tfrac{1}{2}ZY) = 2\sin^{-1}\sqrt{-\tfrac{1}{4}ZY}$$

$$Z_{line} = \sqrt{\tfrac{Z}{Y}}\cos\tfrac{1}{2}\theta = \sqrt{\tfrac{Z}{Y}}\sqrt{1+\tfrac{1}{4}ZY}$$

For a line consisting of ideal shunt capacitors and ideal series inductors we have:

$$Z_{line} = \sqrt{\tfrac{L}{C}}\sqrt{1-\tfrac{\omega^2}{\omega_c^2}} \text{ where } \omega_c = \tfrac{2}{\sqrt{LC}}.$$

A parallel analysis for a π section discrete transmission line yields:

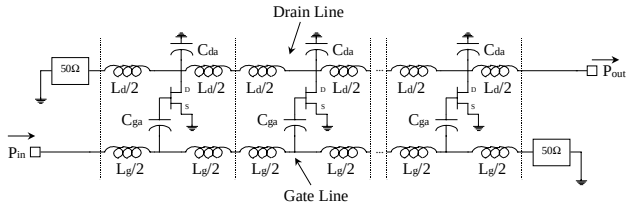
$$Z_{line} = \sqrt{\tfrac{L}{C}} \Big/ \sqrt{1-\tfrac{\omega^2}{\omega_c^2}}$$

From this we see that the impedance of the line is frequency dependent and the line has a cutoff frequency such that no waves of higher frequency can propagate.

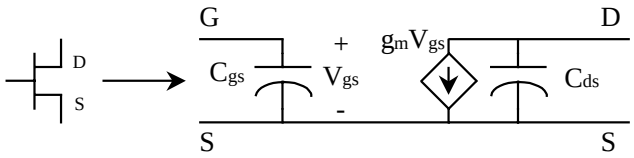
In a typical FET implementation the shunt capacitors are partly provided by the FET and transmission lines serve as the inductors. Thus, for a given impedance for the line, the gate source (or drain source) capacitance becomes a limiting factor to the bandwidth for the amplifier.

III. "Rule of Thumb" FET Distributed Amplifier Formulae

Below a simple FET DA is shown:



In the ensuing analysis, we assume an idealized FET model:



In order to match the phase shifts on both the gate and drain lines while matching the impedances to 50 Ohms, we must have:

$C_{gs} // C_{ga} = C_{ds} + C_{da}$

and

$L_d = L_g = (50\Omega)^2(C_{gs} // C_{ga})$

For this values, the impedance of the gate and drain lines is well-matched to 50 Ohms for frequencies well below the cutoff of the line. We will do a better job of matching later.

The above relations leave C_{da} unspecified. For a positive capacitance in a FET with $C_{gs} > C_{ds}$, as is true for nearly all FETs, the two extremes are $C_{da} = 0$ (C_{da} is an open circuit) and $C_{da} = C_{gs} – C_{ds}$ (C_{ga} is a short circuit).

A four section distributed amplifier was designed with the above relations for the two extreme cases. Figure B1 shows the result of equalizing the lines to C_{ds} and Figure B2 shows the result of equalizing the lines to C_{gs}. The greater bandwidth of figure B1 is apparent (about 50 GHz), however, the design does not achieve any amplification. The design in Figure B2 has substantially less bandwidth (about 20 GHz), but it does achieve a power gain of about 16 dB.

IV. Design Review Amplifier

This design approach discussed above can be improved by optimizing the lines for phase shift per segment and impedance. The scattering parameters shown in Figure B3 were presented in the 217 Design Review. The component values used were:

$L_g = 0.39751$ nH
$C_{ga} = 0.32036$ pF
$L_d = 0.40772$ nH
$C_{da} = 0.057345$ pF
$N_{sections} = 10$

The optimization accounted for the drain source resistance (R_{ds} - in parallel with C_{ds}) and gate source input resistance (R_i - in series with C_{gs}). The following function was minimized:

$$f(L_g, L_d, C_{ga}, C_{da}) = \sum_{\substack{design \\ freqencies}} a\left|\Gamma_g\right| + b\left|\Gamma_d\right| + c\left|\mathrm{Re}\,\theta_g - \mathrm{Re}\,\theta_d\right|$$

Γ_g and Γ_d are the reflection coefficients of the gate and drain lines off a 50 Ohm resistor respectively. Similarly, Re θ_g and Re θ_d are the phase shifts per section of waves traveling on the gate and drain lines. (a,b,c) are adjustable weights (chosen such that the terms of the initial guess contributed in the ratio 4:2:1). The initial guess was chosen by the Rule of Thumb rules with $C_{ga} = 3C_{gs}$. The design frequencies were at 1,2,4,8 and 16 GHz. The Nedler-Mead simplex method was used (MATLAB function "fmins") to minimize the function.

The optimal number of sections to use was computed at 16 GHz from the following formula (given in Pozar, *op.cit.*):

$$N_{opt} = \frac{\ln(\alpha_g l_g / \alpha_d l_d)}{\alpha_g l_g - \alpha_d l_d}$$

where the loss per section on the gate and drain lines is given by:

$$\alpha_g l_g = -\mathrm{Im}\,\theta_g, \alpha_d l_d = -\mathrm{Im}\,\theta_d$$

The resulting amplifier achieved 20 dB of power gain over a bandwidth of about 25 GHz. The scattering parameters can be found in Figure B3. It should be noted that gain is achieved in this amplifier beyond f_T of the 217 FET (21 GHz). Physically this is because the FET parasitics C_{gs} and C_{ds} now work in favor of the design .

V. Gain Bandwidth Tradeoff the Series Capacitance on the Gate Line

Since C_{ga} improved the bandwidth at the expense of gain, it is desirable to know the optimal value of C_{ga} for gain bandwidth product for a given number of sections. This may be crudely estimated by noting that the presence

of C_{ga} makes the voltage across C_{gs} equal to (in the case of an idealized FET):

$$V_{gs,n} = V_{g,n}\frac{1/\,j\omega C_{gs}}{1/\,j\omega C_{gs} + 1/\,j\omega C_{ga}} = V_{g,n}\left(\frac{1}{1+x}\right), x = \frac{C_{gs}}{C_{ga}}$$

where $V_{g,n}$ is the voltage on the n-th section of the gate line at the shunt element. The power gain of such an amplifier is thus proportional to $(1+x)^{-2}$.

Likewise cutoff frequency of the gate line can be written with R are the target line impedance and $L_g = R^2(C_{gs}//C_{ga})$:

$$\omega_{cg} = \frac{2}{\sqrt{L_g(C_{gs}//C_{ga})}} = \frac{2}{R(C_{gs}//C_{ga})} = \omega_{cg0}(1+x)$$

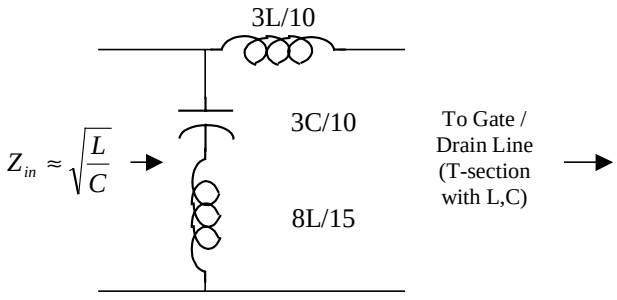
Combining the above results, we find the net power gain bandwidth product is proportional to $(1+x)^{-1}$. For non-negative x, this gain bandwidth function is maximized at zero. This corresponds to shorting out the capacitor C_{ga}.

We see in this analysis then that C_{ga} can only improve bandwidth and not gain bandwidth for a given line impedance and number of sections.

This analysis however does not account for the improvement in loss per segment on the gain line (which would enable more sections and perhaps allow a larger gain bandwidth than a design with fewer sections). In the designs to follow, we will not use C_{ga}, opting for smaller section designs.

VI. Improved Matching Networks on the Gate and Drain Line

The matching networks on the gate and drain lines can be greatly improved if it is noted that the lines act as a constant-k filter section (a discussion of constant k and m derived filter sections can be found in Pozar, *op. cit.*). To match such filter sections, an m-derived bisected π section with m = 0.6 is recommended. For the idealized FET without series capacitors on the gate and drain lines, the matching sections would appear as:



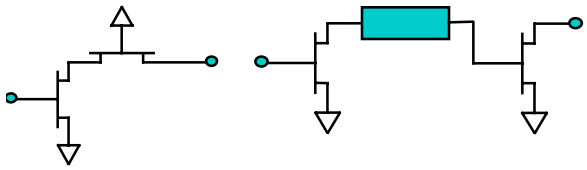
In the microstrip design we implement below (as in all the other designs with gain), the scattering diagrams showed a peak where the stability becomes difficult to insure (S_{11}, S_{22} > 1). To remove these peaks, an m-derived filter section was designed such that its infinite attenuation peak is placed at the frequency of the resonant peak. The m-derived filter section unfortunately cannot be exactly matched to the gate and drain lines because the cutoff frequency of the gate / drain line is above the resonant frequency we are trying to eliminate (for an m-derived filter section, the cutoff frequency is always below the infinite attenuation frequency). Thus for the final design, the input and output an m-derived filter section is matched to 50 Ohms. This section is placed at the input and output of the gate and drain lines (which in turn are matched to 50 Ohms with the m-derived bisected π sections discussed above).

It should be noted than the type of optimization done for the design review amplifier could not substantially improve the phase shift or match characteristics lines designed with the rule of thumb formulae once the bisected pi matching sections were used.

VII. Cascode and Cascade Gain Cells

Although a single transistor in the common-source configuration is the traditional gain element for the distributed amplifier, other configurations are possible.

Both a cascade of two common-source stages and a cascode (common source-common gate) circuit have been implemented by designers interested in higher gain and/or bandwidth for their distributed amplifiers.[5,6]



The cascode circuit shown above (left) has the same transconductance as a single transistor stage, but its output impedance is increased by a factor of approximately $(1+g_mR_{ds})$. The drain-line attenuation of an amplifier using this gain cell is therefore reduced dramatically, while the gain is not directly affected. The decreased drain-line attenuation may allow for a better overall match to the drain line, or it may allow the designer to use more stages. The main drawback of the cascode cell is that it exacerbates the stability problems caused by resonances in s_{22} of the amplifier, since the drain line becomes much less lossy. We decided this disadvantage outweighed the advantages of the cascode for our design. The cascode might be useful, however, in technologies where R_{ds} is lower, such as a bipolar technology, or if the performance in the low end of the frequency spectrum were critical.

The cascade gain cell shown above (right) has a gain larger than that of the single transistor cell by a factor of $(1+g_mR_{ds})$. Its output impedance is identical to that of the common source. The key to the design of the cascade gain cell is the matching network between the two stages. Without some sort of impedance matcher, the bandwidth of the cell is extremely low—in the MHz range. For a narrowband application, it would be possible to simply resonate out the C_{gs} of the second transistor using a parallel inductor. This solution is not sufficient for the bandwidth

of our distributed amplifier, however. We attempted to design a 4-section bandpass Chebychev impedance transformer to match the drain of the first transistor to the gate of the second. This gain cell achieved some degree of matching over a moderate bandwidth, but the gain curve was too uneven to offer any real advantage over the common-source cell. The ripple could most likely be improved with a larger number of sections, but the component count of the n=4 transformer was already unwieldy for a DA.

The conclusion of our investigation into alternate gain cells for the DA was that the simplest solution, the common source, was also the most optimal in this technology. If additional gain were required, the user would be better advised to cascade two entire common-source DAs than to use one with complex gain cells. We can, however, envision situations in which they might be useful.

VIII. Implementation

The final amplifier design was designed using the rule of thumb formula (without C_{ga}). The optimal number of sections was chosen the same as it was for the Design Review circuit. Matching networks and the resonant filter were applying the design as described above. An implementation of the design with ideal components can be seen in figure A1.

We have synthesized the circuit in microstrip technology on a 11 mil GaAs substrate (11 mils avoids Cherenkov radiation at all frequencies of interest). The circuit (figure A2) was constructed using microstrip elements and simulated in HP-EESOF. Since the only reactive components in the lumped-element model are series inductors and shunt capacitors, it was straightforward to synthesize the entire network in microstrip. The series LC resonant sections were implemented by quarter-wave open stubs using widths to match the impedance of the inductor and capacitor. The inductors were synthesized using 1 mil wide microstrips to achieve Z_0=98Ω. The capacitors were implemented with open circuit stubs with width 25 mils, corresponding to an impedance of 27Ω. The lengths of all relevant microstrips were below $\lambda_g/8$. The formulae in Pozar Ch. 4 were used to calculate approximate lengths for all microstrips. The software was unable to handle T-junctions and cross-junctions for our 1 mil wide microstrips, thus we omitted these parasitic elements from our model. These parasitics could subsequenly be tuned out by adjusting the lengths of our L and C components accordingly.

Plots of the scattering parameters for the microstrip model are shown in figures B5 and B6. . The 5-stage design achieves 19.4 dB of power gain (+/- 1.2 dB) from 0.1 to 14.3 GHz. Reflected power at the input and output from loads matched to 50 Ohms are all below –20 dB over the bandwidth of the device.

IX. Stability

We performed simulations to test the internal and external stability of the final microstrip circuit. Input and output stability circles for the entire amplifier are shown in Appendix C. The stability circles plotted from 16-18 GHz show that there is a risk of oscillation at frequencies in that range for some input and output impedances. The circuit is externally stable if both source and load are matched with 50Ω resistances at all frequencies though.

In order to check for internal stability, we devised a test which could easily be applied to gain some understanding of the internal workings of the circuit. We are not certain that this test will correctly predict internal stability in all cases, but it should indicate whether potential problems exist. The methodology of the test is as follows: First, the input and output ports of the amplifier are replaced with 50Ω resistors to ground. Next, the circuit is broken at some internal node, and input and output ports are placed at the two open terminals. We now wish to determine whether there is a potential for oscillation at this node through some internal feedback loop. If so, the power gain of the broken circuit with input terminated in output should be greater than 1 at some frequency. We can use Mason's rule to find the power gain of this broken circuit, as shown in figure p.q.

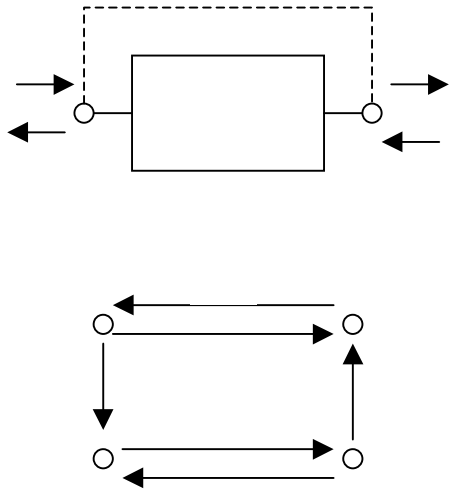


Figure p.q: Block diagram and flow diagram for internal stability test circuit

Using Mason's rule to find *T*, the power transmitted from a_1 to b_2, equivalent to the power gain from a_1 to itself, we find,

$$T = \frac{s_{11}s_{22} + s_{21}(1 - s_{12})}{1 - (s_{11}s_{22} + s_{12} + s_{21}) + s_{21}s_{12}}$$

If *T* has a magnitude greater than 1 and a phase of 0° at any frequency, the circuit will oscillate at that frequency.

We examined several internal nodes of the microstrip circuit and found that, although *T* exceeds 0dB at some frequencies near 17 GHz for all nodes examined, the phase of *T* at these frequencies never crosses 0°. The plot of magnitude and phase of *T* for a typical node is shown in

Appendix C. Therefore we can tentatively conclude that this circuit is internally stable. However, a more rigorous analysis would be required to prove this.

X. Noise

The noise performance for the DA was simulated using the FETN4 noise model (parameters NF=.95, FREF=12). A more accurate noise model of the transistor was created by adding the Cdg, Rds, and Rs parameters externally to the FETN4 element.[7] The FETN4 model does not allow Cdc, the dipole layer capacitance, to be modeled, so there was some discrepancy in the scattering parameters between the noise model DA and that using the 217 FET. Therefore the noise figure measurements should be considered somewhat approximate.

A plot of noise figure for the microstrip DA is shown in Fig. B7. The noise figure in the passband ranges between 6.1dB at 14.3GHz and 1.2dB at 4.4GHz. Over the range from 1.6 to 10.5 GHz, the noise figure is less than 3dB.

XI. Conclusion

In this report we derived design formulae pertinent to the design of FET distributed amplifiers.

We have successfully applied these results to implement a broadband distributed amplifier with respectable gain, noise, input match and output match characteristics. The design is realizable in microstrip and stable for input and output impedances matched to 50 Ohms. Measurements suggest the design is internally stable as well. An improved noise model (including the dipole layer capacitance), T and cross microstrip components while can be simulated down to 1 mil wide lines and additional tests of the internal stability could further verify this design.

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[1] E.L. Ginzton, W.R. Hewlett, J.H. Jasberg and J.D. Noe. "Distributed Amplification." *Proc. IRE*. Vol. 36, pp. 956-969. Aug. 1948.

[2] J.B. Beyer, S.N. Prasad, R.C. Becker, J.E. Nordman, G.K. Hohenwarter. "MESFET Distributed Amplifier Design Guidelines." *IEEE Transactions on Microwave Theory and Techniques.* Vol. MTT-32. No.3. March 1984. Pp. 268-275.

[3] D.M. Pozar. *Microwave Engineering. 2nd ed.* John Wiley & Sons, Inc. 1998.

[4] J.L.B. Walker. "Some Observations on the Design and Performance of Distributed Amplifiers." *IEEE Transactions on Microwave Theory and Techniques.* Vol. 40. No. 1. January 1992. pp. 164-168.

[5] K.W. Kobayashi, L. T. Tran, M. D. Lammer, A. K. Oki and D. C. Streit, "Transimpedance bandwidth performance of an HBT loss-compensated coplanar waveguide distributed amplifier" *Electronics Letters*, Vol. 32, No. 24, Nov. 21 1996, pp. 2287-8.

[6] S. N. Prasad, S. Ponnala, S. Moghe, Z. M. Li, "Cascaded-transistor cell distributed amplifiers", *Microwave and optical technology letters*, Vol. 12, No. 3, June 20 1996, pp. 163-7.

[7] We borrowed this cell from classmate Luca Daniel.

Appendix A: Schematics

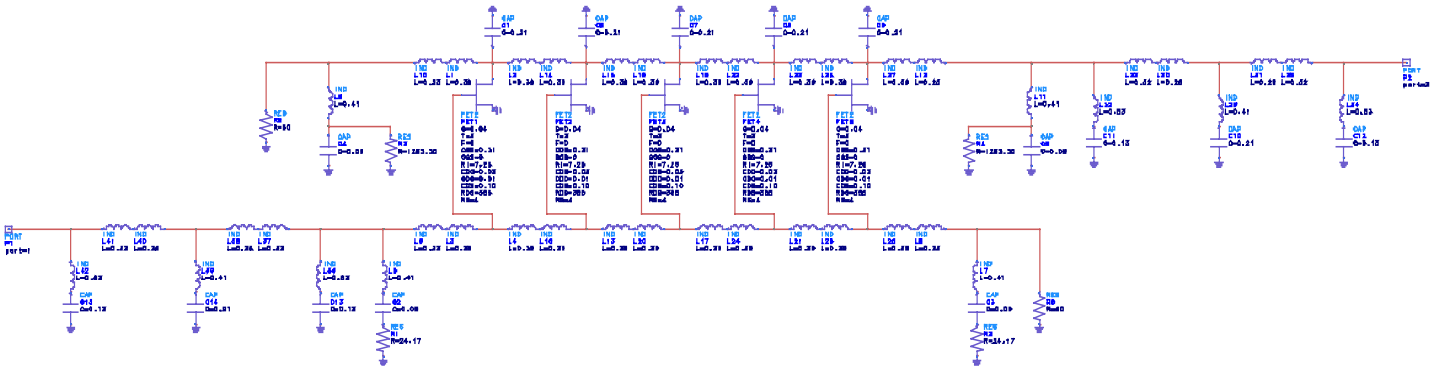


Fig. A1: Optimized distributed amplifier

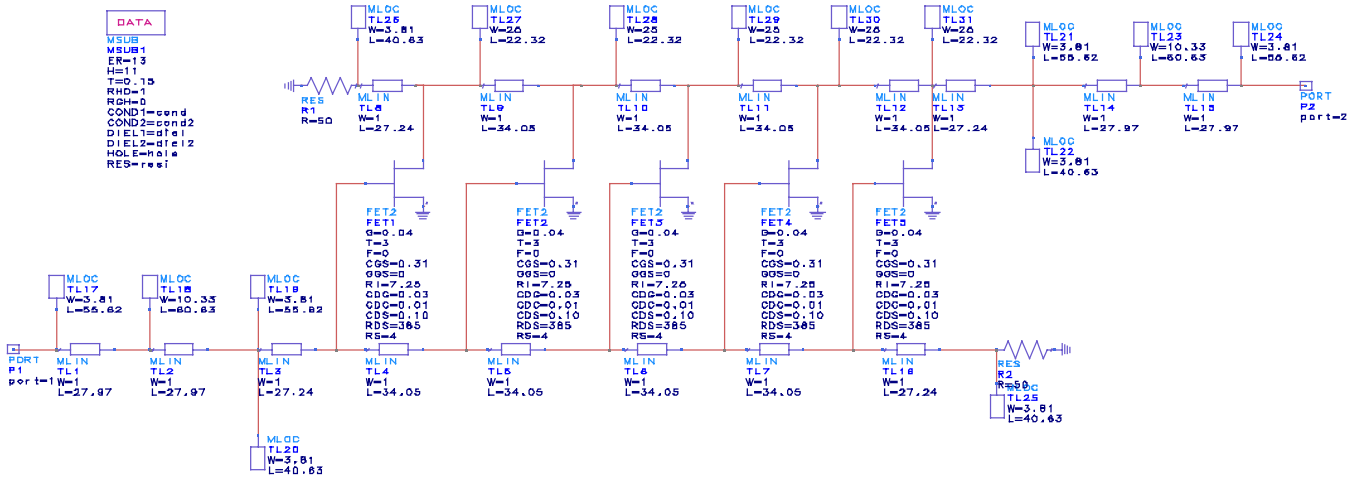


Fig. A2: Microstrip implementation of optimized distributed amplifier

Appendix B: Gain and noise characteristics

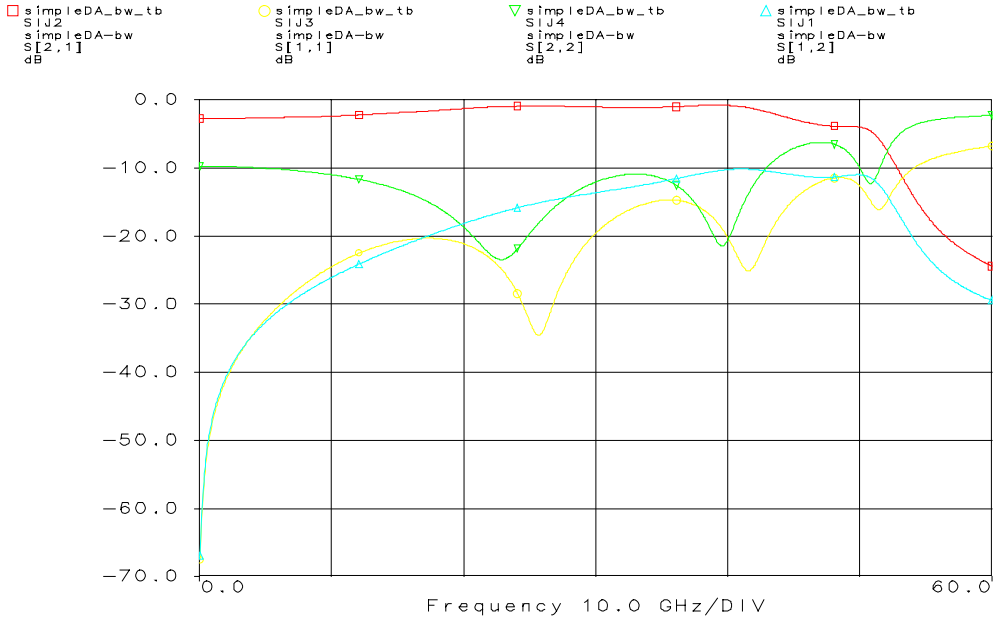


Fig. B1:Scattering parameters of Cds-equalized DA.

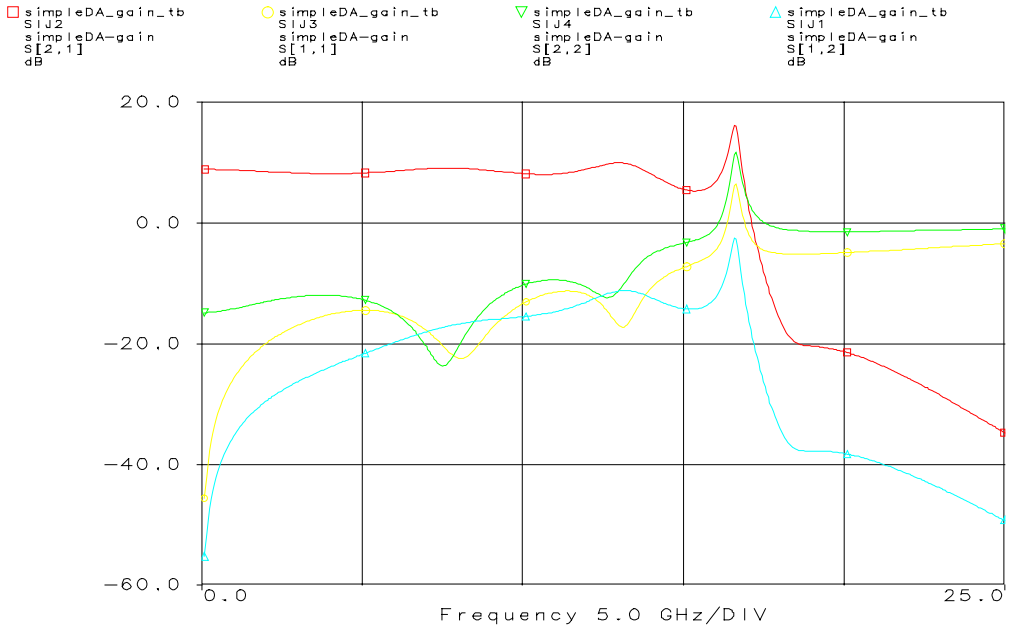


Fig. B2:Scattering parameters of Cgs-equalized DA.

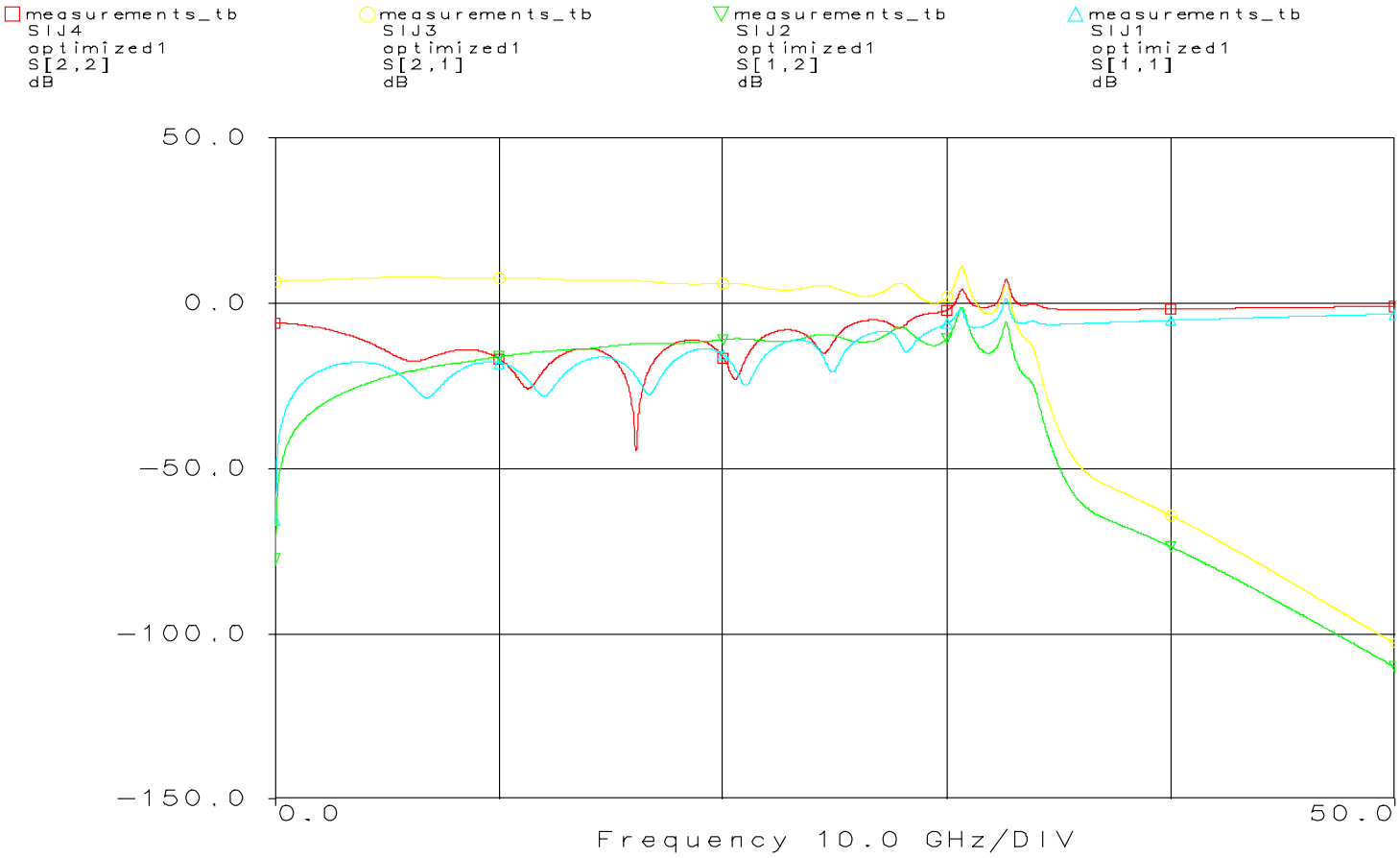


Fig. B3: Scattering parameters of presentation DA.

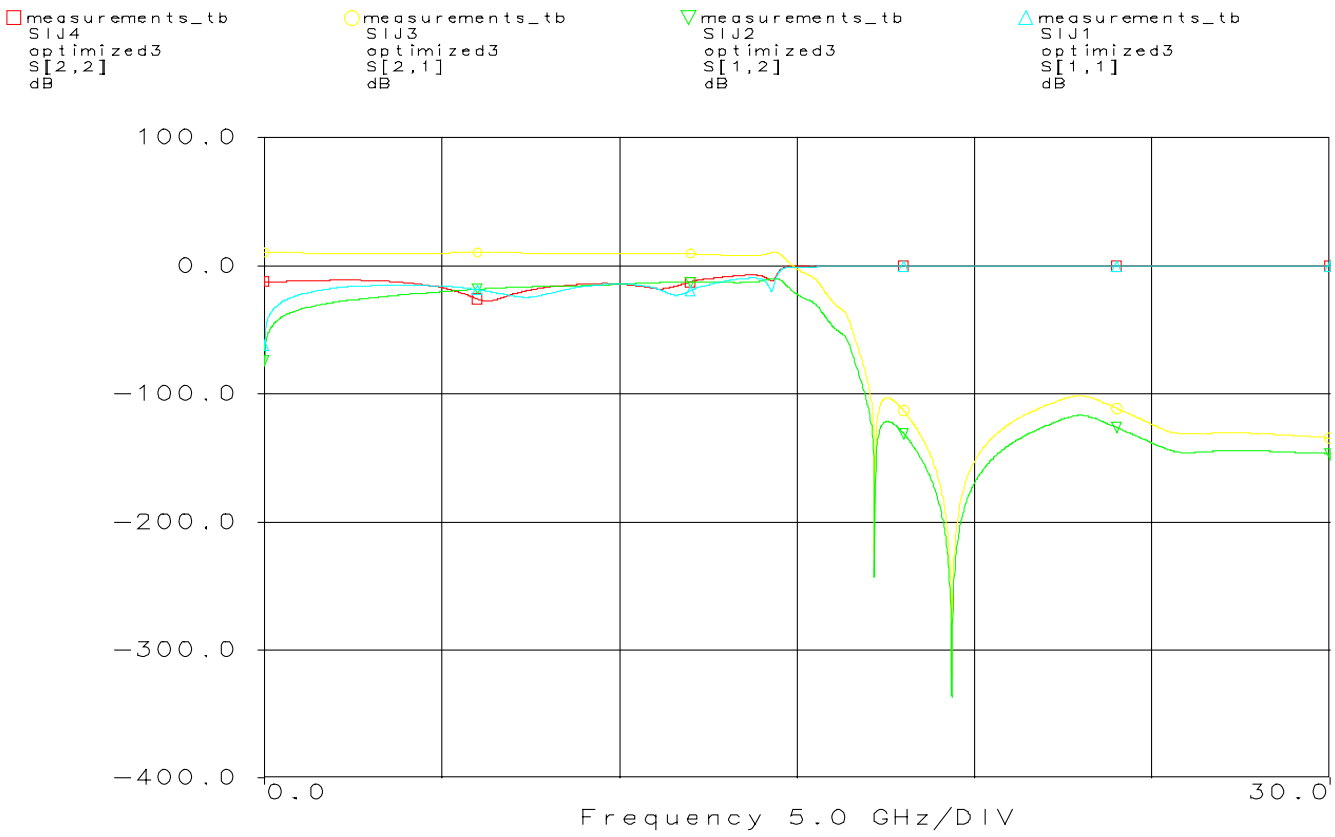


Fig. B4: Scattering parameters of optimized lumped-element DA.

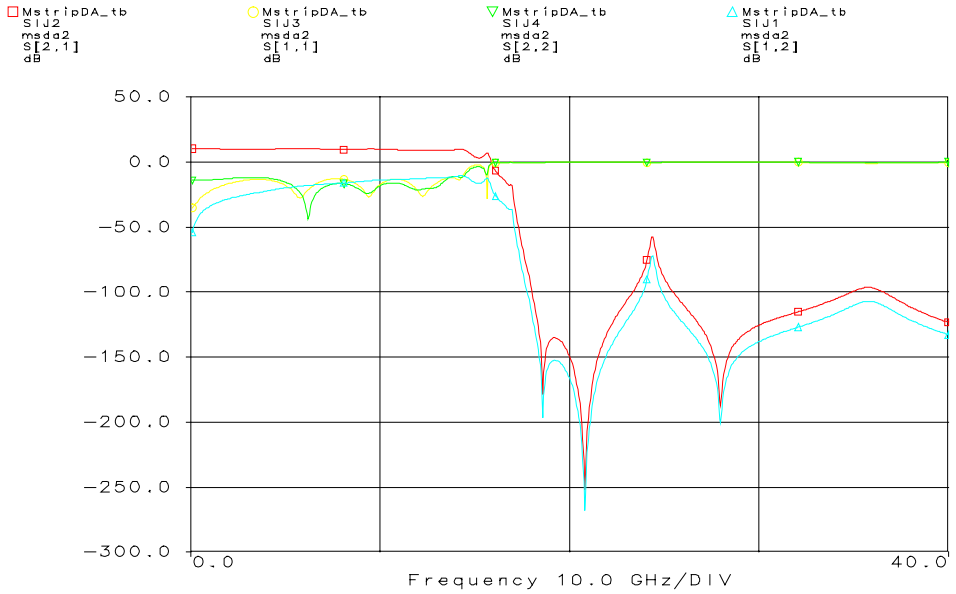
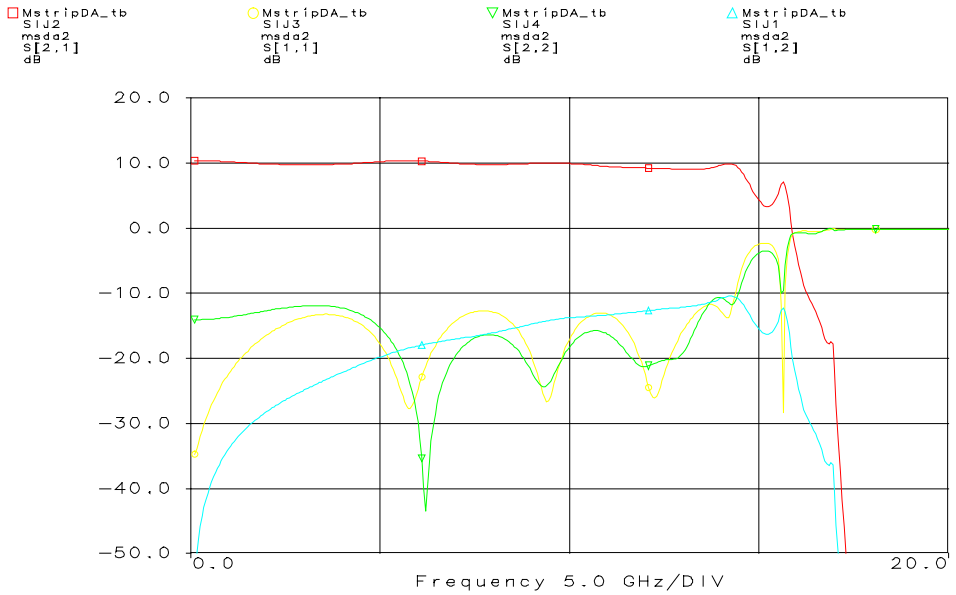


Fig. B5: Scattering parameters of microstrip DA(0-40 GHz)



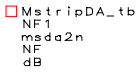


Fig. B6: Scattering parameters of microstrip DA (0-20 GHz)

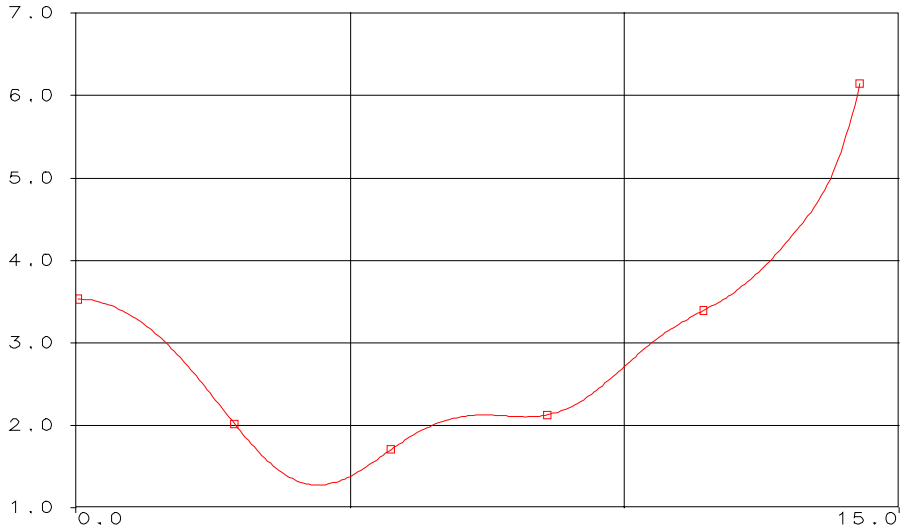
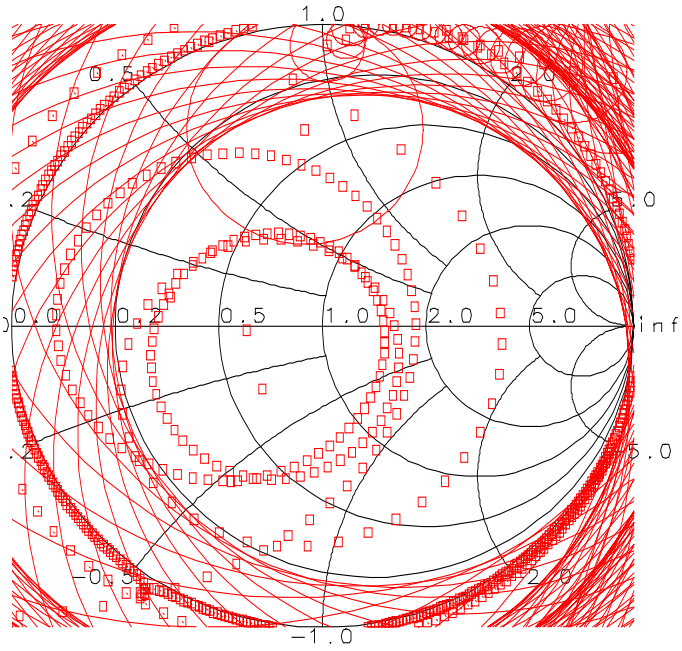


Fig. B7: Noise figure of microstrip DA (0-15 GHz)

Appendix C: Stability circles for microstrip amplifier



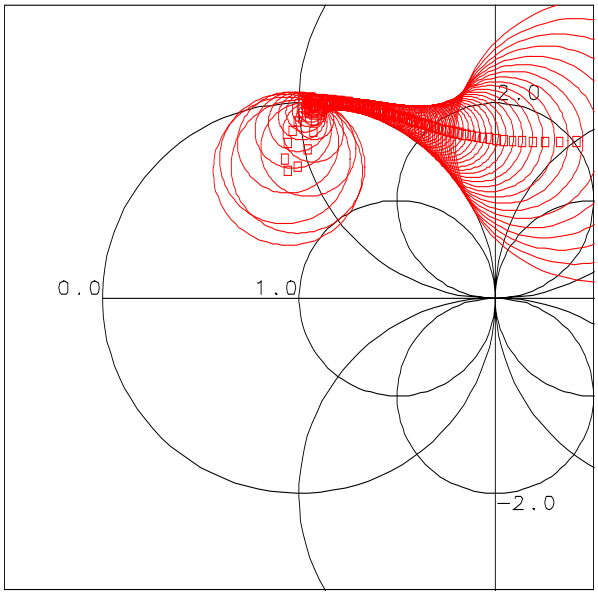
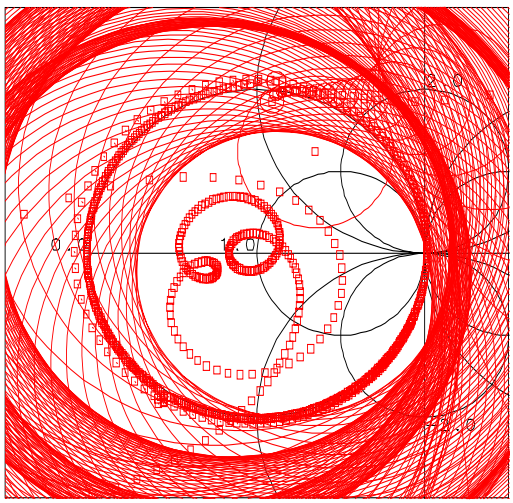


Fig. C1: Input stability circles (0.1-40GHz)

ipDA_tb
2



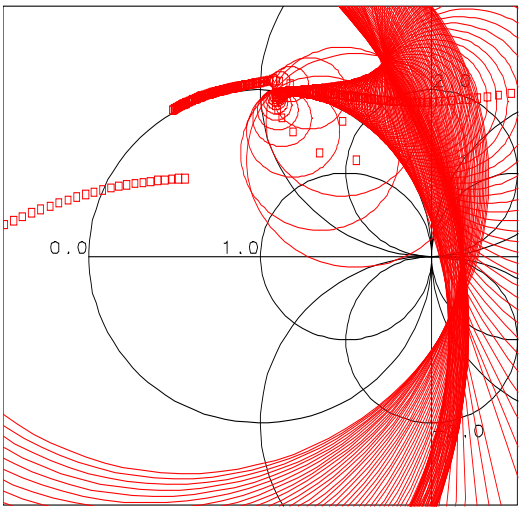


Fig. C2: Output stability circles (0.05-40GHz)

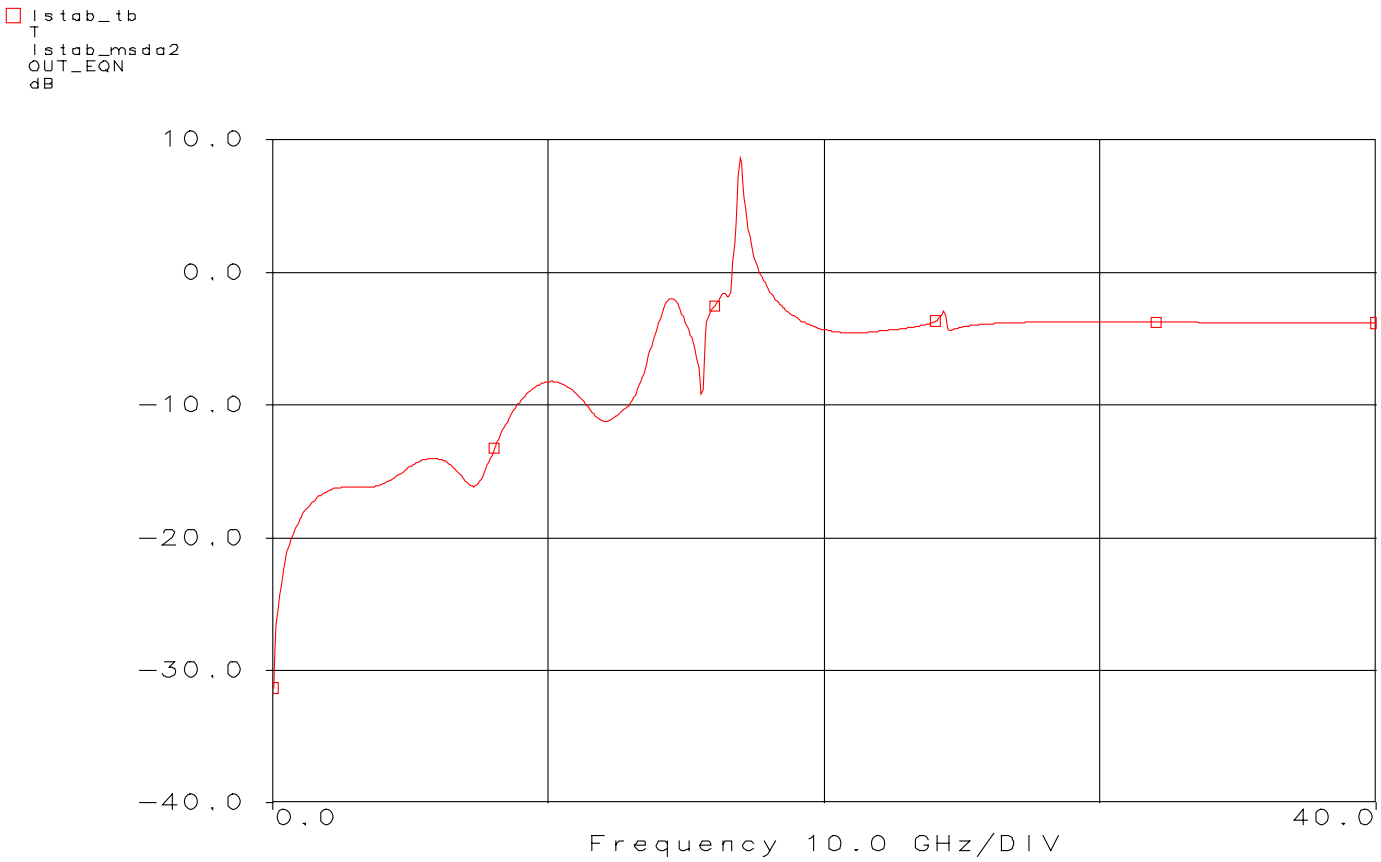


Fig. C2: T-measurement plot (Magnitude, 0.05-40GHz)

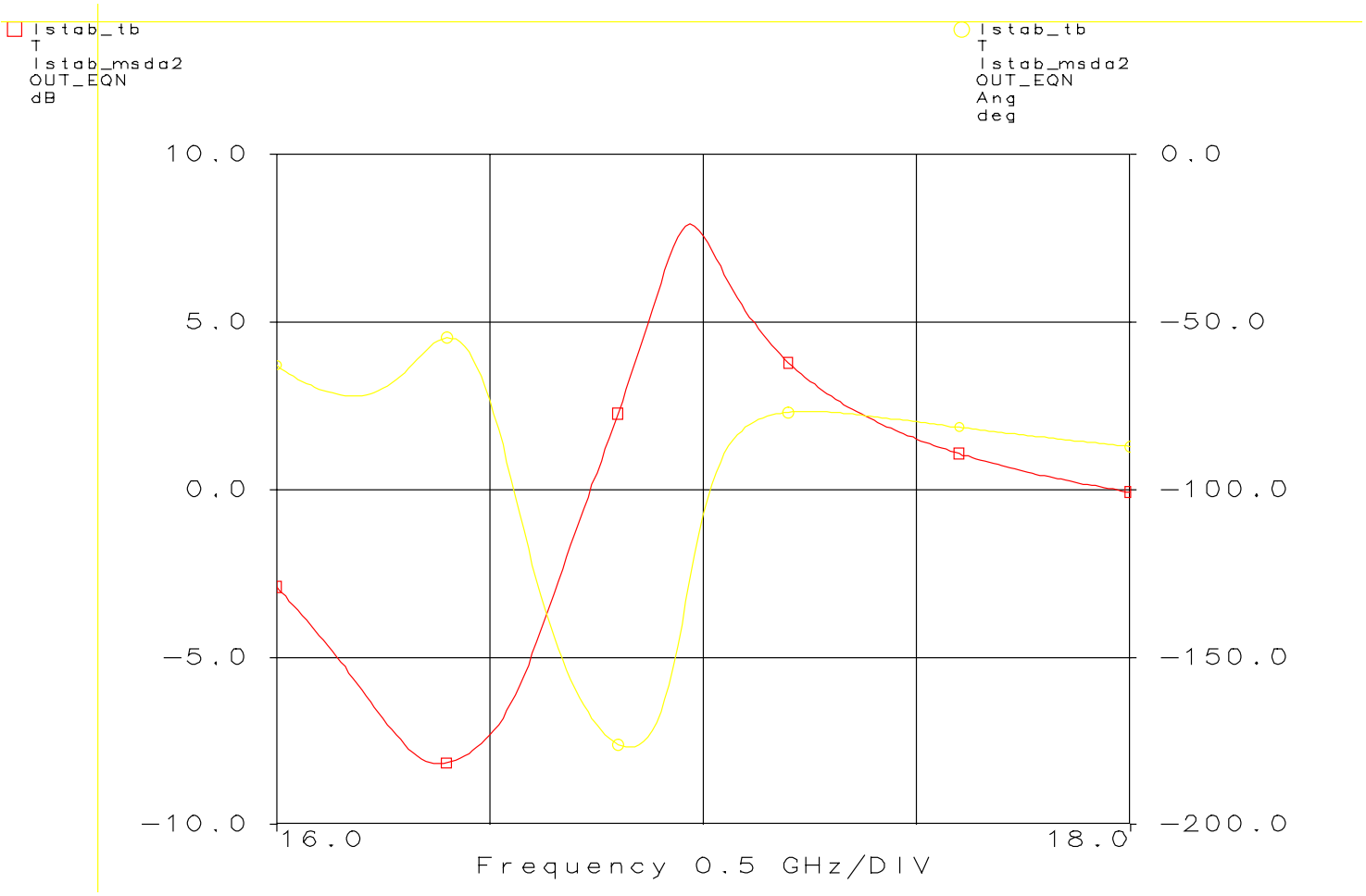


Fig. C4: T-measurement plot (Magnitude and phase, 16-18 GHz)