### 1. MEMS Accelerometer

A micro-electromechanical system (MEMS) accelerometer is a device that can measure acceleration, for example by using a set of strain-sensitive resistors. There are three in every cell phone, detecting the phone's orientation and motion. MEMS accelerometers are made using silicon micromachining. In the accelerometer, a silicon block with a known mass is suspended between springs made of silicon. The compression of the springs can be measured because the resistance of a silicon spring changes when it is compressed. (This occurs because silicon is a piezoresistive material, which we will not talk about in this course.)

Accelerating the device causes the silicon block to move, changing the compression of the attached silicon springs, and therefore changing the resistance across the springs. One of the springs will be compressed while another will be extended, so the resistance of one spring increases while the other decreases. If we measure the changes in the resistance of the springs, then we can understand how the silicon block is moving.

However, the change in resistance is extremely small. For instance, for a change of 9.8m/s² of acceleration (equivalent to the Earth’s gravitational acceleration, $g$), the resistance only changes by about 4% in our example! To measure such a small resistance change, the resistors are placed in the following configuration known as a Wheatstone bridge:

![Wheatstone Bridge Diagram]

The resistances of the two resistors on the left, both with the same value $R_1$, will remain constant. The two resistances on the right represent the silicon springs. The $\varepsilon$ term represents the fractional change in resistance brought about by movement of the silicon block. For example, if $\varepsilon = 0.01$, then the resistance of spring being compressed will increase by 1%, while the resistance of the spring being extended will decrease by 1%.

A voltmeter measures the voltage difference $V_x = u_2 - u_1$ on the device. We use $V_x$ to determine the change in resistance and hence the acceleration.

(a) To determine the acceleration, we first need to understand the relationship between our measured voltage $V_x$ and the resistances of the springs. What is $V_x$ in terms of $R_1$, $R_2$, $\varepsilon$, and $V_S$?
(b) Suppose the minimum voltage the voltmeter can detect is $V_x = 1\mu V$. If this is the minimum $V_x$, what is the minimum measurable resistance change $\epsilon$ that we can measure? We are going to make the simplifying assumption that the $\epsilon$ varies linearly with the acceleration. If each acceleration change of $9.8\, m/s^2$ (1g) corresponds to a change in resistance $\epsilon = 0.04$, then what is the minimum acceleration that can be measured by this system?

2. **RC Circuit**

![RC Circuit Diagram]

(a) Find a differential equation for $V_c(t)$ for $t \geq 0$. Solve the differential equation using the initial condition $V_c(0) = 1V$. Use component values of $C = 1\, \text{fF}$, $R = 10\, \text{k}\Omega$, and $V_s = 2V$. ($1\, \text{fF} = 10^{-15}\, \text{F}$)

(b) Instead of having an initial condition of $V_c(0) = 1V$, we now have an initial condition of $I_R(0) = 150\, \mu A$ ($1\, \mu A = 10^{-6}\, \text{A}$). Find the new expression for $V_c(t)$ for $t \geq 0$. Use the same component values listed in part (a).

3. **Why guessing and checking is alright in solving differential equations**

In lecture (and possibly in other courses), you have seen differential equations solved by looking at the equation, moving parts around, reasoning about it using an analogy with eigenvalue/eigenspaces, and then seeing that the solution that we proposed actually works — i.e. satisfies all the conditions of the differential equation problem. This process should have felt a bit different than how you have seen how systems of linear equations are solved (by doing Gaussian Elimination) where it was clear that every step was valid. Indeed, it is different. Although the eigenvalue/eigenspace analogy to differential equations can be made precise and rigorous, doing that carefully is beyond the scope of this course. In effect, all of that reasoning in between seeing the problem and checking the solution can be considered a kind of inspired guessing.

This should lead you to a natural question — how can we be sure that we have found all of the solutions? We’ve checked to see that the solution we found solves the equations, but maybe there are more solutions that are different. How can we be sure? After all, we are using the solution of the differential equation for its predictive power — for example, we are using the fact of RC time constants to argue that this limits the speed of digital computation. Making such inferences is only proper if we have indeed found the only solution to the differential equation.

In the mathematical literature, this is sometimes referred to as the problem of establishing the “uniqueness” of solutions. The concept is also very important for us in engineering contexts. You have already seen in EE16A’s touchscreen module that node voltages need not be unique, and that is why you need to specify a ground in your circuit. You also saw this concept in EE16A’s localization module where you learned how to approach inconsistent linear equations by the method of least squares: you started with no solutions, allowed some error and then got infinitely many potential solutions with error. To make the solution unique, you had to specify that you wanted to minimize the size of the hypothesized error.
This problem walks you through an elementary proof of the uniqueness of solutions to a simple scalar differential equation of the form

\[
\frac{d}{dt} x(t) = \alpha x(t) \tag{1}
\]

with initial condition

\[
x(0) = x_0. \tag{2}
\]

Being able to do simple proofs is an important skill, not only in its own right, but also for the systematic logical thinking that it exercises. This problem has multiple parts, but the goal is simply to help you see how you could have come up with this proof entirely on your own.

(a) **Please verify that the guessed solution** \( x_d(t) = x_0 e^{\alpha t} \) **satisfies (1) and (2).**

(b) To show that this solution is in fact unique, we need to consider a hypothetical \( y(t) \) that also satisfies (1) and (2).

Our goal is to show that \( y(t) = x(t) \) for all \( t \geq 0 \). (The domain \( t \geq 0 \) is where we have defined the conditions (1) and (2). Outside of that domain, we don’t have any constraints.

How can we show that two things are equal? In the past, you have probably shown that two quantities or functions are equal by starting with one of them, and then manipulating the expression for it using valid substitutions and simplifications until you get the expression for the other one. However, here, we don’t have an expression for \( y(t) \) so that style of approach won’t work.

In such cases, we basically have a couple of basic ways of showing that two things are the same.

- Take the difference of them, and somehow argue that it is 0.
- Take the ratio of them, and somehow argue that it is 1.

We will follow the ratio approach in this problem. First assume that \( x_0 \neq 0 \). In this case, we are free to define \( z(t) = \frac{y(t)}{x_d(t)} \) since we are dividing by something other than zero.

**What is \( z(0) \)?**

(c) **Take the derivative** \( \frac{d}{dt} z(t) \) **and simplify using (1) and what you know about the derivative of** \( x_d(t) \).

*(HINT: The quotient rule for differentiation might be helpful since a ratio is involved.)*

You should see that this derivative is always 0 and hence \( z(t) \) does not change. **What does that imply for** \( y \) **and** \( x_d \)?

(d) At this point, we have shown uniqueness in most cases. Just one special case is left: \( x_0 = 0 \).

Here, the division approach doesn’t seem to work because we are not permitted to divide by zero and \( x_d(t) = 0 \).

However, we want to show that \( y(t) = 0 \) here as well.

Fundamentally, the argument we want to make is of the “it can’t possibly be otherwise” variety. Consequently, a proof by contradiction can be easier to start.

In such proofs, we start by assuming the thing that we want to show is not possible. So assume that \( y(t) \) is not identically 0 everywhere for \( t > 0 \). What does this mean? This means that there is some \( t_0 > 0 \) for which \( y(t_0) = k \neq 0 \). (Otherwise, it would be zero everywhere.)

We want to create a contradiction. It is clear that we will have no easy contradiction if we just move forward for \( t > t_0 \) because we have no information given about such solutions \( y(t) \) that we can contradict.
What do we know about? We have (2) which says something about \( y(0) \). This means, that we need to somehow move backward in time from \( t_0 \). That way, we can hope to contradict the initial condition of 0.

What do we have to work with? Well, we just did some work in the previous parts establishing uniqueness of solutions assuming nonzero initial conditions. How can we view what happens at \( t_0 \) as a kind of nonzero initial condition?

Apply the change of variables \( t = t_0 - \tau \) to (1) to get a new differential equation for \( \tilde{x}(\tau) = x(t_0 - \tau) \) that specifies how \( \frac{d}{d\tau}\tilde{x}(\tau) \) must relate to \( \tilde{x}(\tau) \). This should hold for \(-\infty < \tau \leq t_0\).

(e) Because the previous part resulted in a differential equation of a form for which we have already proved uniqueness for the case of nonzero initial condition, and since \( \tilde{y}(0) = y(t_0) = k \neq 0 \), we know what \( \tilde{y}(\tau) \) must be. Write the expressions for \( \tilde{y}(\tau) \) for \( \tau \in [0, t_0] \) and what that implies for \( y(t) \) for \( t \in [0, t_0] \).

(f) Evaluate \( y(0) \) and argue that this is a contradiction for the specified initial condition (2).

Consequently, such a \( y(t) \) cannot exist and only the all zero solution is permitted — establishing uniqueness in this case of \( x_0 = 0 \) as well.

Although we gave you lots of guidance in this problem, we hope that you can internalize this way of thinking. This elementary approach to proving the uniqueness of solutions to differential equations works for the kinds of linear differential equations that we will tend to encounter in EE16B. For more complicated nonlinear differential equations, further conditions are required for uniqueness (appropriate continuity and differentiability) and proofs can be found in upper-division mathematics courses on differential equations when you study the Picard-Lindelöf theorem. (It involves looking at the magnitude of the difference of the two hypothetical solutions and showing this has to be arbitrarily small and hence zero. However, the basic elementary case we have established here can be viewed as a building block — the quotient rule gets invoked in the appropriate place, etc. The additional ingredients that are out-of-scope for lower-division courses are fixed-point theorems — which you can think of as more general siblings of the intermediate-value theorem you saw in basic calculus.)

4. IC Power Supply

Digital integrated circuits (ICs) often have very non-uniform current requirements which can cause voltage noise on the supply lines. If one IC is adding a lot of noise to the supply line, it can affect the performance of other ICs that use the same power supply, which can hinder performance of the entire device. For this reason, it is important to take measures to mitigate, or “smooth out”, the power supply noise that each IC creates. A common way of doing this is to add a “supply capacitor” between each IC and the power supply. (If you look at a circuit board, and the supply capacitor is the small capacitor next to each IC.)

Here’s a simple model for a power supply and digital circuit:

![Circuit Diagram]

The current source is modeling the “spiky,” non-uniform nature of digital circuit current consumption. The resistor represents the sum of the source resistance of the supply and any wiring resistance between the supply and the load.
The capacitor is added to try to minimize the noise on $V_{DD}$. Assuming that $V_s = 3V$, $R = 1\Omega$, $i_0 = 1A$, $T=10ns$, and $t_p=1ns$,

(a) Sketch the voltage $V_{DD}$ vs. time for one or two periods $T$ assuming that $C = 0$.
(b) Calculate the total charge consumed in each current spike, and the average current consumption.
(c) Sketch the voltage $V_{DD}$ vs. time for one or two periods $T$ for each of three different capacitor values for $C$: $1pF$, $1nF$, $1\mu F$. ($1pF = 10^{-12}F$, $1nF = 10^{-9}F$, $1\mu F = 10^{-6}F$)

5. CMOS Scaling
Jerry wants to create a new machine learning accelerator chip using CMOS technology. When designing his chip, he considers the most important parameters of his design to be the amount of energy dissipated when the gate transitions, and the delay time it takes for the output of a gate to hit $\frac{V_{DD}}{2}$ from either ground or $V_{DD}$ (i.e. the delay of the gate).
Jerry has access to two different fabrication processes: process A and process B.
Process A uses a supply voltage of $V_{DD} = 1V$. The transistors have a parasitic resistance of $R_p = 10k\Omega$, and the output driven by a representative inverter has a parasitic capacitance of $C_p = 5fF$.
Process B uses a supply voltage of $V_{DD} = 3V$. The transistors have a parasitic resistance of $R_p = 30k\Omega$, and the output driven by a representative inverter has a parasitic capacitance of $C_p = 1fF$.

In order to determine which process is better for the design, Jerry decides to analyze the circuit where the input of an inverter transitions from $V_{DD}$ to 0. This can be modeled as the following circuit:

Since the input of the inverter is transitioning from $V_{DD}$ to 0, the initial condition for $V_c(t)$ is:

\[ V_c(0) = 0 \]

(a) Using the values of $V_{DD}$, $R_p$, and $C_p$ from process A, calculate the total energy delivered by the voltage source, $V_{DD}$, while the capacitor is being charged to $V_{DD}$. Also calculate the time it takes for $V_{out}$ to reach $\frac{V_{DD}}{2}$. 

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(b) Repeat part (a), but with the values from process B.
(c) Compare the energy and delay of process A and B.
(d) Jerry’s friend Pat tells Jerry that with process B, one can reduce $V_{DD}$ to 2V. However, the reduction in supply voltage increases the parasitic resistance $R_p$ to 50kΩ. Calculate the new delay and energy.
(e) Based on your previous answers, which process should Jerry choose to use?

6. NMOS and PMOS Modeling

We talked in lecture about modeling a transistor as a switch plus a resistor. In real devices, the resistance component is very important! This means that the device uses power when it is on because current is dissipating through the device.

Let’s look at the Intel 10 nm FINFET, the industry-leading MOSFET technology from 2017, to see how our model fits a real device.

Intel engineers characterize their devices by measuring the current-voltage relationship when the device is on, giving what’s called an "I-V curve". In this measurement, $V_{GS}$ is held constant at several different values from 0 to 0.7V while $V_{DS}$ is varied. $V_{GS} \geq V_{th}$ for NMOS and $|V_{GS}| \geq |V_{tp}|$ for PMOS in this measurement, so the device is on. The current $I_D$ through the device is measured, and is divided by the gate width $W_{gate}$ so that differently-sized transistors can be compared. The resulting plot reveals many useful parameters of the transistors, including the resistance $R_{on}$ and the threshold voltage $V_t$. 

![NMOS Transistor Resistor-switch model](image1.png)

![PMOS Transistor Resistor-switch model](image2.png)
Another way transistors are evaluated is by examining their behavior when $V_{DS}$ is held constant such that the transistor is off, giving the "Subthreshold Curves". That $V_{DS}$ can control the device in this way is part of a more complex understanding of transistor physics that we do not go into in this class. However, we can still look at some interesting features of this curve. It shows the current that flows through the device even when the device is turned off, which is commonly called the "leakage current".

Reminder: The notation $1E - 04$ is scientific notation for $1 \times 10^{-4}$. Notice also that $I_{D_{\text{gate}}}$ in Figure 3 is in units of mA/µm, while in Figure 4 $I_{D_{\text{gate}}}$ is plotted in log-scale (base 10) and is in units of A/µm.

(a) In the I-V curve in Figure 3, the "linear" region of the device occurs as $|V_{DS}|$ is increased until the curve starts to level off. Estimate the slope of the linear region for both the NMOS and PMOS devices for the $|V_{GS}| = 0.7V$ curve (the top curve). Given that the slope $= \frac{\Delta(I_{D_{\text{gate}}})}{\Delta V}$ and $W_{\text{gate}} = 1$ µm, what is the on-resistance $R_{on}$ for each device?

(b) What power is dissipated in each device when it is on, given these $R_{on}$, if we take $|V_{DS}|$ to be 0.1V?

(c) We can improve our resistor-switch model of the transistor by adding in a gate capacitance. Assume $C = 1$fF.
If this NMOS transistor is connected at the $V_{out}$ terminal to a copy of itself, what is the RC time constant $\tau$ of this stage?

You can assume that the NMOS transistor is just discharging the gate capacitance of another NMOS capacitor in the next stage, just like in the ring oscillator that we drew in class. You can ignore any other devices that might be in the circuit, such as PMOS devices in an inverter. We are just interested in knowing how fast a single NMOS transistor can discharge the capacitance of a copy of itself. This is closely related to the transition frequency of the transistor, which is a common metric used to compare process technologies.

(d) In part (c), what is the maximum frequency at which we can switch the input voltage through one cycle from low ($0\,V$, the transistor is off), to high ($V_{DD}$, the transistor is on), and back to low if we want the output voltage to fully stabilize between each time we change the input voltage? Assume the output voltage fully stabilizes at $7\tau$ seconds after switching the input voltage.

(e) In the subthreshold curve in Figure 4, we can gain some valuable insight about the transistor behavior when the device is off. Estimate the current $I_D$ through the device when $|V_{DS}| = 0.7\,V$ and $|V_{GS}| = 0\,V$, given that $W_{gate} = 1\mu m$. What power is dissipated in this transistor when it is off, given this estimate of $I_D$?

(f) What is the total leakage current and power that is dissipated in a system where there are one billion ($10^9$) NMOS transistors that are off?

(g) **Reflection** It is useful to get exposure to real research so you can see what’s happening in the field! Take a few minutes to look at Intel’s 10nm FINFET paper, attached. It isn’t necessary for you to understand the majority of the article (in fact, many professors who are from other areas probably wouldn’t either!). But we hope that by seeing what research is going on in electrical engineering, you will see that there are many different ways to apply what you’re learning.

Write about something you learned or something that surprised you. (Some suggestions: Figures 2 and 3 have information about scaling; how does this relate to Moore’s Law? Figures 6, 7, and 13 show images of actual devices; how do these compare to your mental model of the devices?)
A 10nm High Performance and Low-Power CMOS Technology Featuring 3rd Generation FinFET Transistors, Self-Aligned Quad Patterning, Contact over Active Gate and Cobalt Local Interconnects


Logic Technology Development, Intel Corporation

ABSTRACT

A 10nm logic technology using 3rd-generation FinFET transistors with a Self-Aligned Quad Patterning (SAQP) for critical patterning layers, and cobalt local interconnects at three local interconnect layers is described. For high density, a novel self-aligned contact over active gate process and elimination of the dummy gate at cell boundaries are introduced. The transistors feature rectangular fins with 7nm fin width and 40nm fin height, 5th generation high-k metal gate, and 7th-generation strained silicon. Four or six workfunction metal stacks are used to enable undoped fins for low Vt, standard Vt and optional high Vt devices. Interconnects feature 12 metal layers with ultra-low-k dielectrics throughout the interconnect stack. The highest drive currents with the highest cell densities are reported for a 10nm technology.

INTRODUCTION

In the past decade, innovations in transistor architecture have accelerated transistor performance from the introduction of strained silicon [1] to high-k/metal-gate [2] to the introduction of multi-gate, FinFET devices [3]. Despite the slowing of lithography scaling, transistor density scaling has accelerated in Intel’s 14nm [4] and 10nm technologies. The traditional node notation has lost its ability to adequately measure the transistor density benefit between technologies. By using a transistor density metric that combines the NAND and scan flip-flop densities (Fig. 1), the acceleration in transistor density starting with a 2.5x scaling at the 14nm generation can be seen. This 10nm technology continues that acceleration at 2.7x from the 14nm generation through use of SAQP w/19nm immersion lithography, improved transistor matching to enable fewer fins in the standard cell library and novel process features to enable tighter layout (Fig. 2).

KEY DESIGN RULES & TECHNOLOGY FEATURES

Table I summarizes the key design rules. Contacted gate pitch is scaled to 54nm and the minimum 6-T SRAM cell size is reduced to 0.0312µm², maintaining traditional scaling trends (Fig. 3). SAQP is introduced at the diffusion, metal-0 and metal-1 layers to achieve tight fin pitches down to 34nm and metal pitches of 36nm with 193nm immersion lithography. Scaling of density critical interconnect layers is up to 0.51x vs. the traditional 0.7x.

To maximize the density scaling at the 10nm generation, several additional architecture features have been added. The first eliminates the dummy gate that has been present at the cell boundaries. By introducing a minimum isolation step at the boundary, the two neighboring cell transistors are isolated by the width of a single gate (Fig. 4).

The next feature is to place the contact to the gate over the active area of the device (Fig. 5). This improves the density by eliminating the need to extend the gate over the isolation to make the contact.

In order to place the gate contact over the active area, both the diffusion contact and gate contacts are formed with a novel self-aligned contact process (Fig. 6). Self-aligned diffusion contacts have been used in high volume manufacturing since the 22nm generation to enable the tight contact to gate overlay requirements. Self-aligned diffusion contacts are formed by recessing the gate metal and then depositing a silicon nitride etch-stop on top of the metal to prevent the diffusion contact from shorting to the gate. With this technology an additional recess of the diffusion contact is added and a silicon carbide etch-stop layer is deposited to prevent the gate contact from shorting to the diffusion contact.

With the aggressive scaling of the contact space, contact resistance (Rext) is a key consideration in optimization of the transistor. In this technology, the contact metal stack has introduced two features to lower the contact resistance. The first is replacing the tungsten contact metal with cobalt. This provides a 60% reduction in contact line resistance. The second is adding a conformal titanium layer to wraparound the source/drain diffusion regions to lower the spreading resistance. A thin NiSi layer has also been added to lower the PMOS contact resistance.

The fin patterning uses SAQP to achieve a 7nm fin width at a 34nm pitch (Fig. 7). In-situ doped, raised S/Ds are used to provide low Rext along with improved mobility from strain enhancement. To balance drive current vs. capacitance,
a fin height of 46nm has been used. A low-k gate spacer has been introduced to reduce the parasitic contact-gate capacitance by 10%. Four or six workfunction metals are used depending on product need. This enables undoped fins for low Vt, standard Vt and optional high Vt devices providing improved mobility, short channel effects and transistor matching for all transistors. The improved transistor matching enables aggressive reduction in fin usage, improving transistor density.

**TRANSISTOR PERFORMANCE AND VARIATION**

The 3rd generation FINFETs show the characteristic steep subthreshold slopes (~70 mV/dec.) and very low DIBL (~70 mV/V) for minimum Lgate devices (Fig. 8). The transistor performance is enhanced by the use of stress enhancement techniques from in-situ doped strained epitaxy in the S/D. A novel ILD0 stress through the gate, orthogonal to the fin, is used to enhance the NMOS drive by an additional 5%. The combination of the stress enhancement along with the contact resistance reduction techniques and the reduced fin pitch leads to a NMOS Idsat of 1.78mA/μm at 0.7V and 10mA/μm (Fig 9). This is an increase of 71% Idsat on NMOS compared to 14nm FINFET transistors. Similarly, NMOS Idlin is 0.475mA/μm, an increase of 100% compared to 14nm FINFET transistors. PMOS shows similar drive current improvements of 35% Idsat and 55% Idlin (Fig. 10). Transistor I-V curves are shown in figure 11.

**RELIABILITY**

Optimization of the high-k + metal-gate stack yields excellent reliability characteristics. Fig. 12 shows NMOS and PMOS TDBB, compared to 14nm. Both show a clear improvement relative to 14nm.

**INTERCONNECTS**

The interconnect stack with 12 layers of interconnect is shown in Fig. 13. Cobalt is introduced at the lowest two interconnect layers providing a 5-10x improvement in electromigration and a 2x reduction in via resistance. SAQP is used at the lowest two metal layers to achieve a 40nm metal-0 pitch and a 36nm metal 1 pitch. Self-aligned Double patterning (SADP) is used at Metal 2-Metal 5 to enable a 44nm metal pitch with scaling of up to 0.51x compared to 14nm. A cobalt cladding layer is utilized at Metal 2 – Metal 5 to improve electromigration. Low-k CDO dielectrics are used on 11 layers.

**SRAM, PRODUCT AND YIELD**

The 10nm yield learning vehicle was a 204Mb SRAM featuring a three SRAM cells, a High Density (HD) 0.0312μm² cell, a Low Voltage (LV) 0.0367μm² cell and a High Performance (HP) 0.0441μm² cell. Yield has been demonstrated on an SRAM test vehicle and on microprocessors.

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**CONCLUSIONS**

This paper presents an industry-leading 10nm CMOS technology with excellent transistor and interconnect performance and aggressive design rule scaling. This is the densest CMOS technology demonstrated to date. The process features 3rd generation FinFETs with optimized fin profiles at 34nm Fin pitch using SAQP and 54nm Gate pitch using SADP. The interconnect stack features self-aligned contacts/vias with a 36nm minimum metal pitch formed with SAQP, cobalt interconnects at critical layers, and aggressive design rule scaling from the 14nm generation. We have shown a high-performance, high-density SRAM featuring 0.0312μm² cell size fabricated using all 10nm process features.

**REFERENCES**


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**Table 1: Layer Pitches**

**Figure 1: Definition of transistor density metric**
Figure 2: Logic Transistor Density Multi-Generation Scaling Trend

Figure 3: SRAM Scaling Trend

Figure 4: Dummy Gate elimination layout comparison

Figure 5: Contact over active gate layout comparison

Figure 6: Self-aligned Diffusion and Gate contact images (not same scale)

Figure 7: Transistor Fin and Gate-Cut Images (not same scale)
7. Write Your Own Question And Provide a Thorough Solution.

Writing your own problems is a very important way to really learn material. The famous “Bloom’s Taxonomy” that lists the levels of learning is: Remember, Understand, Apply, Analyze, Evaluate, and Create. Using what you know to create is the top level. We rarely ask you any homework questions about the lowest level of straight-up remembering, expecting you to be able to do that yourself (e.g. making flashcards). But we don’t want the same to be true about the highest level. As a practical matter, having some practice at trying to create problems helps you study for exams much better than simply counting on solving existing practice problems. This is because thinking about how to create an interesting problem forces you to really look at the material from the perspective of those who are going to create the exams. Besides, this is fun. If you want to make a boring problem, go ahead. That is your prerogative. But it is more fun to really engage with the material, discover something interesting, and then come up with a problem that walks others down a journey that lets them share your discovery. You don’t have to achieve this every week. But unless you try every week, it probably won’t ever happen.

8. Homework Process and Study Group

Citing sources and collaborators are an important part of life, including being a student! We also want to understand what resources you find helpful and how much time homework is taking, so we can change things in the future if possible.

(a) What sources (if any) did you use as you worked through the homework?
(b) Who did you work on this homework with? List names and student ID’s. (In case of homework party, you can also just describe the group.)
(c) How did you work on this homework? (For example, I first worked by myself for 2 hours, but got stuck on problem 3, so I went to office hours. Then I went to homework party for a few hours, where I finished the homework.)
(d) Roughly how many total hours did you work on this homework?

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