1. Op-Amp Review

Consider the circuit below:

(a) Write down all branch and node equations using KCL and the Golden Rules of op-amps.

**Solution:**

For an op-amp in negative feedback, the Golden Rules are (1) the voltage difference between the two inputs is zero \( V^+ = V^- \), and (2) no current goes into the inputs of an op-amp.

Let’s label the unknown nodes in this circuit as nodes \( a \) through \( f \) and branch currents \( I_1 \) to \( I_7 \). Here, we apply second Golden Rule to have all input currents of op-amps as 0. See the following figure:
According to the first Golden Rule, we can write down:

\[ V_a = V_p \]
\[ V_b = V_n \]
\[ V_e = V_f \]

Then we write down the node current equations based on Kirchhoff’s Current Law (KCL) (the sum of total currents flowing into one node is the same as the sum of currents flowing out of that same node.):

\[ I_1 = I_2 \implies \frac{V_c - V_p}{R_2} = \frac{V_a - V_b}{R_1} = \frac{V_p - V_n}{R_1} \]
\[ I_2 = I_3 \implies \frac{V_a - V_b}{R_1} = \frac{V_p - V_n}{R_1} = \frac{V_n - V_d}{R_2} \]
\[ I_4 = I_5 \implies \frac{V_d - V_f}{R_3} = \frac{V_f}{R_4} \]
\[ I_6 = I_7 \implies \frac{V_e - V_c}{R_3} = \frac{V_{out} - V_e}{R_4} \]

You can define currents in whichever directions you like, but you should arrive at the same conclusion that \(|I_1| = |I_2| = |I_3|\).

(b) Notice that there exists a symmetry between the two op-amps at the first stage of this circuit. What are the directions of the currents going through the two \(R_2\)’s? How do the currents of \(R_2\)’s influence the current through \(R_1\)?

**Solution:**

According to the branch current equations: \( I_1 = I_2 \) and \( I_2 = I_3 \), so the currents going through the two \(R_2\)’s are the same but with opposite directions: one is from the output of the op-amp to the inverting input, while the other is from the inverting input to the output. The current through \(R_1\) is the same as the current through the \(R_2\)’s.
(c) What is the current through $R_1$?

**Solution:**

The current through $R_1$ is $I_2 = \frac{V_p - V_n}{R_1}$. If $V_p - V_n$ is negative, the current will flow in the opposite direction of what is drawn in the diagram.

(d) What are the output voltages of the two op-amps at the first stage?

**Solution:**

For the upper op-amp, $V_c = V_a + I_1 R_2$, where $I_1 = \frac{V_p - V_n}{R_1}$, and $V_a = V_p$. Therefore, the output voltage $V_c$ of the upper op-amp is $V_p + \frac{V_p - V_n}{R_1} R_2$.

For the lower op-amp, $V_d = V_b - I_3 R_2$, where $I_3 = \frac{V_p - V_n}{R_1}$, and $V_b = V_n$. Therefore, the output voltage $V_d$ of the lower op-amp is $V_n - \frac{V_p - V_n}{R_1} R_2$.

(e) Compute the voltage at the $+$ terminal of the second-stage op-amp.

**Solution:** From part (a), we know that $(V_d - V_f) R_3 = V_f R_4$. Hence, we could express $V_f$ with $V_d$ as follows:

$$V_f = \frac{R_4}{R_3 + R_4} V_d$$

and plug in the value of $V_d$ we computed in (d), $V_d = V_n - \frac{V_p - V_n}{R_1} R_2$:

$$V_f = \frac{R_4}{R_3 + R_4} \left( V_n - \frac{V_p - V_n}{R_1} R_2 \right)$$

(f) What is $V_{\text{out}}$?

**Solution:**

There are two ways to compute $V_{\text{out}}$: (1) use all known values to derive the answer, or (2) start with $V_c$ and $V_d$ as inputs (free variables) first, and then plug in the values of $V_c$ and $V_d$ in the end of computation. Here we will show you (1), and in part (h), you will see (2).

From part (a) (Golden Rules), we know that $V_e = V_f$, and from part (e), we derived $V_f = \frac{R_4}{R_3 + R_4} \left( V_n - \frac{V_p - V_n}{R_1} R_2 \right)$.

Also, from part (d), we showed that $V_c = V_p + \frac{V_p - V_n}{R_1} R_2$.

From part (a), we know that $\frac{V_p - V_c}{R_3} = \frac{V_{\text{out}} - V_p}{R_2}$. We can express $V_{\text{out}}$ in terms of $V_c$ and $V_e$:

$$V_{\text{out}} = \left( 1 + \frac{R_4}{R_3} \right) V_e - \frac{R_4}{R_3} V_c$$

After plugging in the values for $V_c$ and $V_e$, we get $V_{\text{out}}$:

$$V_{\text{out}} = \left( 1 + \frac{R_4}{R_3} \right) \frac{R_4}{R_3 + R_4} \left( V_n - \frac{V_p - V_n}{R_1} R_2 \right) - \frac{R_4}{R_3} \left( V_p + \frac{V_p - V_n}{R_1} R_2 \right)$$

$$= \frac{R_4}{R_3} \left( V_n - V_p - \frac{2 R_2 (V_p - V_n)}{R_1} \right)$$

$$= \left( V_n - V_p \right) \frac{R_4}{R_3} \left( 1 + \frac{2 R_2}{R_1} \right)$$
(g) If we broke $R_1$ into two series resistors, each with a resistance of $\frac{R_1}{4}$, what is the voltage at the node in between these resistors?

**Solution:**
The voltage across the resistor $R_1$ is $V_p - V_n$, and the current flowing through $R_1$ is $$\frac{(V_p - V_n)}{R_1}.$$ The voltage in the middle is $$V_p - \frac{R_1}{2} \frac{(V_p - V_n)}{R_1} = \frac{V_p + V_n}{2}.$$ In other words, it is the average of $V_p$ and $V_n$.

(h) Based on the above analysis, if $V_p = -V_n$, we could introduce a “fake ground” in the middle of the resistor $R_1$ and come up with the following circuit:

![Circuit Diagram](image)

Now, each of the first two op-amps is being used in a form that resembles building blocks that you have seen before. What are the gains of those blocks?

What is $\frac{V_{out}}{V_p - V_n}$ for this revised circuit?

**Solution:**
Usually, we have the DC voltage inputs of $V_p$ and $V_n$ as $V_p = -V_n$. Hence, the voltage in the middle of $R_1$ is 0. That’s why we introduce a fake ground here.

Let’s focus on the two op-amps in the first stage: they are exactly the same, except the input voltages. According to the golden rules, the voltage at the $-$ terminal must be the same as at the $+$ terminal. $R_2$
and $\frac{R_1}{2}$ here are forming voltage dividers for the output voltage of each op-amp. Hence, the gains of the two op-amps are $1 + \frac{2R_2}{R_1}$.

Then, let’s take a look at the op-amp in the second stage. Suppose the two inputs for the whole block are $V_c$ and $V_d$, as we used before. Recall that $V_e$ and $V_f$ must be the same (two inputs of the op-amp).

We have derived $V_e = V_f = \frac{R_4}{R_3 + R_1} V_d$ in part (e), and we know that $V_{out} = \left(1 + \frac{R_4}{R_3}\right) V_e - \frac{R_4}{R_3} V_c$. Replace $V_e$ with $\frac{R_4}{R_3 + R_1} V_d$, and we conclude that

$$V_{out} = \frac{R_4}{R_3} (V_d - V_c).$$

Hence, the gain of the third block in $\frac{R_4}{R_3}$.

Combining the above results, we have $V_{out} = \frac{R_4}{R_3} (V_d - V_c)$, where $V_c = \left(1 + \frac{2R_2}{R_1}\right) V_p$ and $V_d = \left(1 + \frac{2R_2}{R_1}\right) V_n$. The overall gain is

$$\frac{V_{out}}{(V_p - V_n)} = -\frac{R_4}{R_3} \left(1 + \frac{2R_2}{R_1}\right).$$

(Check the positions of $V_p$ and $V_n$.)

This entire circuit is called an instrumentation amplifier, which is the descendant of a combo of two unity gain amplifiers followed by a differential amplifier.

2. KVL

Consider the circuit shown below:

![Circuit Diagram](Figure 1: Adapted from Ulaby, Maharbiz, Furse. *Circuits*. Third Edition.)

Using KVL, determine the amount of power supplied by the voltage source. Do not use superposition.

**Solution:**

We will label the currents $I_1$, $I_2$, and $I_3$ as shown in the following diagram.

![Circuit Diagram](Figure 1: Adapted from Ulaby, Maharbiz, Furse. *Circuits*. Third Edition.)

$$\begin{align*}
\text{Loop 1:} & \quad I_1 = 9 \text{ A} \\
\text{Loop 2:} & \quad 3(I_2 - I_1) + 8(I_2 - I_3) = 0 \\
\text{Loop 3:} & \quad 8(I_3 - I_2) + 8I_3 + 40 = 0
\end{align*}$$
Simplification leads to:

\[
\begin{align*}
11I_2 - 8I_3 &= 27 \\
-8I_2 + 16I_3 &= -40
\end{align*}
\]

Solving this system of equations gives:

\[I_2 = 1 \text{ A} \quad I_3 = -2 \text{ A}\]

The power supplied by the voltage source is:

\[P = VI = 40 \cdot (-2) = -80 \text{ W}\]

3. KCL

Consider the circuit shown below:

\[\begin{array}{c}
15 \text{ V} \\
\downarrow \\
5 \Omega \\
\downarrow \\
10 \Omega \\
\downarrow \\
2V_x \\
\downarrow \\
5 \Omega \\
\downarrow \\
2 \mu \text{F} \\
\end{array}\]

Figure 2: Adapted from Ulaby, Maharbiz, Furse. *Circuits.* Third Edition

Determine the voltage \(V_x\) at steady state.

**Solution:**

At steady state, there is no current flowing through the capacitor.

In terms of the node voltage \(V_x\), KCL gives

\[
\frac{V_x - 15}{5} + \frac{V_x}{10} - 2V_x + \frac{V_x}{5} = 0,
\]

whose solution leads to

\[V_x = -2 \text{ V}.
\]

4. Transistors and Boolean Logic

A boolean formula can be implemented in digital circuitry using nMOS and pMOS transistors. In circuits, the truth value 1 (true) is represented by a high voltage, called POWER (\(V_{\text{DD}}\)). The truth value 0 (false) is represented by a low voltage, called GROUND (GND). In this problem, we will only use the truth values in order to simplify notations. That is, if you see \(A = 1\) for a point \(A\), then it means the voltage of \(A\) is equal to \(V_{\text{DD}}\). Similarly, if \(A = 0\), then the voltage of \(A\) is equal to GND.

An inverter can be implemented with 1 nMOS and 1 pMOS, as shown in the figure below. When the input \(A\) is 0, then the nMOS is OFF and the pMOS is ON. Thus, the output \(Y\) is pulled up to 1 because it is connected to \(V_{\text{DD}}\). Conversely, when \(A\) is 1, then the nMOS is ON and the pMOS is OFF, and \(Y\) is pulled down to 0. Therefore, the circuit implements the Boolean formula, \(Y = \overline{A}\).
In general, a Boolean-formula circuit has an nMOS pull-down network to connect the output to 0 (GND) and a pMOS pull-up network to connect the output to 1 (V\text{DD}). The pull-up and pull-down networks in the inverter example each consist of a single transistor.

In this problem, you will design pull-up networks given the pull-down networks.

(a) The pull-down network of the Boolean formula (a 2-input NAND gate), \( Y = (A \cdot B) \), is given below.

Design the pull-up network (the dashed box) with 2 pMOS transistors.

Solution:
From De Morgan’s laws, we have \( Y = \overline{A + \overline{B}} \), which means that when \( A = 0 \) or \( B = 0 \), \( Y \) should be pulled up to 1. Therefore, we connect two pMOS transistors in parallel in the pull-up network.
(b) The pull-down network of the Boolean formula (a 2-input NOR gate), \( Y = (A + B) \), is given below. Design the pull-up network (the dashed box) with 2 pMOS transistors.

Solution:
From De Morgan’s laws, we have \( Y = \overline{A \cdot B} \), which means that when \( A = 0 \) and \( B = 0 \), \( Y \) should be pulled up to 1. Therefore, we connect two pMOS transistors in series in the pull-up network.
(c) The pull-down network of the Boolean formula, \( Y = (A \cdot B + C) \), is given below. Design the pull-up network (the dashed box) with 3 pMOS transistors.

Solution:
Let \( Z = \overline{A} + \overline{B} \). From De Morgan’s laws, we have \( Y = (\overline{A} + \overline{B}) \cdot \overline{C} = Z \cdot \overline{C} \), which means that when \( Z = 1 \) and \( C = 0 \), \( Y \) should be pulled up to 1. For \( Z \), we connect 2 pMOS transistors in parallel as in part (a). Then, we connect the two pMOS transistors of \( Z \) and the one pMOS transistor of \( C \) in series in the pull-up network.
(d) The pull-down network of the Boolean formula, \( Y = (A + B) \cdot C \), is given below. Design the pull-up network (the dashed box) with 3 pMOS transistors.

Solution:
Let \( Z = \overline{A} \cdot \overline{B} \). From De Morgan’s laws, we have \( Y = (A \cdot B) + \overline{C} = Z + \overline{C} \), which means that when \( Z = 1 \) or \( C = 0 \), \( Y \) should be pulled up to 1. For \( Z \), we connect 2 pMOS transistors in series as in part (b). Then, we connect the two pMOS transistors of \( Z \) and the one pMOS transistor of \( C \) in parallel in the pull-up network.
(e) You have designed four pull-up networks. What can you conclude about the rules for designing pull-up networks when pull-down networks are given?

**Solution:**

The pull-up network is the complement of the pull-down network. Series connections of transistors are changed to parallel connections, and vice versa.

Recall that the reason that we design things this way is to prevent power from being burned unnecessarily when the logical state is not changing. With this complementary configuration, either the top or bottom network will be an open circuit. There will never be a path connecting $V_{DD}$ to ground.

(f) For the circuit below, write the truth table for inputs A and B with output Y. What boolean operation is this?

Note some of the gate voltages are $\overline{A}$ and $\overline{B}$. 
Solution:
In CMOS, if the gate of an nMOS is 1, the switch is closed and acts as a resistor. If the gate voltage is 0, then it acts as an open. The opposite is true for pMOS.
To get the truth table, draw the circuit for each input case and see whether the output is connected to ground or $V_{DD}$.
This is what the circuit should look like for $A = 0, B = 0$: 
Y is connected to ground through resistors, so for the input combination $A = 0, B = 0, Y = 0$. Repeat this for the 3 other cases and you will get the following truth table:

<table>
<thead>
<tr>
<th>$A$</th>
<th>$B$</th>
<th>$Y$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

This circuit is an XOR gate ($A \oplus B$).

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