1. Op-Amp Review

Consider the circuit below:

(a) Write down all branch and node equations using KCL and the Golden Rules of op-amps.

(b) Notice that there exists a symmetry between the two op-amps at the first stage of this circuit. What are the directions of the currents going through the two \( R_2 \)'s? How do the currents of \( R_2 \)'s influence the current through \( R_1 \)?

(c) What is the current through \( R_1 \)?

(d) What are the output voltages of the two op-amps at the first stage?

(e) Compute the voltage at the + terminal of the second-stage op-amp.

(f) What is \( V_{out} \)?

(g) If we broke \( R_1 \) into two series resistors, each with a resistance of \( \frac{R}{2} \), what is the voltage at the node in between these resistors?

(h) Based on the above analysis, if \( V_p = -V_n \), we could introduce a “fake ground” in the middle of the resistor \( R_1 \) and come up with the following circuit:
Now, each of the first two op-amps is being used in a form that resembles building blocks that you have seen before. What are the gains of those blocks? What is $V_{out}$ for this revised circuit?

2. **KVL**

Consider the circuit shown below:

![Circuit Diagram](Figure 1: Adapted from Ulaby, Maharbiz, Furse. Circuits. Third Edition.)

Using KVL, determine the amount of power supplied by the voltage source. Do not use superposition.

3. **KCL**

Consider the circuit shown below:
Determine the voltage $V_x$ at steady state.

4. Transistors and Boolean Logic

A boolean formula can be implemented in digital circuitry using nMOS and pMOS transistors. In circuits, the truth value 1 (true) is represented by a high voltage, called POWER ($V_{DD}$). The truth value 0 (false) is represented by a low voltage, called GROUND (GND). In this problem, we will only use the truth values in order to simplify notations. That is, if you see $A = 1$ for a point $A$, then it means the voltage of $A$ is equal to $V_{DD}$. Similarly, if $A = 0$, then the voltage of $A$ is equal to GND.

An inverter can be implemented with 1 nMOS and 1 pMOS, as shown in the figure below. When the input $A$ is 0, then the nMOS is OFF and the pMOS is ON. Thus, the output $Y$ is pulled up to 1 because it is connected to $V_{DD}$. Conversely, when $A$ is 1, then the nMOS is ON and the pMOS is OFF, and $Y$ is pulled down to 0. Therefore, the circuit implements the Boolean formula, $Y = \overline{A}$.

In general, a Boolean-formula circuit has an nMOS pull-down network to connect the output to 0 (GND) and a pMOS pull-up network to connect the output to 1 ($V_{DD}$). The pull-up and pull-down networks in the inverter example each consist of a single transistor.

In this problem, you will design pull-up networks given the pull-down networks.

(a) The pull-down network of the Boolean formula (a 2-input NAND gate), $Y = (A \cdot B)$, is given below. Design the pull-up network (the dashed box) with 2 pMOS transistors.
(b) The pull-down network of the Boolean formula (a 2-input NOR gate), \( Y = \overline{A + B} \), is given below. Design the pull-up network (the dashed box) with 2 pMOS transistors.

(c) The pull-down network of the Boolean formula, \( Y = \overline{(A \cdot B) + C} \), is given below. Design the pull-up network (the dashed box) with 3 pMOS transistors.
(d) The pull-down network of the Boolean formula, \( Y = (A + B) \cdot C \), is given below. Design the pull-up network (the dashed box) with 3 pMOS transistors.

![Diagram of pull-down network](image)

(e) You have designed four pull-up networks. What can you conclude about the rules for designing pull-up networks when pull-down networks are given?

(f) For the circuit below, write the truth table for inputs A and B with output Y. What boolean operation is this?

Note some of the gate voltages are \( \overline{A} \) and \( \overline{B} \).

![Diagram of another circuit](image)

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