This homework is due September 5, 2017, at 11:59AM.

1. Fundamental Theorem of Solutions to Differential Equations

In this question, you will discover the power of the fundamental theorem of solutions to differential equations. For convenience, we shall restate the theorem here.

**Theorem.** Consider a differential equation of the form,

\[ \frac{d^n y}{dt^n}(t) + \alpha_{n-1} \frac{d^{n-1} y}{dt^{n-1}}(t) + \ldots + \alpha_1 \frac{dy}{dt}(t) + \alpha_0 y(t) = 0 \]

Given \( n \) initial conditions of the form,

\[ y(t_0) = a_0, \frac{dy}{dt}(t_0) = a_1, \ldots, \frac{d^{n-1} y}{dt^{n-1}}(t_0) = a_{n-1}, \]

there exists a unique solution (say, \( f \)).

(a) Consider the following 2 functions.

\[ \phi_1(x) = e^x, \phi_2(x) = \sum_{n=0}^{\infty} \frac{x^n}{n!} \]

Prove that \( \phi_1(x) = \phi_2(x) \) by showing that both functions satisfy the following differential equation:

\[ \frac{df}{dx}(x) = f(x) \text{ with } f(0) = 1 \]

*Side note:* Assume \( 0^0 = 1 \).

(b) Consider the following 2 functions.

\[ \phi_1(x) = \cos(x), \phi_2(x) = \cos(-x) \]

Prove that \( \phi_1(x) = \phi_2(x) \) by showing that both functions satisfy the following differential equation:

\[ \frac{d^2 f}{dx^2}(x) = -f(x) \text{ with } f(0) = 1, \frac{df}{dx}(0) = 0 \]

2. Transistors and Boolean Logic

A Boolean formula can be implemented in digital circuitry using nMOS and pMOS transistors. In circuits, the truth value 1 (true) is represented by a high voltage, called POWER (\( V_{DD} \)). The truth value 0 (false) is represented by a low voltage, called GROUND (GND). In this problem, we will only use the truth values in
order to simplify notations. That is, if you see $A = 1$ for a point $A$, then it means the voltage of $A$ is equal to $V_{DD}$. Similarly, if $A = 0$, then the voltage of $A$ is equal to GND.

An inverter can be implemented with 1 nMOS and 1 pMOS, as shown in the figure below. When the input $A$ is 0, then the nMOS is OFF and the pMOS is ON. Thus, the output $Y$ is pulled up to 1 because it is connected to $V_{DD}$. Conversely, when $A$ is 1, then the nMOS is ON and the pMOS is OFF, and $Y$ is pulled down to 0. Therefore, the circuit implements the Boolean formula, $Y = \overline{A}$.

In general, a Boolean-formula circuit has an nMOS pull-down network to connect the output to 0 (GND) and a pMOS pull-up network to connect the output to 1 ($V_{DD}$). The pull-up and pull-down networks in the inverter example each consist of a single transistor.

In this problem, we will ask you to design pull-up networks when pull-down networks are given.

(a) The pull-down network of the Boolean formula (a 2-input NAND gate), $Y = (A \cdot B)$, is given below. Design the pull-up network (the dashed box) with 2 pMOS transistors.

(b) The pull-down network of the Boolean formula (a 2-input NOR gate), $Y = (A + B)$, is given below. Design the pull-up network (the dashed box) with 2 pMOS transistors.
(c) The pull-down network of the Boolean formula, $Y = (A \cdot B) + C$, is given below. Design the pull-up network (the dashed box) with 3 pMOS transistors.

(d) The pull-down network of the Boolean formula, $Y = (A + B) \cdot C$, is given below. Design the pull-up network (the dashed box) with 3 pMOS transistors.
(e) You have designed four pull-up networks. What can you conclude about the rules for designing pull-up networks when pull-down networks are given?

(f) For the circuit below, write the truth table for inputs A and B with output Y. What boolean operation is this?

Note some of the gate voltages are \( \overline{A} \) and \( \overline{B} \)

3. RC Circuit

Consider the circuit below, assume that when \( t \leq 0 \), the capacitor has no charge stored (\( V_c(t = 0) = 0 \)). At \( t = 0 \), the switch closes. Assume \( V_s = 15 \) V, \( R = 500 \Omega \), and \( C = 100 \mu F \).
Figure 1: RC Circuit with Voltage Source

(a) What are the boundary conditions for \( I_c(t) \) (i.e. what is \( I_c(t = 0) \) and \( I_c(t \to \infty) \)?)

(b) Use KVL and the relationship between charge and current (\( q = \int I dt \)) to find the first order differential equation in terms of the current through the capacitor, \( I_c \). Assume \( \frac{dV_s}{dt} = 0 \) (Hint: you will need to take a derivative with respect to time to get the equation)

(c) What is the eigenvalue \( \lambda \) of this equation?

(d) Using the eigenvalue and boundary conditions found in previous parts, find an expression for \( I_c(t) \) in terms of \( V_s, R \) and \( C \)

(e) What order of magnitude of time (nanoseconds, milliseconds, 10’s of seconds, etc.) does this circuit settle (\( I_c \) is <5% of it’s initial value)?

(f) Give 2 ways to reduce the settling time of the circuit if we are allowed to change one component in the circuit.

(g) Sketch the current vs time plot of \( I_c(t) \) Make sure to label \( I_c(t) \) at \( t = 0, t = \tau, t = 2\tau, \) and \( t = 3\tau \)

4. From Transistors to Inverter

The following circuit is an inverter built with one pMOS and one nMOS transistor. We assume \( V_{out} \) is connected to the input of another identical inverter (not shown). We also assume there is a capacitance connected between \( V_{out} \) and GND. In real transistors, this capacitance arises from a combination of capacitances contributed by the transistors of both the inverter in question and any inverters connected to the output. For the moment, we’ll just call this capacitance \( C_L \) (for load). The resistances associated with the pMOS and nMOS are \( R_{onP} \) and \( R_{onN} \), respectively. Let the threshold voltage of the pMOS be \( V_{tp} \), while that for the nMOS be \( V_{tn} \). We will now model the action of the inverter as an RC circuit with two switches controlled by \( V_{in} \) as what we did in lectures.

(a) For starters, what are the on-off conditions of the two switches? Please draw the RC circuit modeling this inverter.
(b) Assume $V_{in} = V_{DD}$ for $t < 0$, and $V_{in} = 0$ for $t \geq 0$. In other words, we are assuming the input to our inverter can switch states infinitely fast (this is not true in real life, but gives us a good lower bound on how fast an inverter can switch). How much energy does it take to fully charge $C_L$?

(c) Given the same condition as in (b), write down the differential equation that describes $V_{out}(t)$ for $t \geq 0$.

(d) What is the solution to this differential equation? Plot $V_{out}(t)$ for $t > 0$.

(e) The term propagation delay is used to describe the amount of time it takes between when the input reaches $V_{DD}/2$ and when the output reaches $V_{DD}$. Calculate the propagation delay for our inverter above (keep in mind that the input to our inverter changes instantly). Is propagation delay a function of $V_{DD}$?

(f) Now consider a serial chain of inverters, each driving the one before it. If we assume that $|V_{in}| = |V_{tp}| = V_{DD}/2$ what is the propagation delay for one of these inverters, given (d) and (e)? (If you like, ignore the first inverter and assume it is driven by an input as in (a)). Here we let $R_{onP} = R_{onN} = R$.

(g) Now let’s consider the following scenario: there are $N$ inverters on the chip in your cell phone. It takes $E$ Joules of energy to charge all of the inverters at once (from zero to $V_{DD}$). What is the value of $C_L$?

(h) Here we interpret a voltage $V$ as logic "1" when $V > V_{DD}/2$, and logic "0" when $V < V_{DD}/2$. Let’s assume the maximum frequency, $f$, at which an inverter can switch back and forth between logic "0" and logic "1" at the output is the inverse of the propagation delay (i.e. we can only switch as fast as one propagation delay). Find an expression that links $f$, $C_L$, and $R$.

5. Digital-analog converter

A digital-analog converter (DAC) is a circuit for converting a digital representation of a number (binary) into a corresponding analog voltage. In this problem, we will consider a DAC made out of resistors only (resistive DAC) called the R-2R ladder. Here is the circuit for a 3-bit resistive DAC.

Let $b_0, b_1, b_2 = \{0, 1\}$ (that is, either 1 or 0), and let the voltage sources $V_0 = b_0V_{DD}$, $V_1 = b_1V_{DD}$, $V_2 = b_2V_{DD}$, where $V_{DD}$ is the supply voltage.
As you may have noticed, \((b_2, b_1, b_0)\) represents a 3-bit binary (unsigned) number where each of \(b_i\) is a binary bit. We will now analyze how this converter functions.

(a) If \(b_2, b_1, b_0 = 0, 0, 1\), what is \(V_{\text{out}}\)? Express your answer in terms of \(V_{\text{DD}}\).

(b) If \(b_2, b_1, b_0 = 0, 1, 0\), what is \(V_{\text{out}}\)? Express your answer in terms of \(V_{\text{DD}}\).

(c) If \(b_2, b_1, b_0 = 1, 1, 1\), what is \(V_{\text{out}}\)? Express your answer in terms of \(V_{\text{DD}}\).

(d) If \(b_2, b_1, b_0 = 1, 0, 0\), what is \(V_{\text{out}}\)? Express your answer in terms of \(V_{\text{DD}}\).

(e) Finally, solve for \(V_{\text{out}}\) in terms of \(V_{\text{DD}}\) and the binary bits \(b_2, b_1, b_0\).

(f) Explain how your results above show that the resistive DAC converts the 3-bit binary number \((b_2, b_1, b_0)\) to the output analog voltage \(V_{\text{DD}}\).

Contributors:

- Siddharth Iyer.
- Yen-Sheng Ho.
- Kyle Tanghe.
- Yu-Yun Dai.
- Edward Wang.