Nonplanar Metallization

Planar Metallization
"Caps" and "Plugs"

The plug material can be same as interconnect material (e.g. Cu) or different material (e.g. W)

Figure 13.22 The use of caps versus plug-filled contacts.
Non-Optimized Planarization example

THREE LEVEL METALLIZATION FROM COMPANY A
W plugs for contacts, via 1 and via 2
Al/TiN/Ti/TiN for metal 1 and 2; Al alloy for metal 3
CMP for IM0 1 and IM02.
Good Planarization Example

Five Level Metallization for Company C
W plugs for contacts and vias
W for metal 1, Al/Ti metal 2,3, 4; Al metal 3
CMP for all dielectrics.
Surface Planarization

Benefits for Lithography Processes:
• Lower Depth-of-Focus requirement
• Reduced optical reflection effects on resist profiles
• Reduced resist thickness variation over steps

Benefit for Etching Processes:
• Reduced over-etch time required due to steps

Benefit for Deposition Processes:
• Improved step coverage for subsequent layer deposition
Planarization Factor $\beta$

$\beta = 1 - \frac{\text{final step height}}{\text{initial step height}}$

- **No Planarization**
  - $t_{\text{step}}$
  - $\beta = 0$

- **Smoothing only**
  - $t_{\text{step}}$
  - $\beta = 0$

- **Smoothing and partial planarization**
  - $t_{\text{step}}$
  - $0 < \beta < 1$

- **Complete Local Planarization**

- **Complete Global Planarization**
  - $t_{\text{step}} = 0$
  - $\beta = 1$ everywhere
Planarization: A bad example

- Topography management must start at lower layers!
Planarization Techniques

1. Spin-on glass or polyimide
2. Deposit and Etchback
3. Chemical-Mechanical Polishing (CMP)
Spin-On Glass (SOG)

A: SOG STANDALONE

B: CVD/SOG COMPOSITE

C: CVD/SOG/CVD COMPOSITE WITH PARTIAL SOG ETCH-BACK
SOG Annealing

- **Cure:**
  - 400-500°C -> inorganic backbone polymer
    - exact composition depends on SOG type
  - 800-1100°C -> densified glass (inorganic SOGs)
  - can be performed in N₂, O₂ or steam
    - steam allows densification to occur at lower temperatures
Polyimides

Polymers:

- excellent thermal stability (up to 450°C)
- good dielectric properties \((\varepsilon_r=3.3, \rho=10^{16} \ \Omega\text{-cm})\)
- superior chemical resistance
Deposit and Etchback

1. Deposit thick oxide layer (600 - 1000nm)

2. Spin on resist or polymer to planarize surface

3. Etch back with a process that has equal oxide and resist/polymer etch rates (e.g. CF$_4$ + O$_2$ dry etch)

(4. Deposit second oxide layer)

- Simple process, requiring equipment and materials already available in the lab
Chemical Mechanical Polishing (CMP)

Wafer is polished using a slurry containing
• silica abrasives (10-90 nm particle size)
• etching agents (e.g. dilute HF)

• Backing film provides elasticity between carrier and wafer

• Polishing pad made of polyurethane, with 1 mm perforations – rough surface to hold slurry
CMP Configurations

Rotating wafer
Rotating pad

Rotating Wafer
Linear track pad
CMP Process Control

- Particle size
- pH
- Concentration
- Type of slurry
- Depth of wafer in carrier
- Slurry feed speed
- Slurry
- Polishing force
- Temperature
- Carrier rotational speed
- Plate rotational speed
- Backforce
- Conditioning method
- Conditioning speed
- Pad Hardness
- Type of pad
- CMP
- Removal
- Polishing rate
- Uniformity
- Planarization Selectivity
- in-situ Profilemeter
- EPD
Preston Model:

Local Removal rate \( R = K_p \, P \, v \)

where \( P \) = local applied pressure
\( v \) = relative pad-wafer velocity
\( K_p \) = Preston coefficient [unit in pressure\(^{-1}\)]

function of film hardness, Young’s modulus, slurry, pad composition and structure
CMP Selectivity of \( \text{Si}_3\text{N}_4 \)
Problems encountered in CMP

- Non uniformity
- Rounding
- Dishing

Fig. 6. Mechanical model (with exaggerated pad bending).
Pattern Dependence of CMP

- High isolated features polish fast
- Increased pressure at corners of features creates rounding

*Note: Y-axis highly magnified!!!
Figure 12. End-point detection using wafer carrier motor current (source 20).
Figure 13. Diagram of a IR sensor embedded into the wafer carrier (left). Description of IR interferometry using the IR sensor (right) (source 20).
CMP Application Example

RIE of Cu difficult due to low vapor pressure of by-products

=> Cu lines formed by CMP

Cu has to be encapsulated by a liner (e.g. TiN) to prevent out-diffusion into SiO2 and Si

Figure 2. Schematics of the inlaid Cu produced by chemical-mechanical polishing (CMP): (a) shows a depositedCu/Ti on patterned dielectric, (b) the same after CMP and stopping at Ti.
Single Damascene Process

ILD = Inter-Level Dielectric

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Dual Damascene Cu Metallization with Diffusion Barrier
Dual Damascene process flow (a) An insulator sandwich is first deposited and the upper nitride layer is patterned. The insulator layer is etched. The etch terminates on the silicon nitride etch stop. (b) The nitride layer is patterned and etched. (c) Following the next oxide etch step, two different width openings exist in the two oxide layers. (d) Barrier and seed layers are deposited and plated with copper. (e) Final structure following removal of excess copper.
Aspect Ratio \((T/W) = 1.6/1\)

6 Layers of Damascene Copper