N.CHEUNG **EE143, Sp 2009**

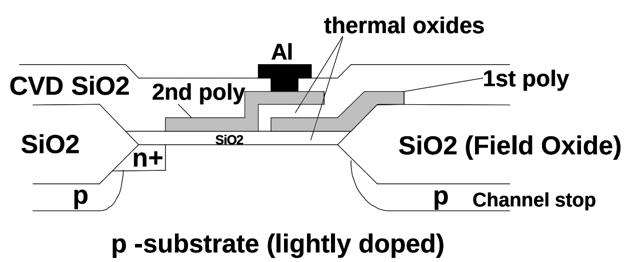
Homework Assignment # 10 (Due April 13, 8am)

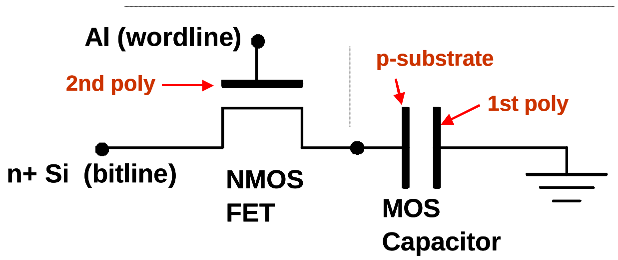
Reading Assignment
1)EE143 Lecture Notes on Process Integration
2) Jaeger, pp.221-228 on CMOS integration
OPTIONAL Reading : EE143 Reader, John Chen , Chapter 5, " CMOS Process Technology". This Chapter describes processing of more advanced MOS structures.

In this homework assignment, we will practice designing process flows based on planar technology. You have to draw cross-sections of the devices at major processing steps.

Problem 1 Double Poly DRAM

Design a process flow for the following double poly-Si NMOS dynamic random access memory (DRAM) element. Note that 1st poly and 2nd poly are separated a very thin layer of thermal oxide. A standard NMOS process is used with LOCOS to form the field oxide. Enter the process description under the first column and a sketch of the cross-section after critical process steps under the Second column.

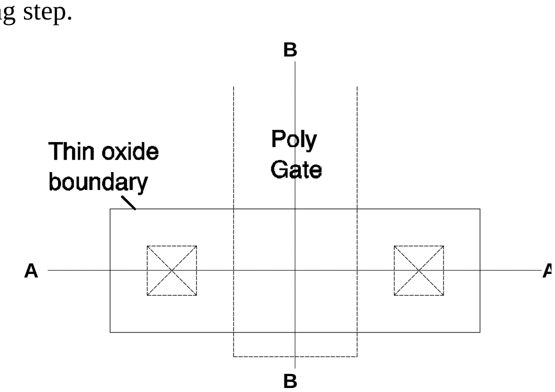




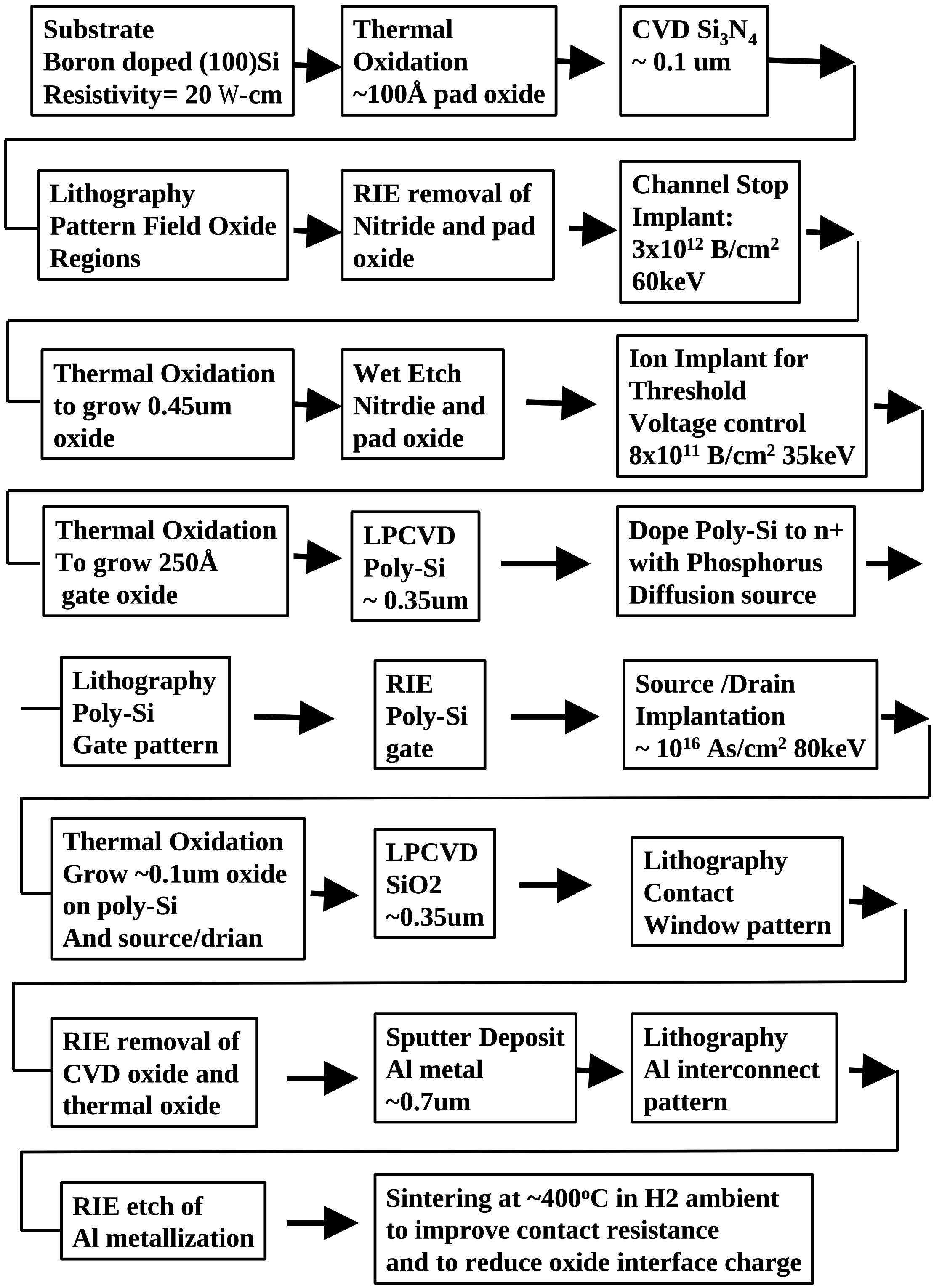
Problem 2 Generic NMOS Process Flow

Draw the cross-sections of the NMOS device along the lines (i) A-A **and** (ii) B-B after

(a) The silicon nitride CVD deposition step
(b) The field oxide growth step
(c) RIE poly-Si gate step
(d) RIE of intermediate oxide and thermal oxide step
(e) Hydrogen annealing step.

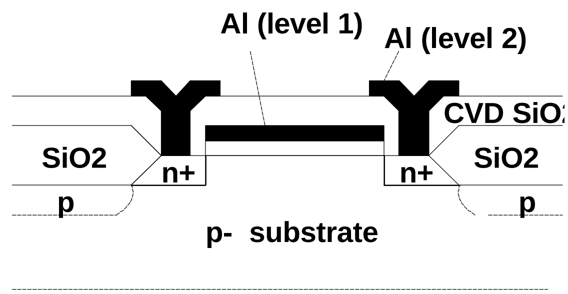


Problem 2 process flow description



Problem 3 Self-aligned Al Gate MOSFET

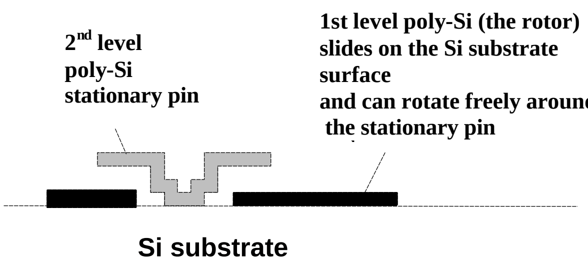
After aluminum deposition, the processing temperature cannot higher than 650°C because the aluminum will melt. For example, the 900°C annealing step required to activate the implanted dopants for source/drain implants cannot be performed after aluminum deposition. **With this constraint in mind,** design a process flow for this **self-aligned implanted source/drain MOSFET using Al as the gate material** [shown as Al(level 1) in figure]. A schematic cross-section of the device is illustrated below.
Describe the process flow and show the cross-sections at major processing steps.
[Hint: Use a high-temperature compatible material to form a “dummy” gate. After S/D formation, selectively remove the dummy gate and replace it with Al]

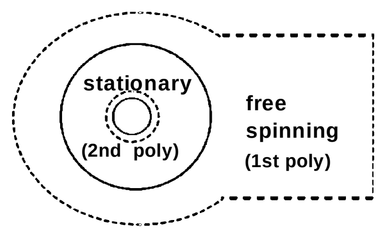


Self-aligned Al-Gate MOSFET

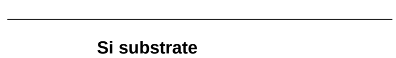
Problem 4 Pin Joint Process Sequence

(a) Using surface micromachining, a **pin joint** can be fabricated with the cross-section and top view shown below. The pin joint has a stationary pin (the anchor) on the wafer surface and a free spinning rotor which slides on top of the wafer surface. Note that the top of the stationary pin has a dimension larger than that of the rotor inner hole to keep the rotor in place.





You find the following brief description of the process flow in the notebook of a former EE143 student. Sketch the cross-sections and top views at the highlighted processing steps (marked by bold font).

Process Description	***Cross-Sections***	***Top Views***
Starting Material –Pure Si wafer		

Deposit 1st level Phosphosilicate glass (PSG) by CVD
Deposit of 1st level Poly-Si by CVD
Pattern 1st level poly-Si and PSG-1(Mask #1)
Deposit 2nd level PSG
Pattern opening for stationary pin (Mask #2)
Deposit 2nd level poly-Si by CVD
Pattern 2nd level poly-Si (Mask#3)
Selectively etch away 1st level and 2nd level PSG using HF acid.

(b) The following qualitative questions are related to the process flow in part (a). No partial credit will be given without an explanation or discussion.

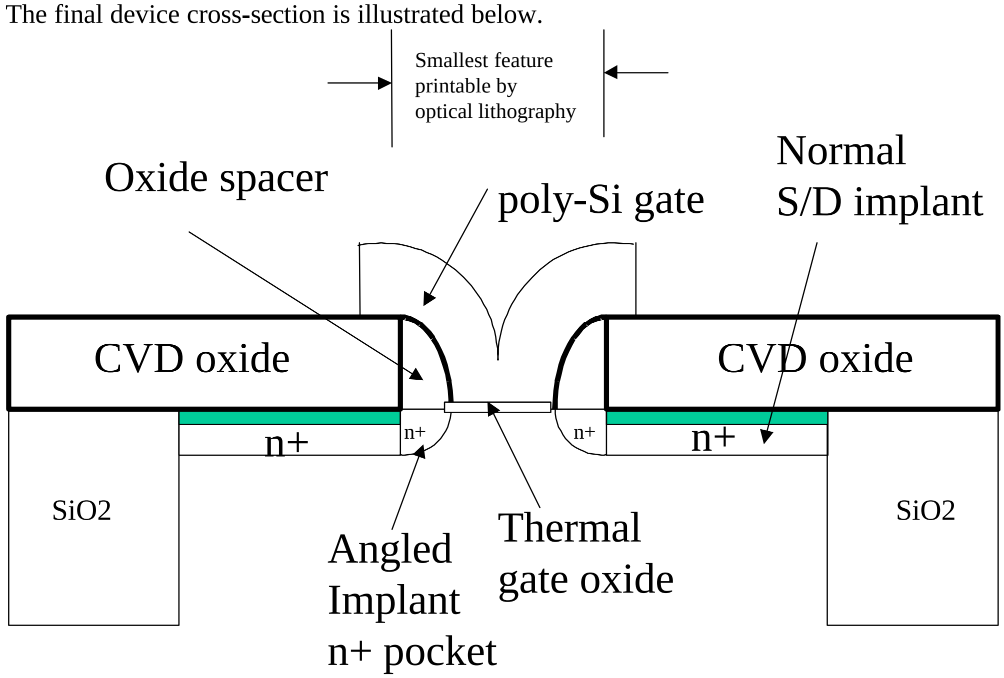
(I) To reduce the inertia of the rotor, some former EE143 students proposed to replace the 1st level poly-Si with photoresis as the rotor material. Will this replacement be compatible with the process sequence?
(II) Instead of depositing the 2nd level PSG by CVD, can we use thermal oxidation to form the 2nd level oxide? Discuss why or why not?
(III) The process flow in part (a) uses two separate poly-Si deposition. Can we fabricate the device with only one layer of poly-Si? Explain why or why not ?

Problem 5 Sub-50nm MOSFET Process Flow

Optical lithography can only define features larger than 50nm. To fabricate MOSFETs with channel length less than 50nm, the following process description is found in a publication:

(1) Fabricate oxide trench for device isolation
(2) Form silicon nitride on pad-oxide films.
(3) Pattern nitride/pad-oxide to smallest feature by optical lithography
(4) n+ S/D implant
(5) Angle implant (tilted ~ ±45 degrees) to form n+ pockets.
(6) Form $TiSi_2$ on S/D regions
(7) Deposit CVD oxide and planarize surface by CMP
(8) Selectively remove nitride dummy gate
(9) Deposit CVD oxide and form oxide spacer by RIE
(10) Grow gate oxide by thermal oxidation
(11) Poly-Si gate deposition by CVD
(12) Pattern Poly-Si gate

The final device cross-section is illustrated below.



Let us start with a structure with oxide trench isolation already fabricated. Continue the process description with your interpretation of the process flow. Show the cross-sections at major processing steps.

Process Description **Cross-section**

1) Starting structure (oxide trench isolation)