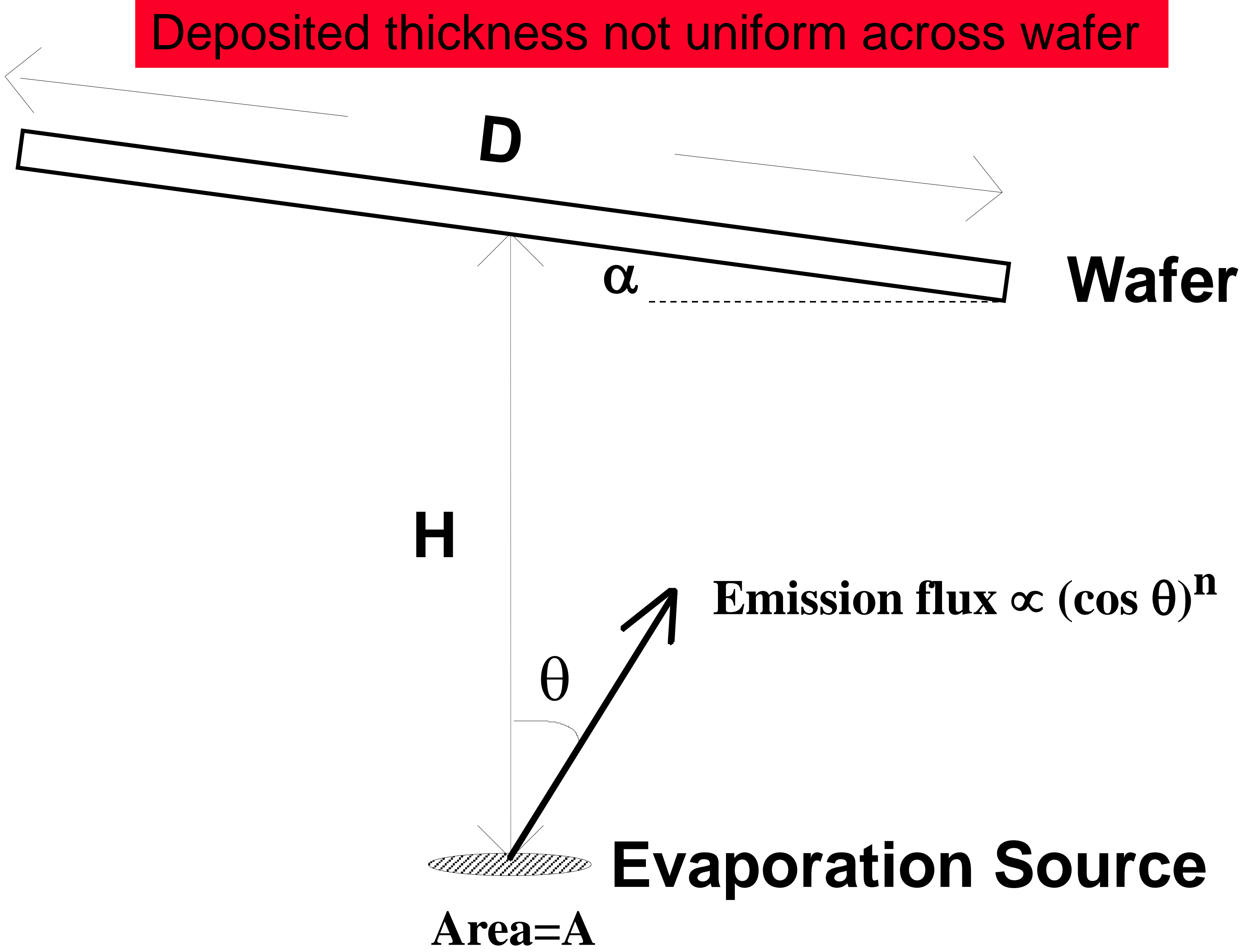
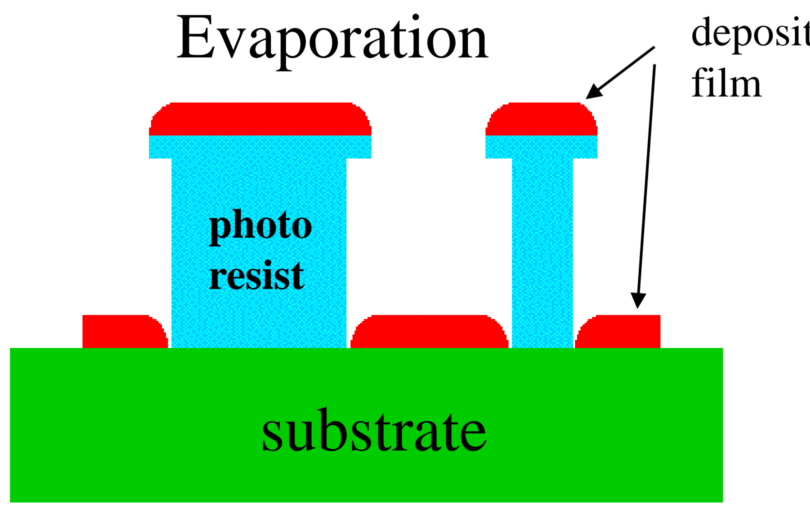
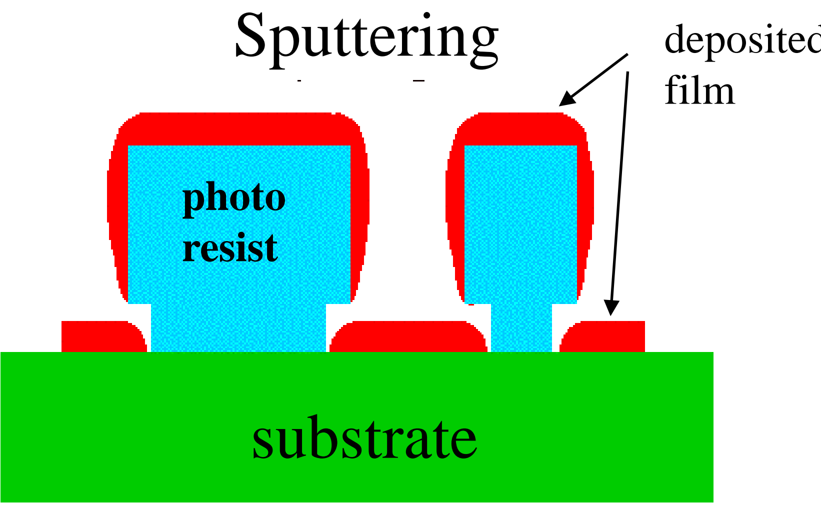

Deposited thickness not uniform across wafer
D
Wafer
α
H
Emission flux ∝ (cos θ)^n
θ
Evaporation Source
Area=A

Step coverage

Lift-off performance



Step coverage problem
is not the same
as thickness nonuniformity
problem



Thermal Oxidation Model

stagnant layer

C_G

C_s

SiO_2

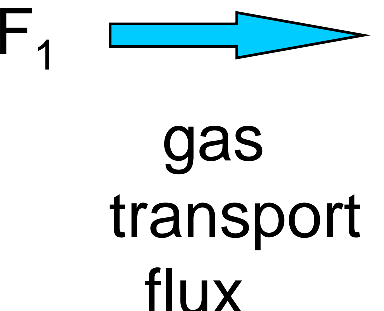
Si

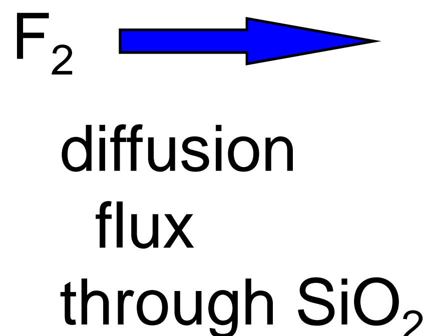
Note
$C_s \neq C_o$

C_o

C_i

X_{0x}

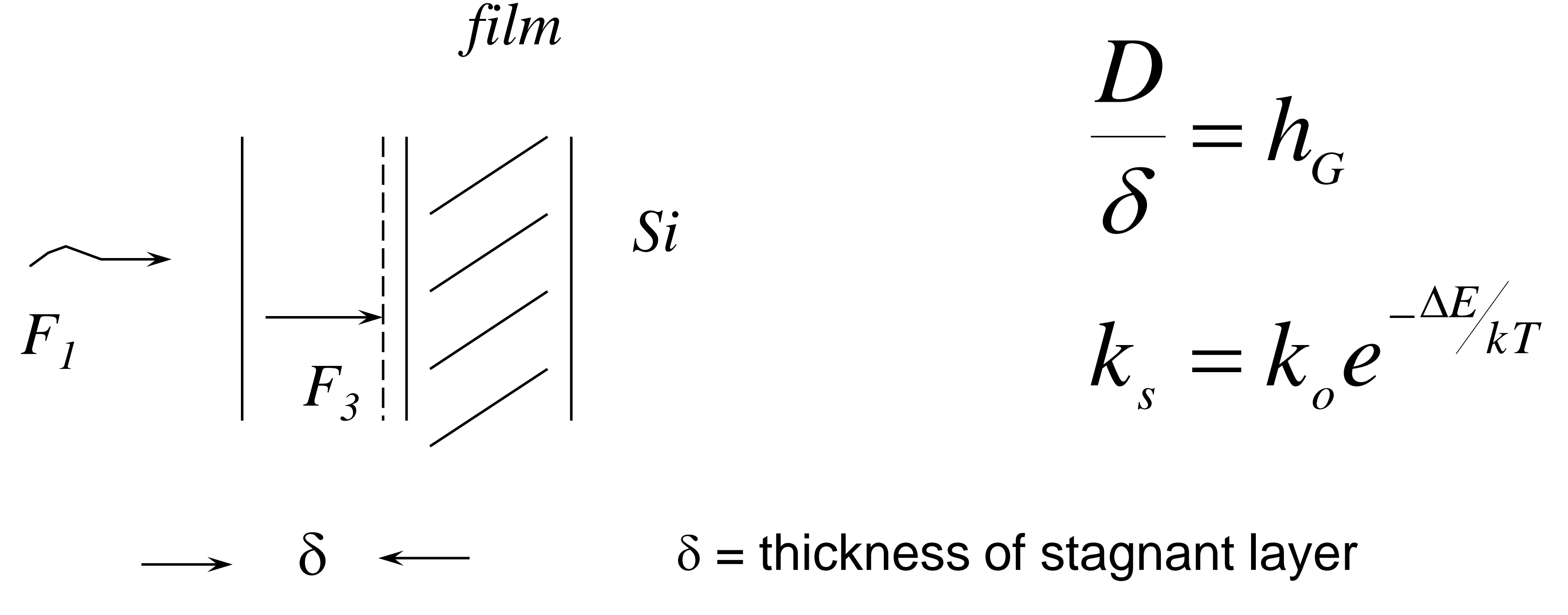




F_3

reaction
flux
at interface

CVD Deposition Rate [Grove Model by setting Xox =0]

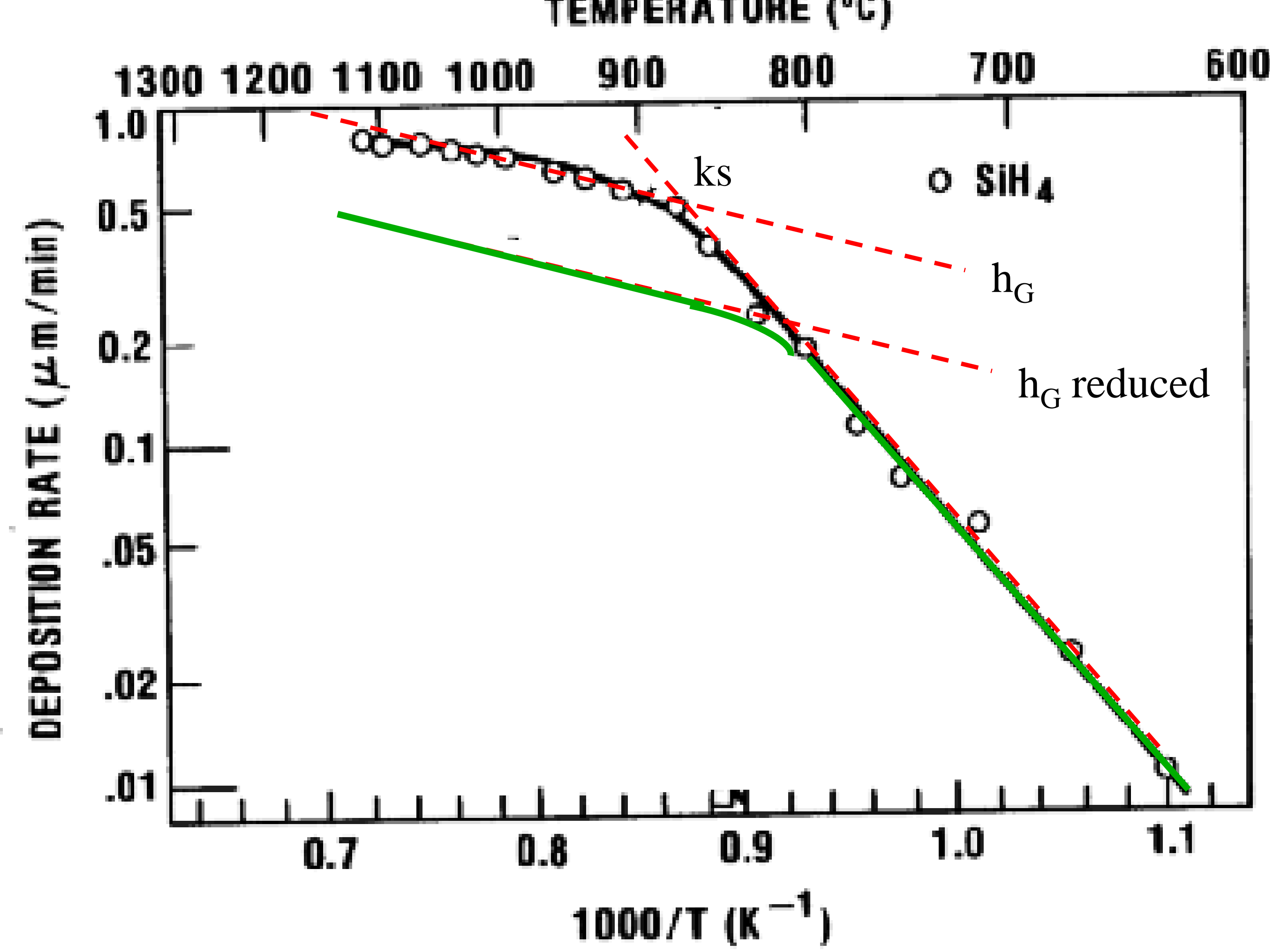


$$F_1 = D\,[\,C_G - C_S\,] / \delta$$

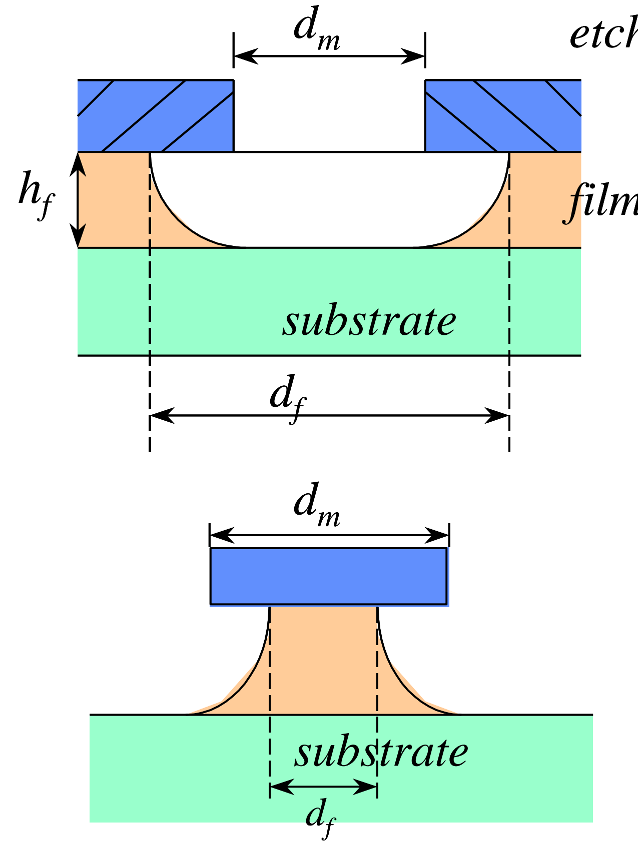
$$F_3 = k_S\, C_S$$

$$F_1 = F_3$$

ks depends only on temperature
h_G depends on temperature, pressure and flow velocity



Degree of Anisotropy



$$Bias\ B \equiv d_f - d_m$$

B can be > 0 or < 0.

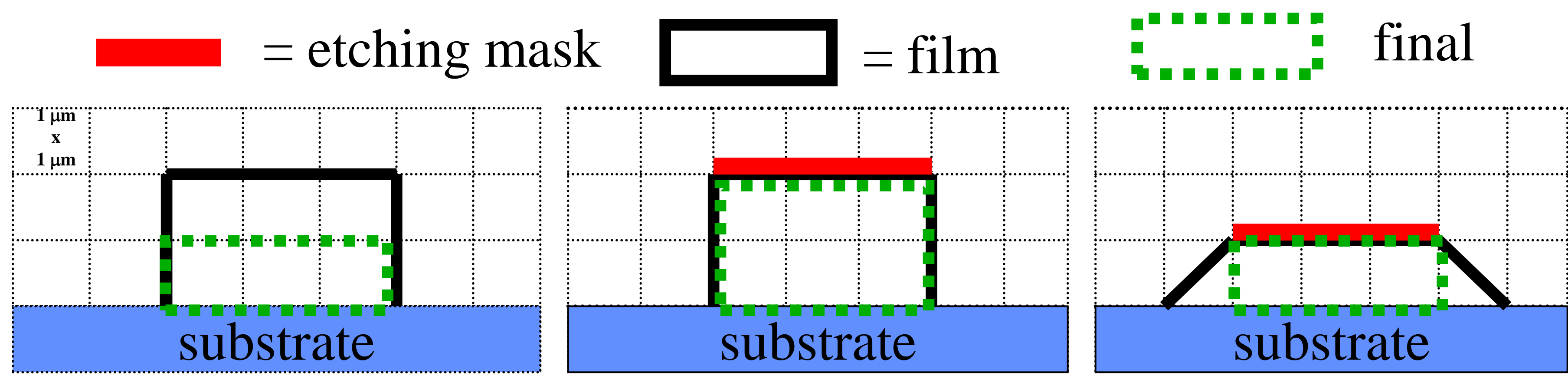
$$A_f \equiv 1 - \frac{|B|}{2h_f}$$

$$0 \leq A_f \leq 1$$

Etching profile depends on:

1) mask/film configuration
2) Film etching rate and anisotropy
3) Maks etching rate and anisotropy

SIMPLE EXAMPLE: Film etching 100% anisotropic
NO mask etching



Etching Selectivity S

$$S_{AB} = \frac{v_A(\text{vertical etching velocity of mateal A})}{v_B(\text{vertical etching velocity of mateal B})}$$

Wet Etching

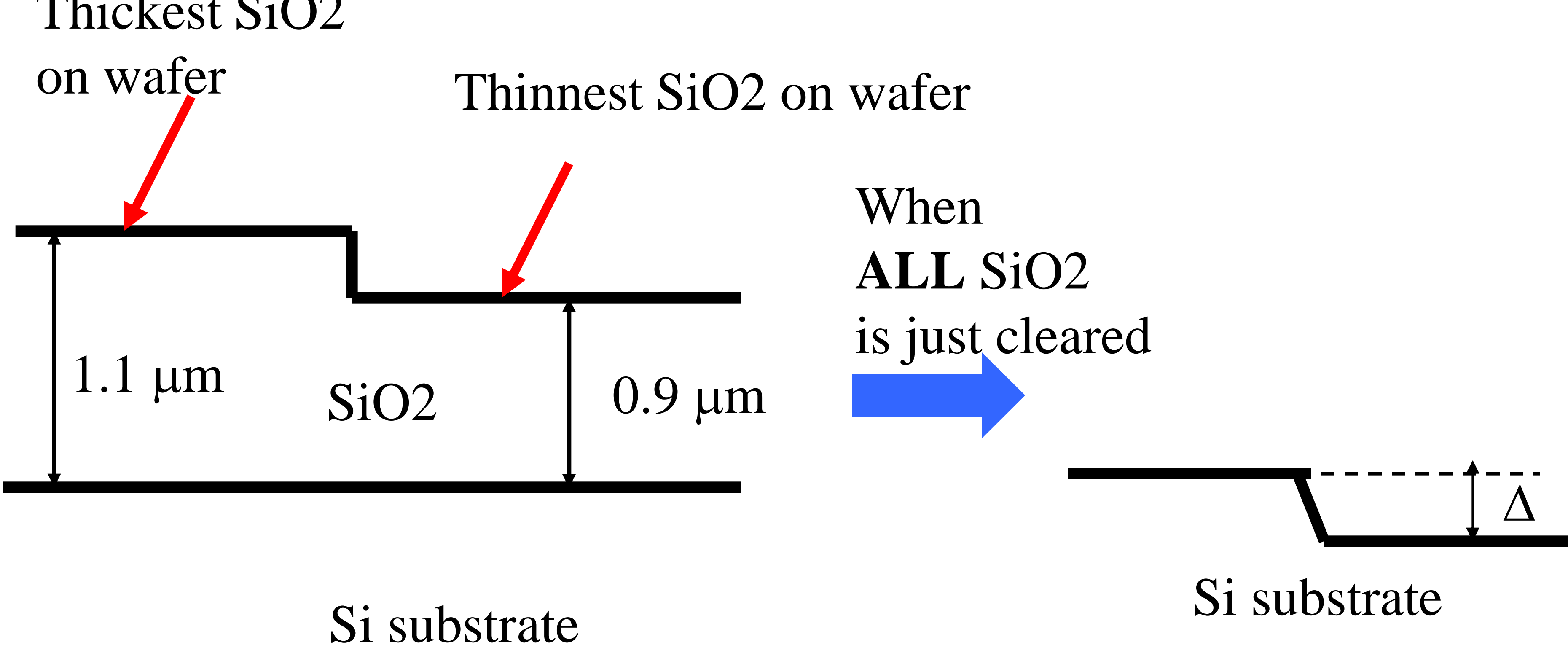
S is controlled by: chemicals, concentration, temp.

RIE

S is controlled by:
plasma parameters, plasma chemistry,
gas pressure, flow rate & temperature.

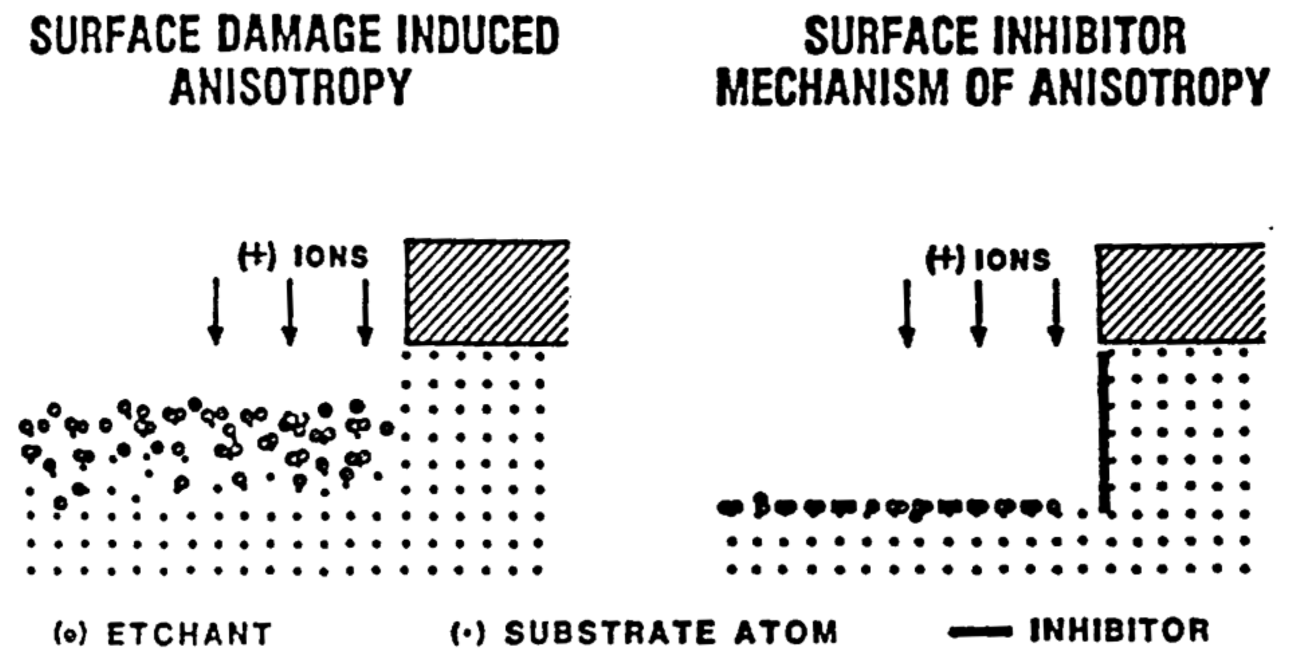
Importance of Etching Selectivity

A simple Example



How to Control Anisotropy ?

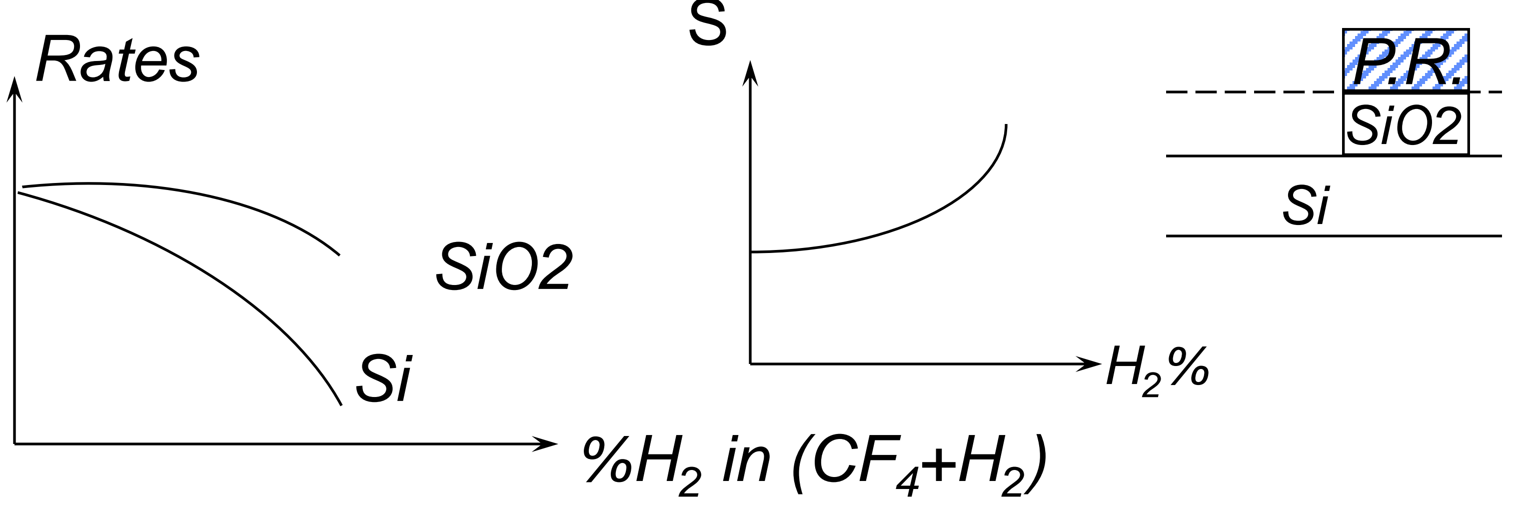
1) ionic bombardment to damage expose surface.
2) sidewall coating by inhibitor prevents sidewall etching.



How to Control Selectivity ?

$$S = \frac{Rate\ SiO_2}{Rate\ Si}$$

E.g. SiO_2 etching in CF_4+H_2 plasma



Reason: $F^* + H \rightarrow HF \therefore F^* content \downarrow$

$\therefore SiF_4 \downarrow$

The F* reaction with Si alone is a chemical etching (more isotropic)

Effect of RIE process variables on etching characteristics

Effects of Process Variables

Increasing pressure

H_2 additions

CF_4 plasma

O_2 additions

300 eV

Control variable

effect

Increasing anisotropic etching

Increasing in SiO_2:Si selectivity

Ion bombardment energy (i.e. bias and Vp)

Etching area

Polymer formation area

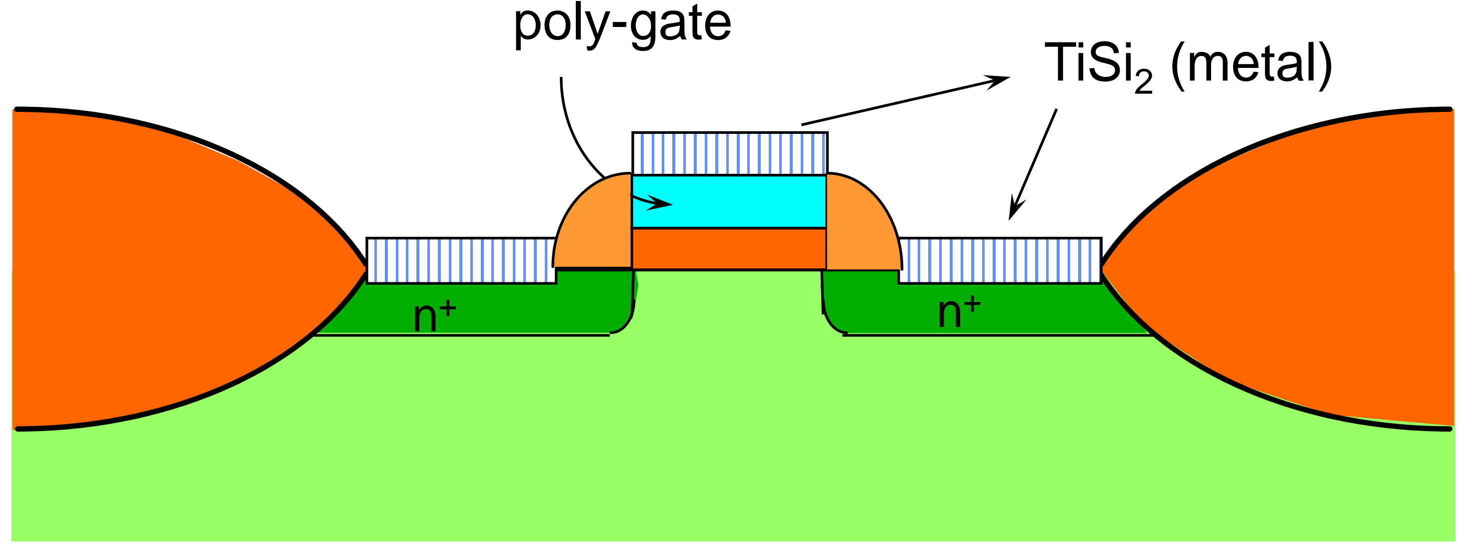
Isotropal etching

0

Increasing anisotropic etching

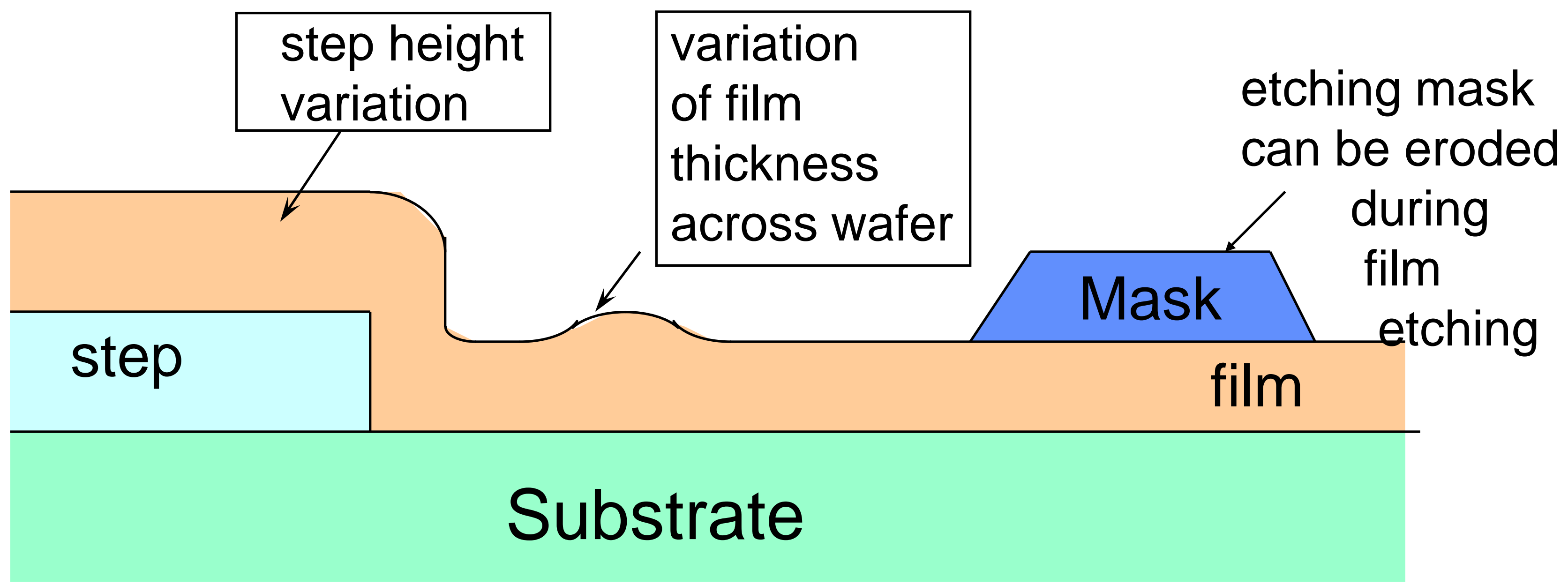
Increasing isotropic etching

Self-Aligned Silicide Process (SALICIDE) using Ion Implantation and Metal-Si reaction



*Self-aligned structures are always preferred for process integration

Worst-Case Design Considerations for Etching



Example: Dual Damascene Process