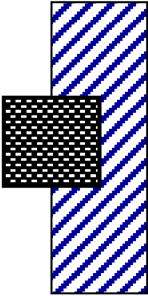
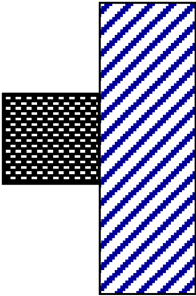
Importance of Layer-to-Layer Alignment

Example: metal line to contact hole

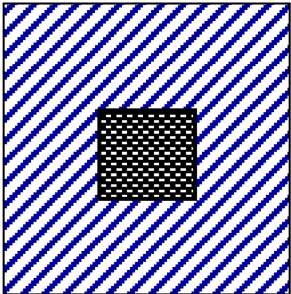


→ marginal contact



→ no contact!

safety margin to allow for misalignment



Example of Design Rule:

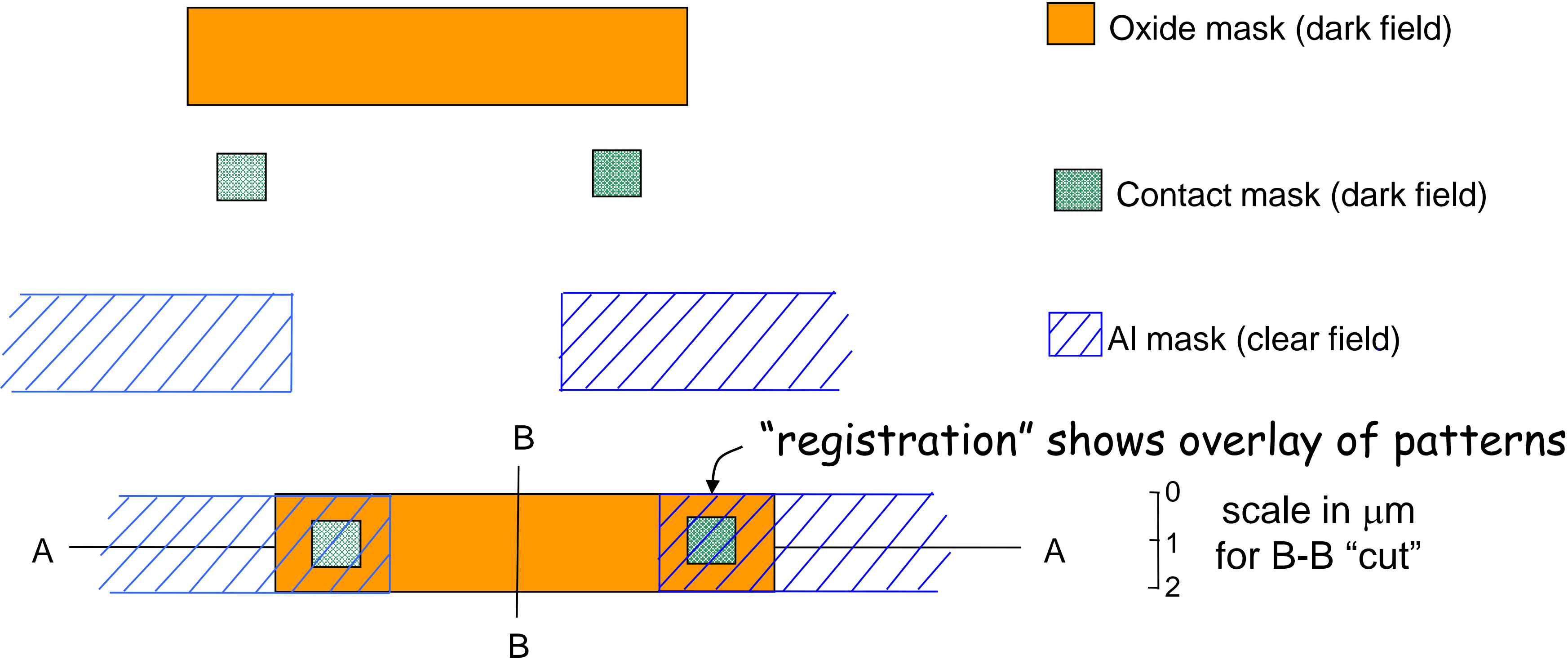
If the minimum feature size is 2λ, then the safety margin for overlay error is λ.

→ **Design Rules are needed**:

- Interface between designer & process engineer
- Guidelines for designing masks

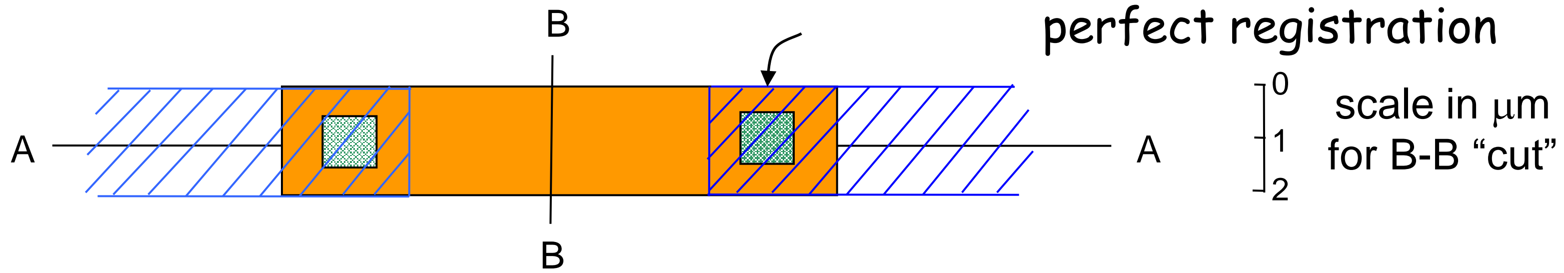
IC RESISTOR MASK LAYOUTS – REGISTRATION OF EACH MASK

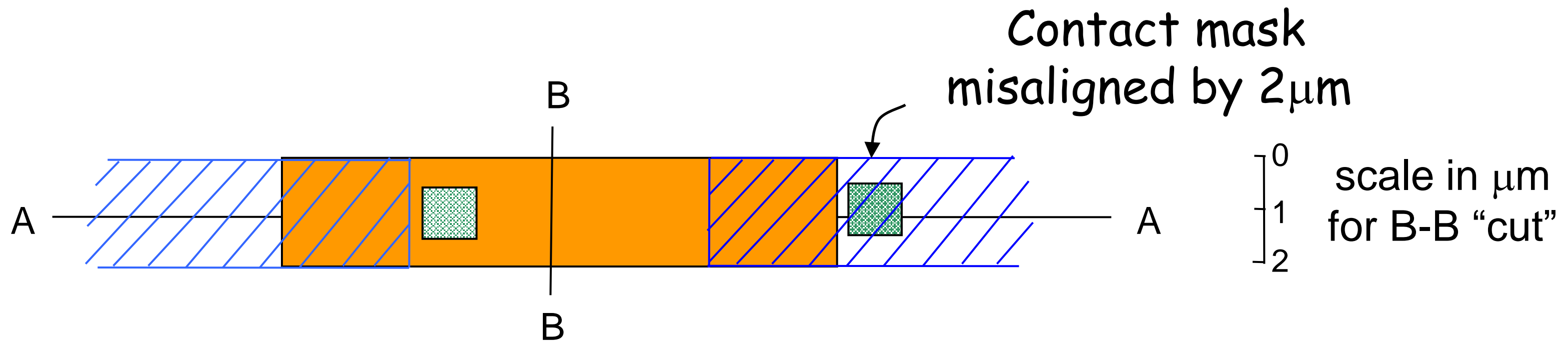
Registration of mask patterns is critical → show separate layouts to avoid ambiguity



Registration of one mask to the next (also called "alignment" and "overlay") is a crucial aspect of lithography

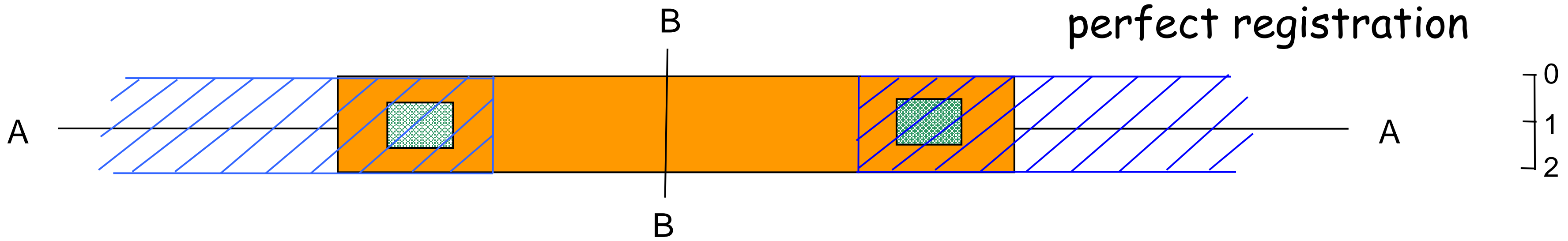
Same Layout but with misregistration (misalignment)

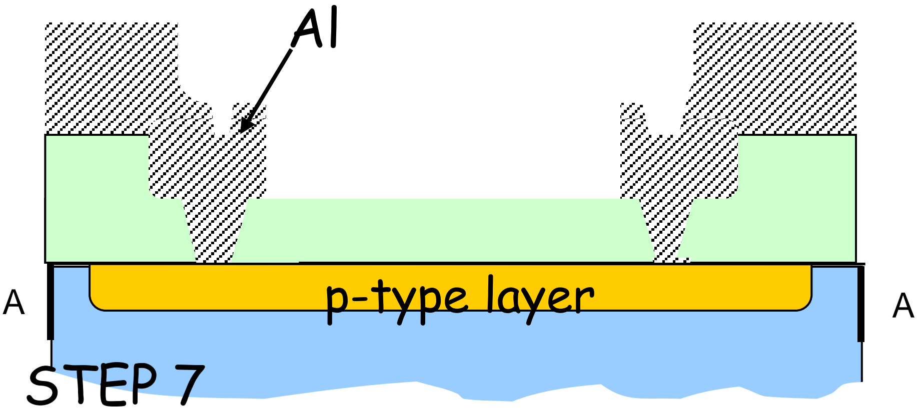




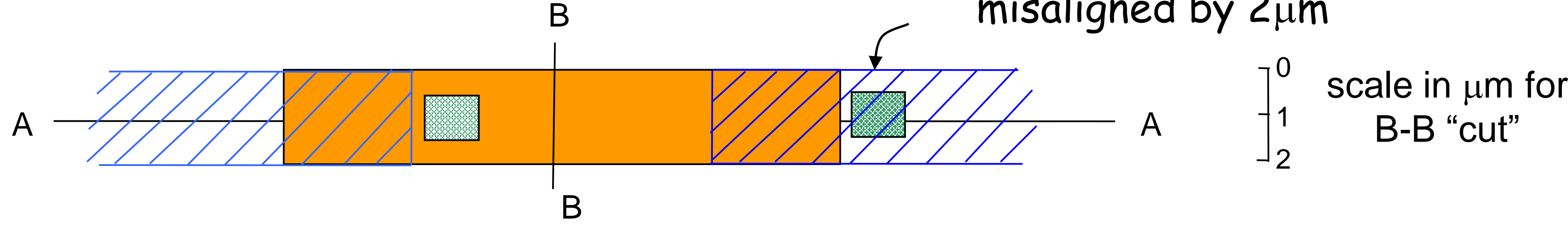
Lets look again at cross-section A-A to understand the consequence of this misalignment. Note contact mask → 2μm

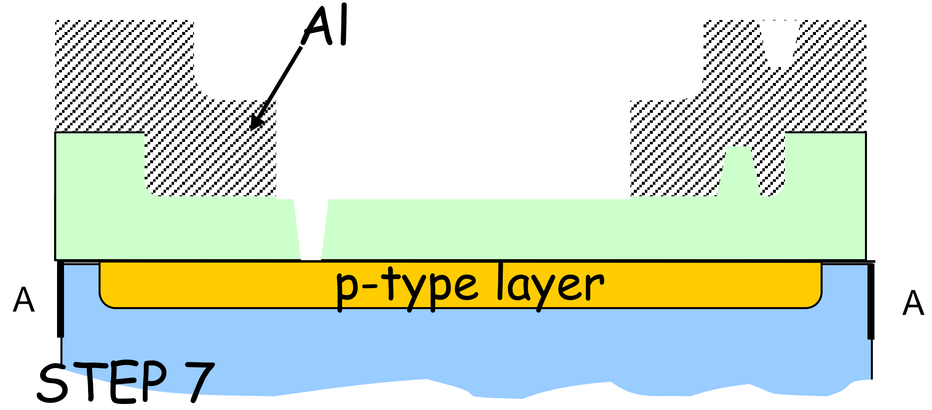
Layout with no misregistration (misalignment)





Layout with misregistration (misalignment)





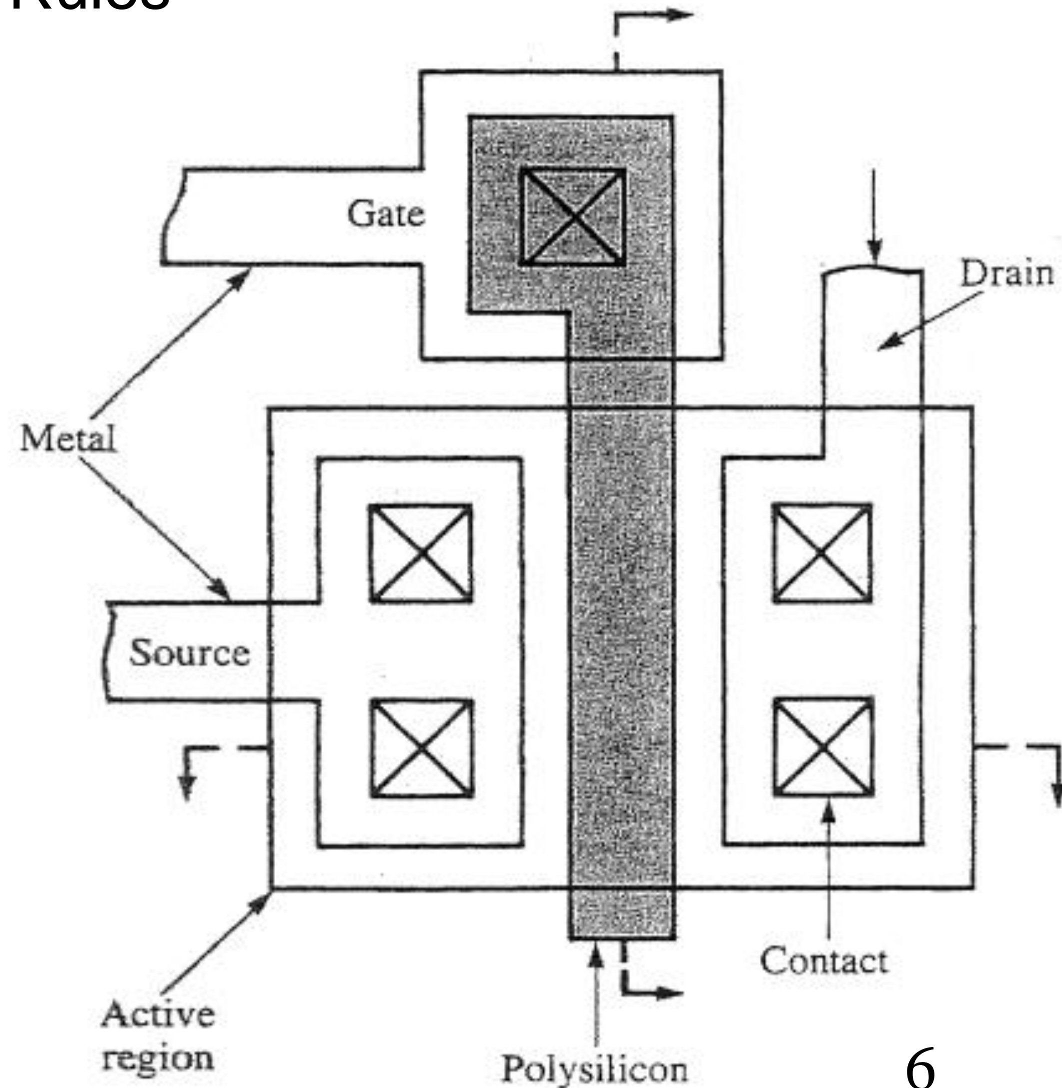
This resistor has an open circuit !!

Thus we need safety margins in layout which take into account the possible tolerances in fabrication. Each process has a set of "**design rules**" which specify the safety margins.

Layout Design Rules

(1) Absolute-Value Design Rules
* Use absolute distances

(2) λ -based Design Rules

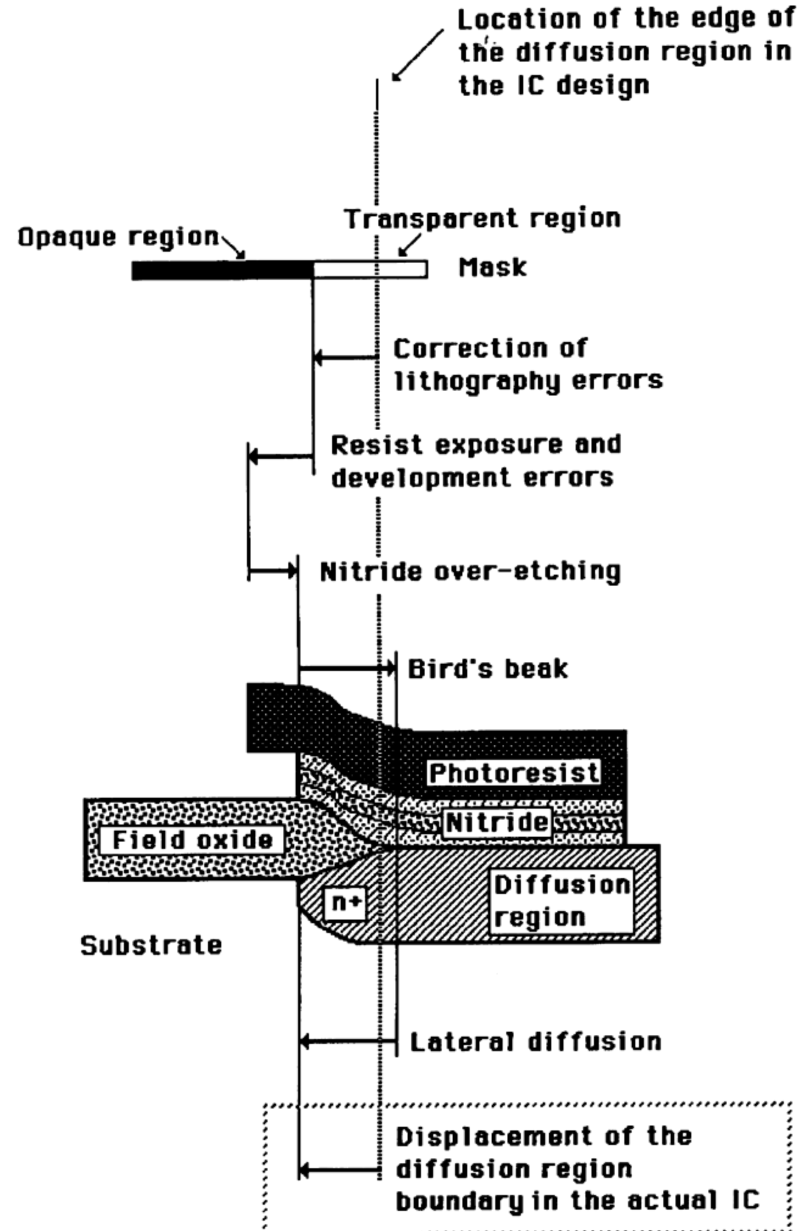


EE143 Layout Design Rules

1. Basic length unit = λ = 2μm

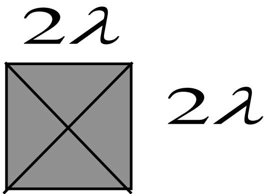
1.1 Lithography and etching limit =2λ

1.2 Overlay accuracy = λ

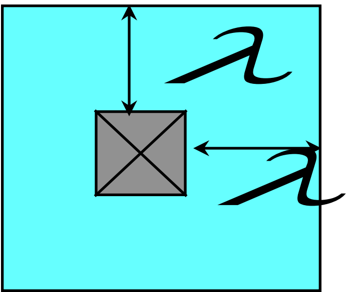


2.1 Metal-Si Contact Hole

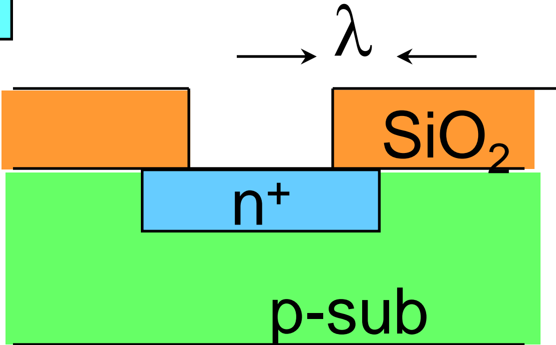
(same rule for Metal-poly)

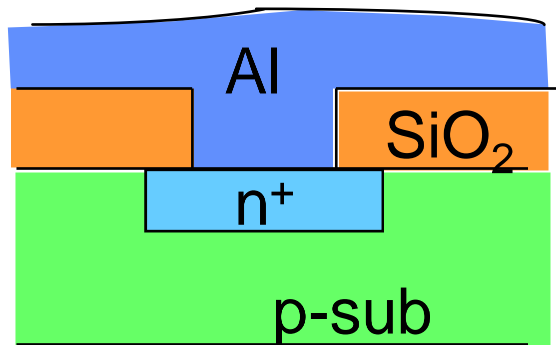


Min. contact hole = 2 λ x 2 λ



Min contact hole to diffusion layer distance = λ

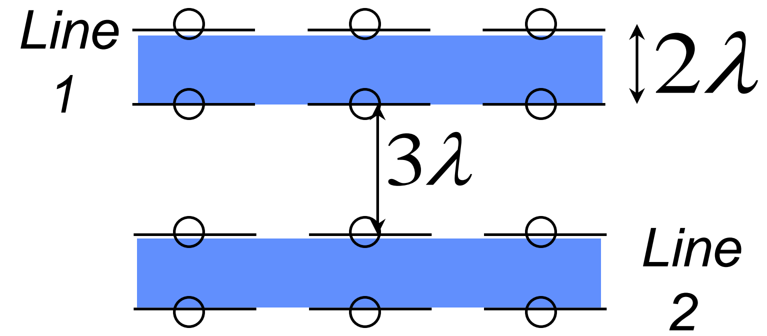




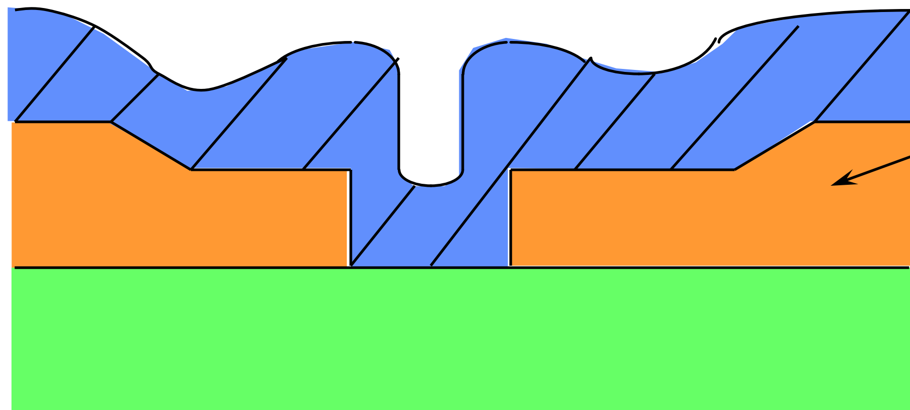
2.2. Metal Lines

Min width = 2λ

Min. metal-metal spacing = 3λ



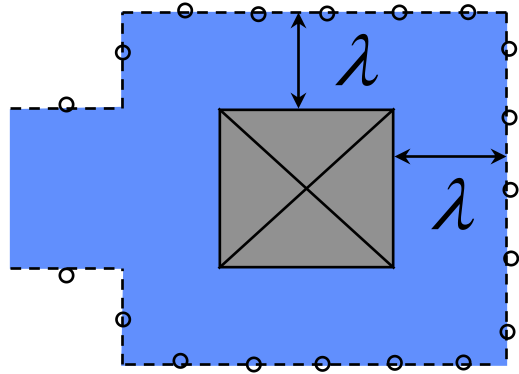
[Rationale]

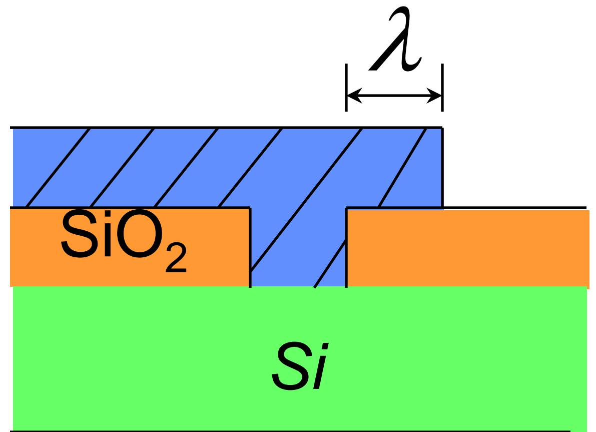


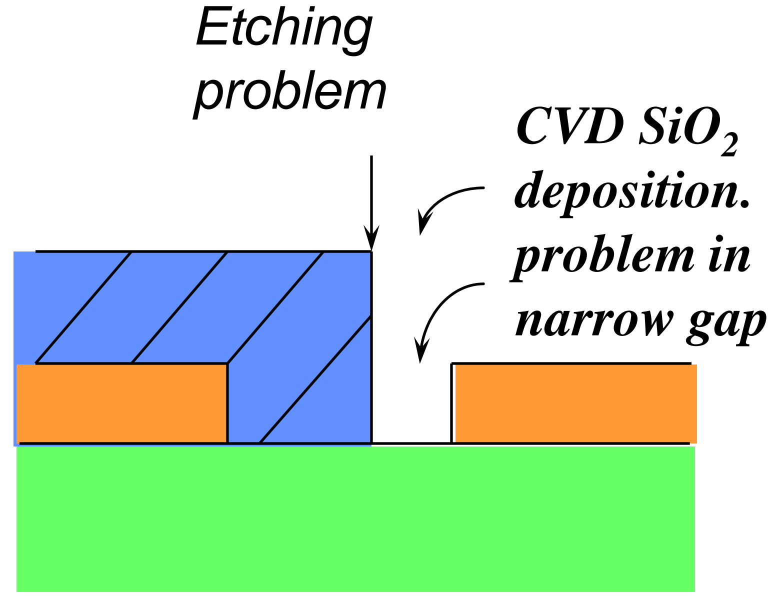
metal runs on rough topography

3 λ spacing to ensure no shorting between the 2 lines.

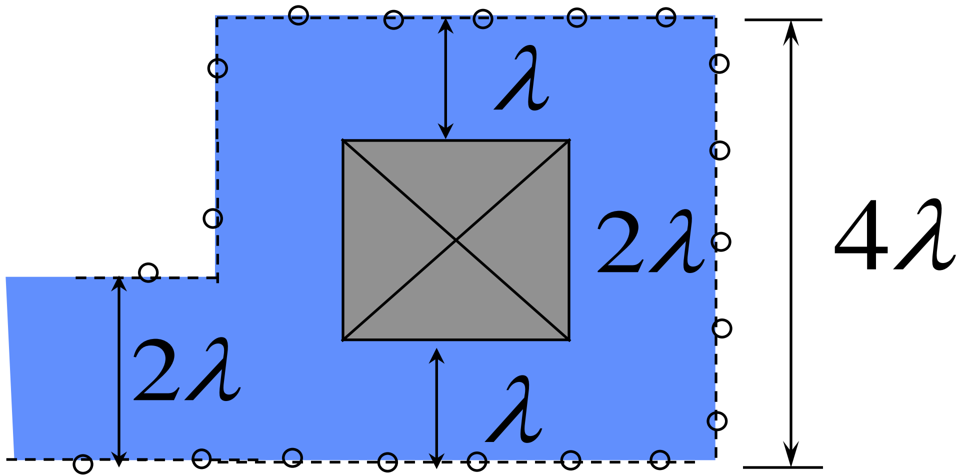
Min overlap of contact hole $= \lambda$





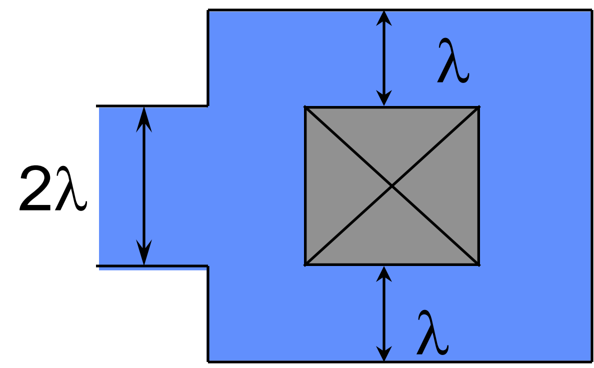


Metal line-width is larger when running over a contact hole



Configuration 1

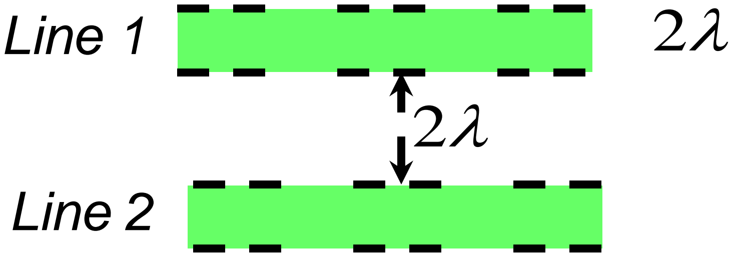
Configuration 2



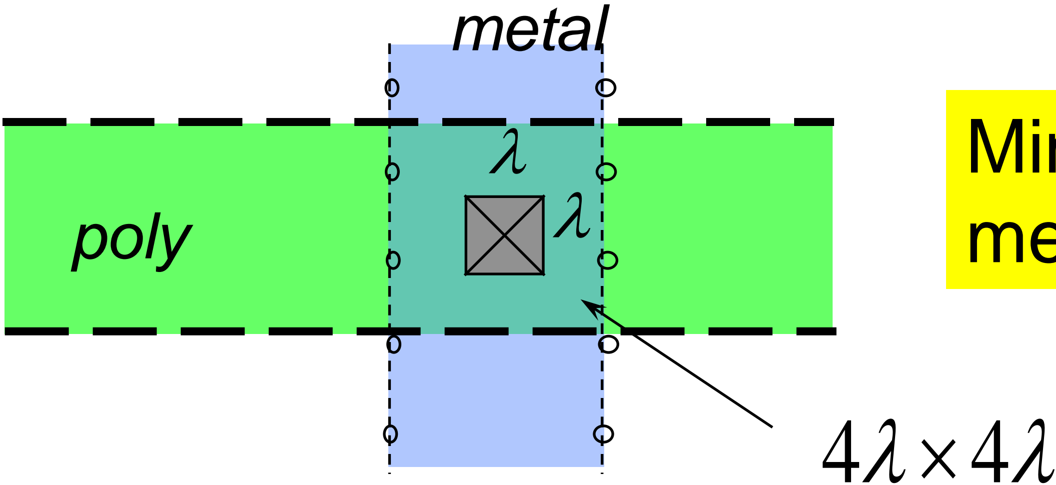
2.3 Poly-Si Lines

Min width = 2λ

Min poly-poly spacing = 2 λ

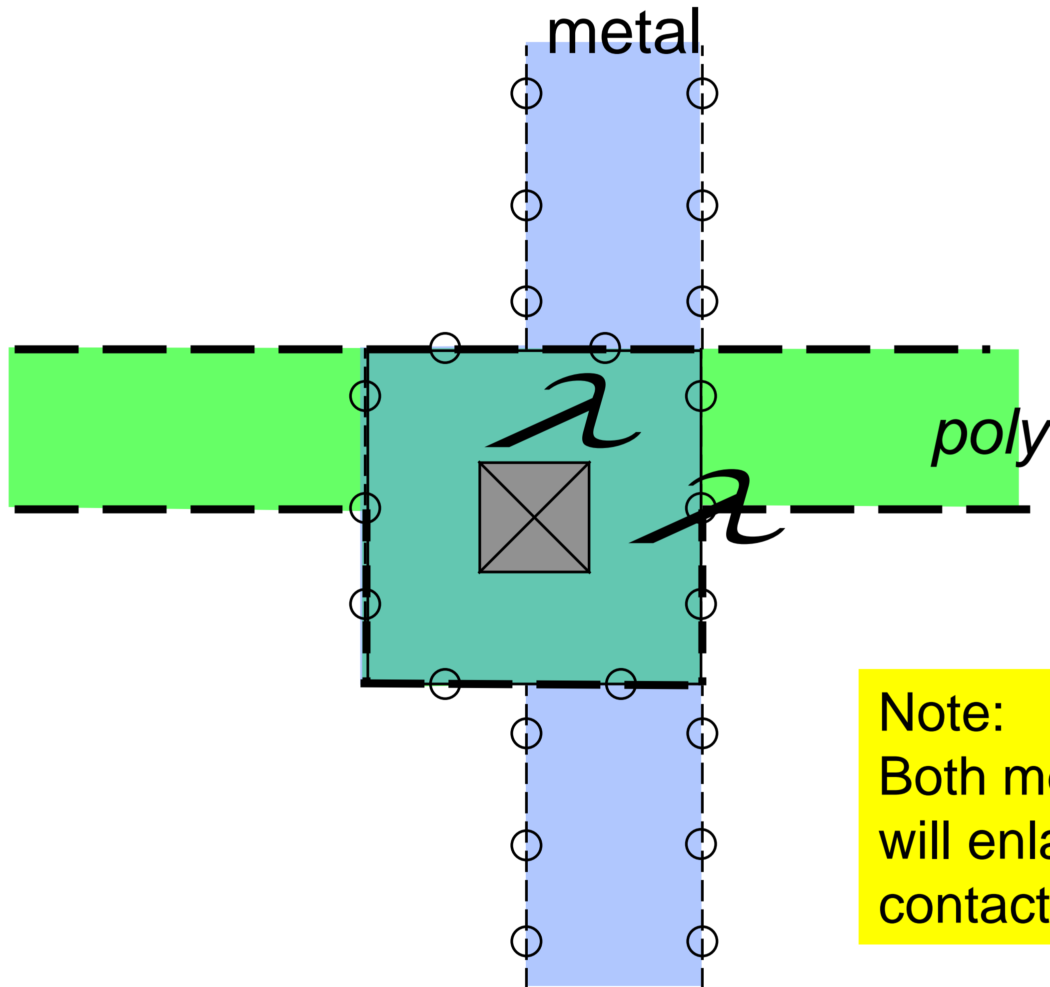


[Rationale: Unlike metal lines, poly-Si runs on smoother topography]



Min underlap of metal/poly contact = λ

Example: Metal Contact to Poly



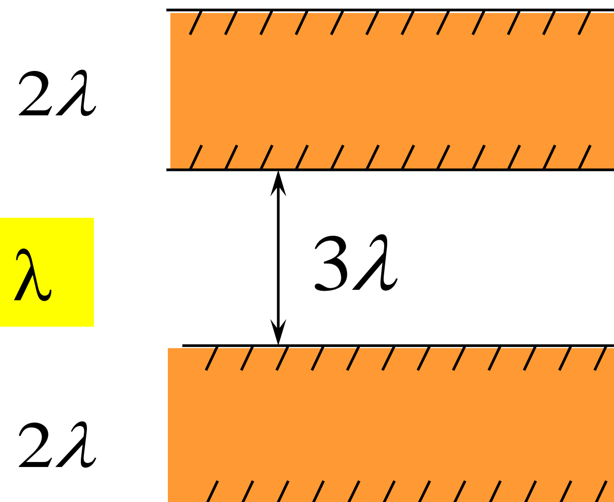
Note:
Both metal and poly linewidths will enlarge to accommodate contact hole overlay error λ

2.4. MOS Thin-Oxide Region

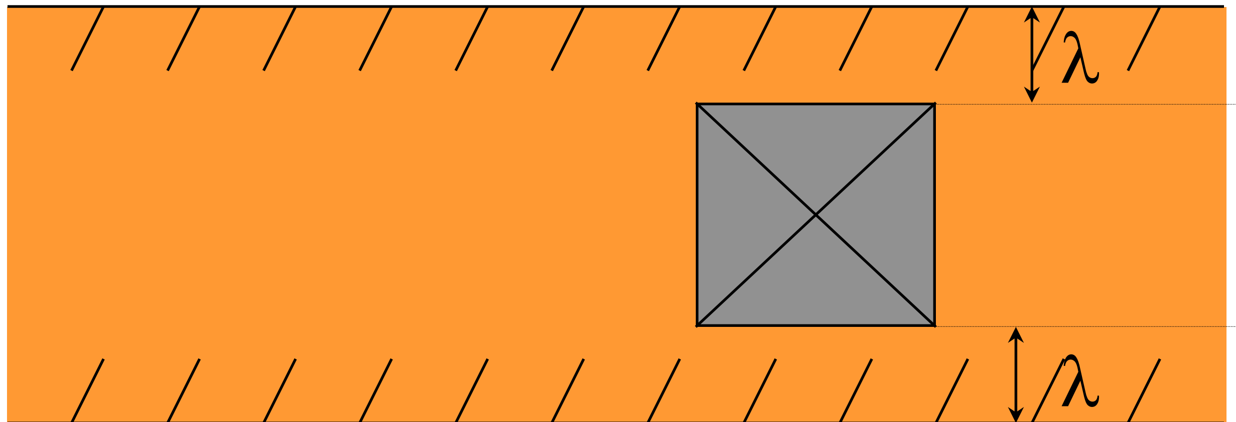
Thick Oxide Region (FOX)

Min Width = 2 λ

Min spacing = 3 λ

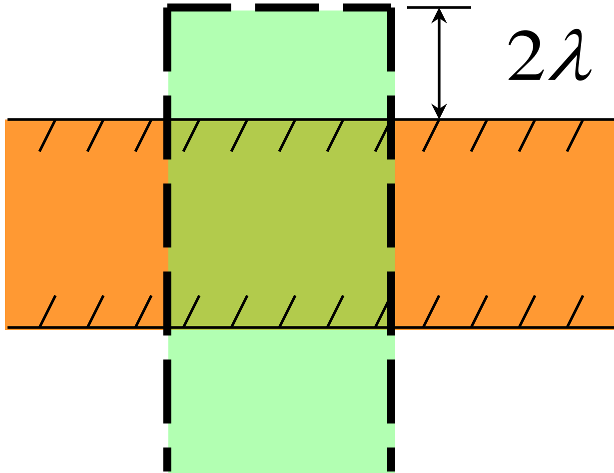


Min underlap of thin-oxide contact $= \lambda$

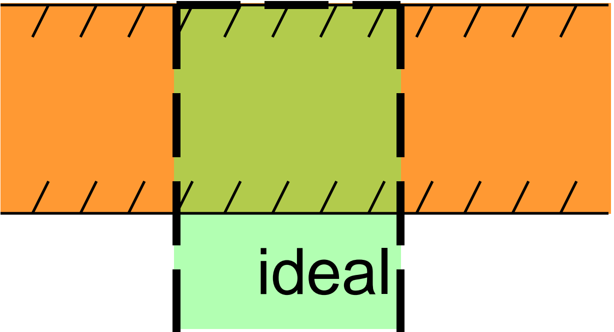


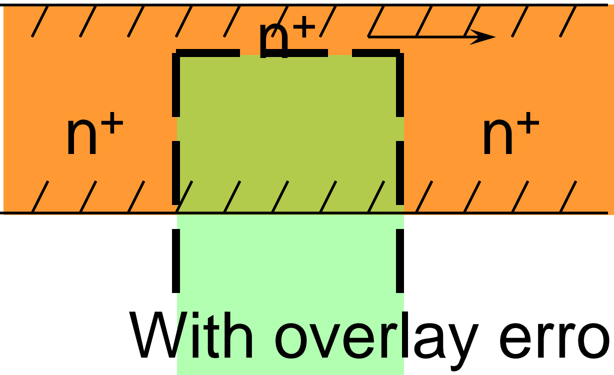
3. Poly-Si Gate

Min gate-overlap of field oxide = 2λ

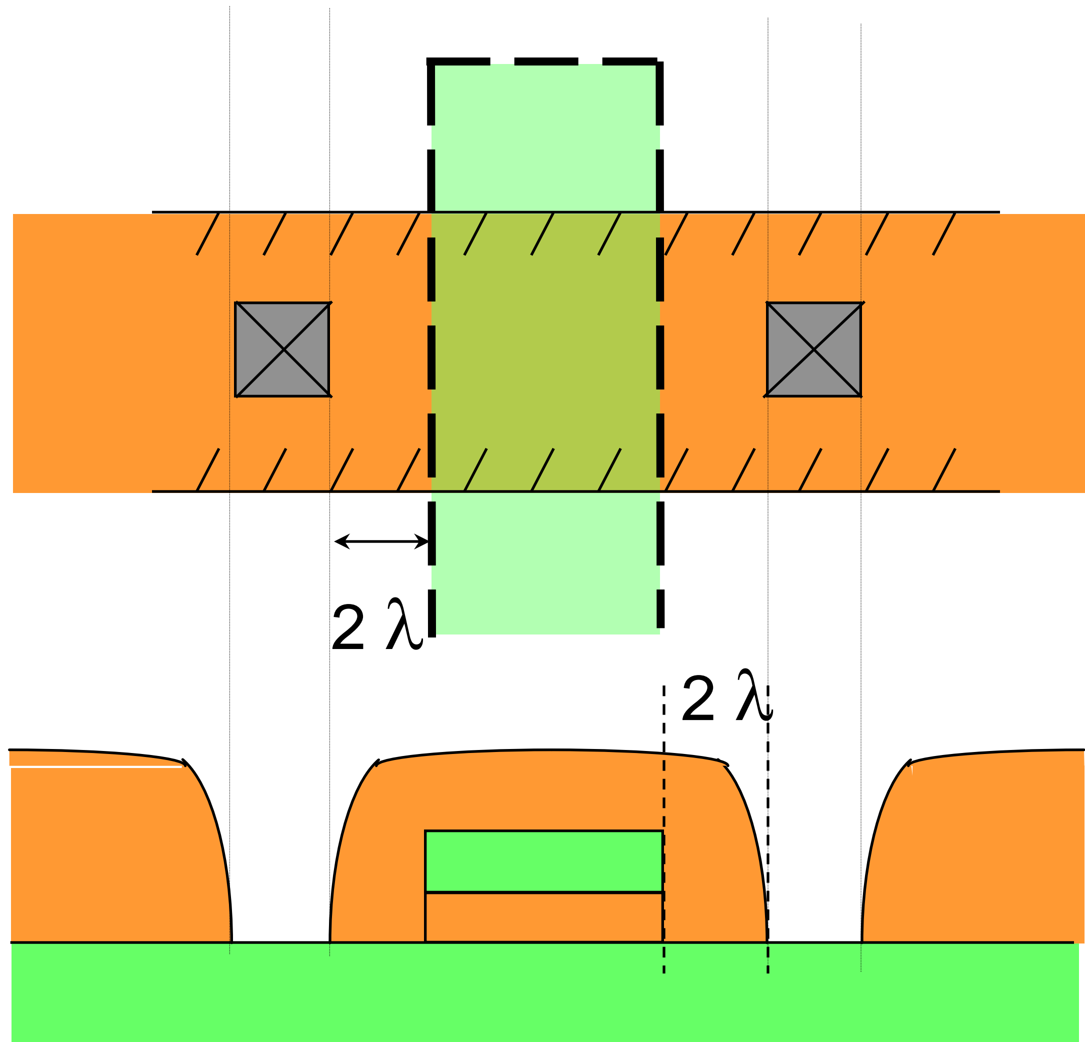


[Comment] Avoid n+ channel formation during S/D Implant

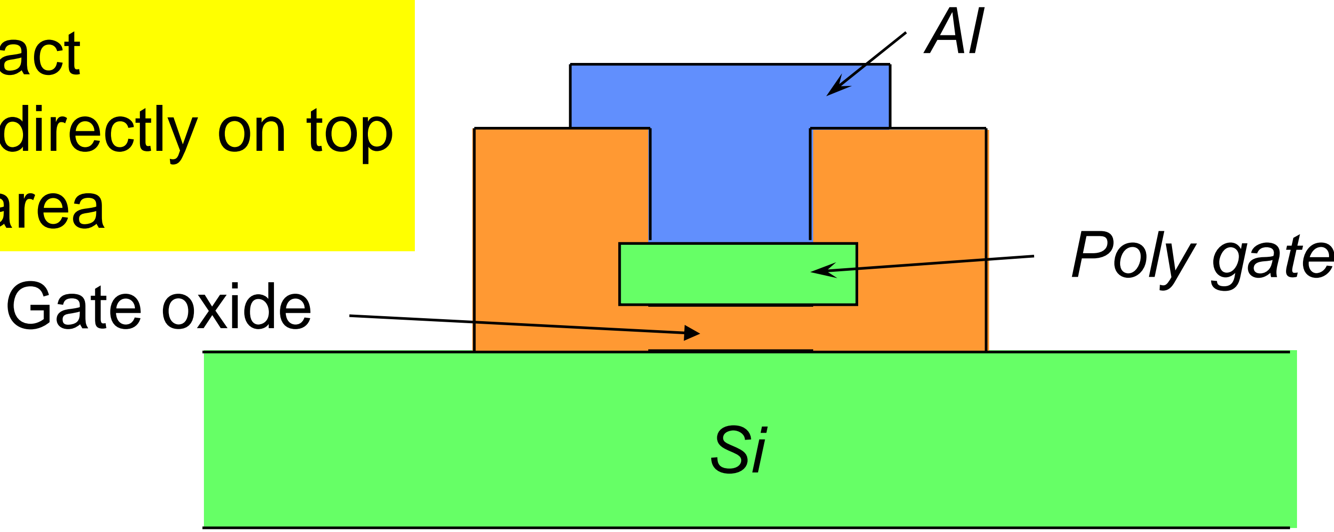


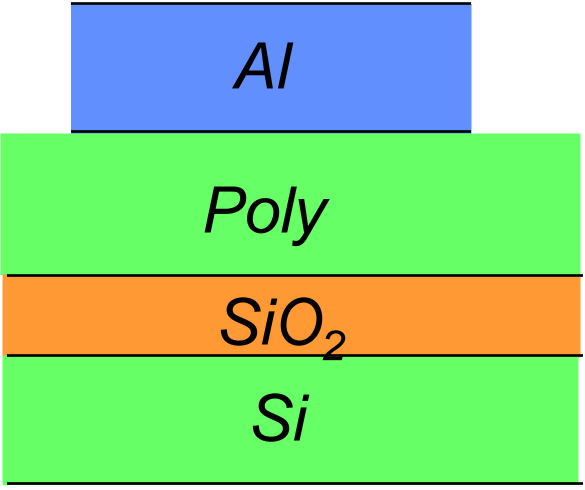


Min thin-oxide contact to gate spacing = 2 λ

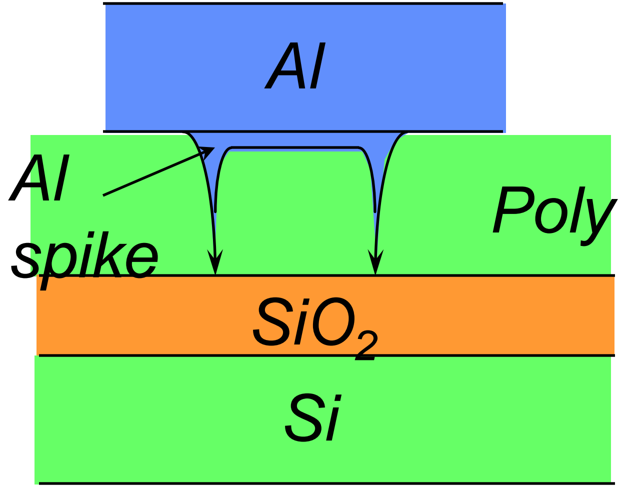


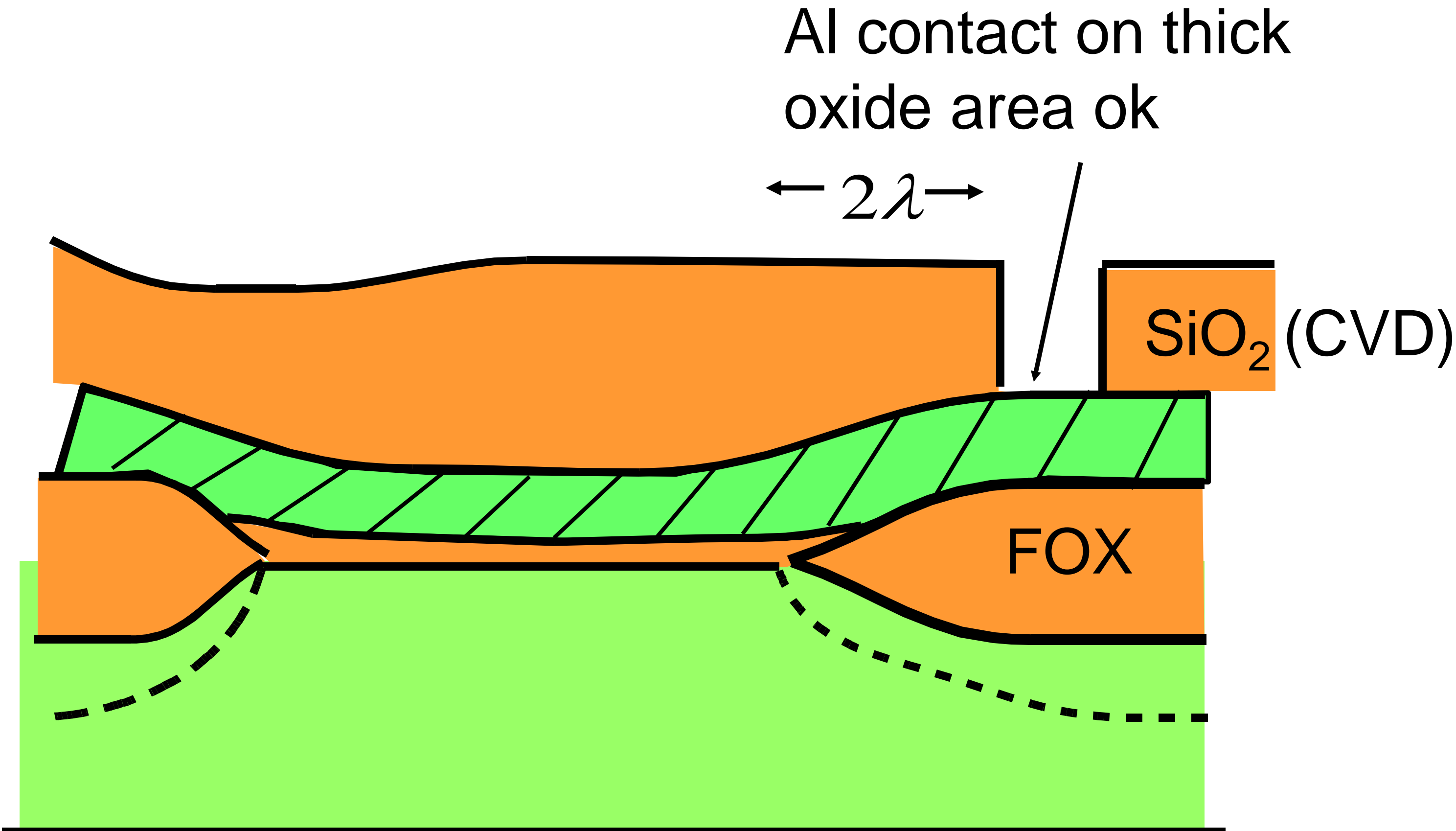
Comment:
Al to poly contact
should not be directly on top
of gate oxide area





~$400^{O}C$



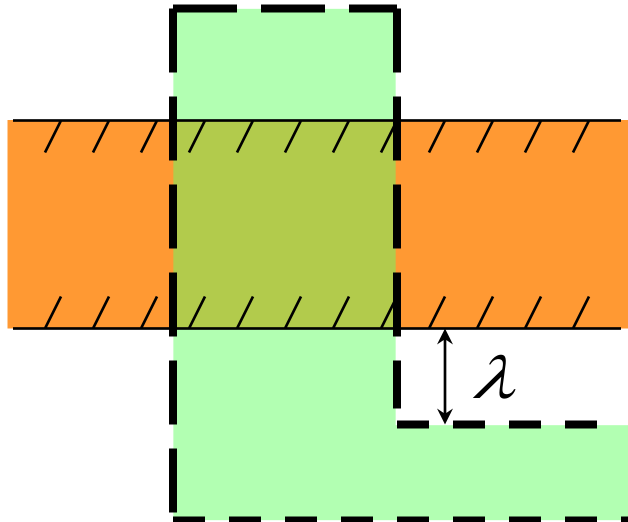

Al contact on thick
oxide area ok
2λ
SiO_2 (CVD)
FOX

Min Gate Width = 2 λ

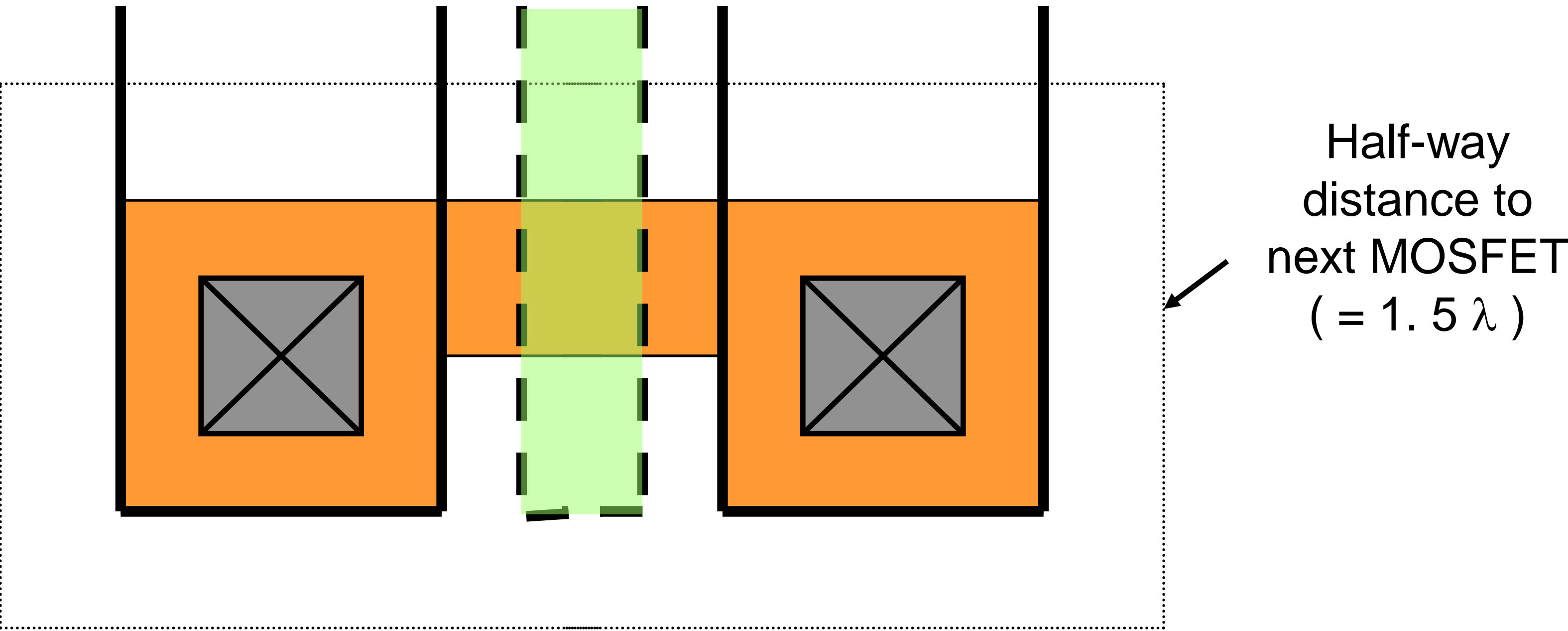
Min Gate Length = 2 λ

Usually: W/L are specified by circuit requirement.

Min. poly to thin oxide spacing = λ



Example Design a minimum-size poly-gate MOS transistor with W/L = 4μm/4μm (2 λ x 2λ)



Minimum size contact = 2λx2λ
Minimum thin-oxide-region underlap of contact = λ
Minimum source/drain contact to gate spacing = 2λ
Minimum L = 2λ Minimum W = 2λ
Minimum gate overlap of field-oxide region = 2λ
Minimum metal overlap of contact = λ
Minimum thin-oxide-region to thin-oxide-region spacing = 3λ
* Layout area /transistor = 15λx7λ = 105 λ^2

metal
poly
Active region
Contact hole