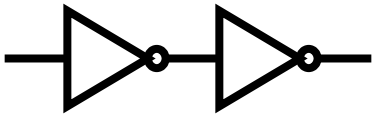
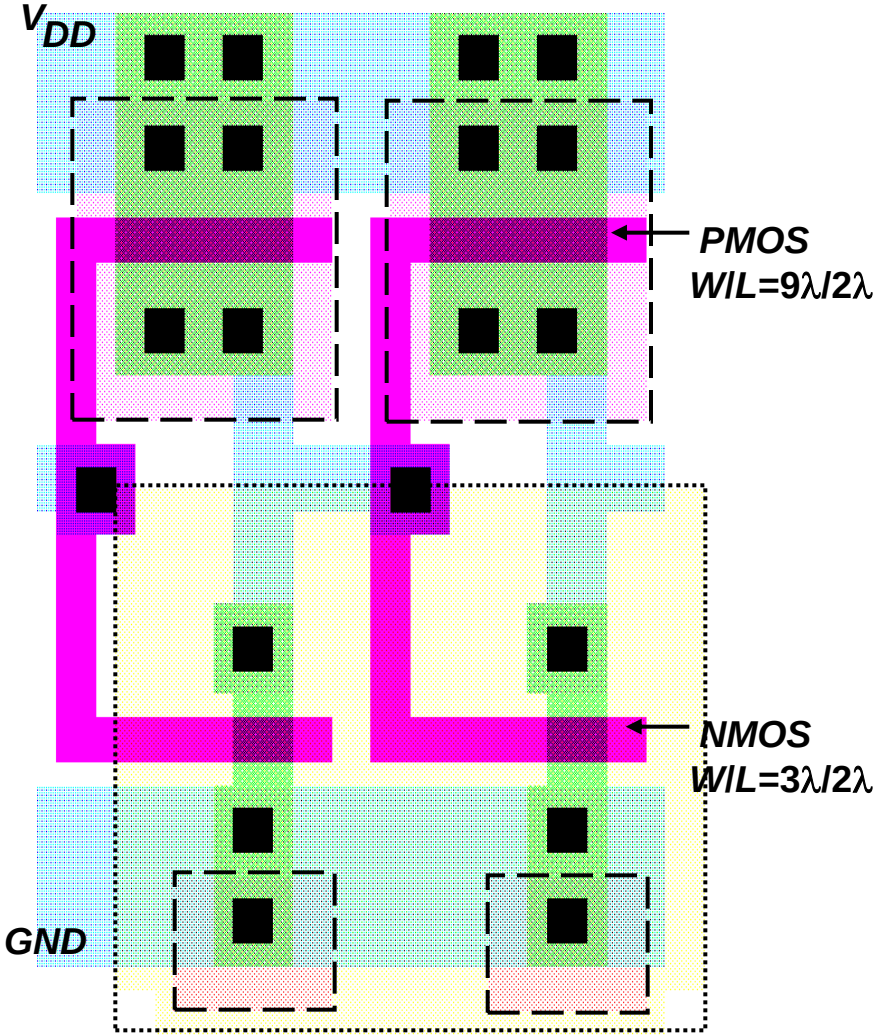
CMOS Inverter Layout





Note body contacts:

- p-well to GND
- n-substrate to V_{DD}

P-well mask
(dark field)

Active
(clear field)

Gate
(clear field)

Select mask
(dark field & clear field)

Contact
(dark field)

Metal
(clear field)

Visualizing Layouts and Cross-Sections with SIMPLer

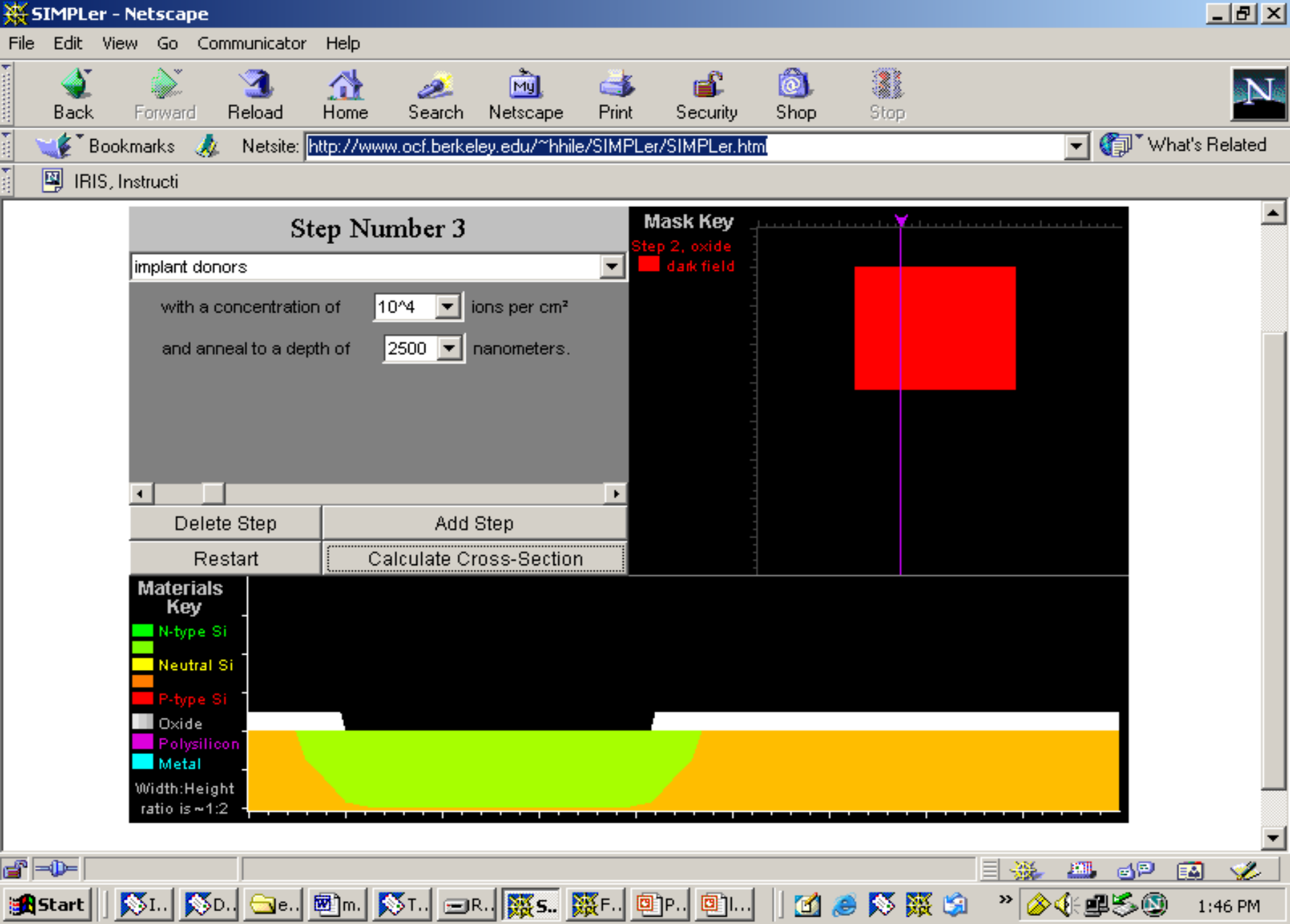
SIMPL is a CAD tool created by Prof. Neureuther's group

- allows IC designers to visualize device cross-sections corresponding to a fabrication process and physical layout.

A Berkeley undergraduate student, Harlan Hile, created a mini-version of SIMPL (called SIMPLer) for EE40.

- It's a JAVA program -> can be run on any computer, as well as on a web server.
- A 3D version SIMPL-GL can be accessed at

http://cuervo2.eecs.berkeley.edu/Volcano/simpl_gl/main.htm


SIMPLer - Netscape
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Bookmarks Netsite: http://www.ocf.berkeley.edu/~hhile/SIMPLer/SIMPLer.htm What's Related
IRIS, Instructi
Step Number 3
implant donors
with a concentration of 10^4 ions per cm²
and anneal to a depth of 2500 nanometers.
Delete Step
Add Step
Restart
Calculate Cross-Section
Mask Key
Step 2, oxide
dark field
Materials Key
N-type Si
Neutral Si
P-type Si
Oxide
Polysilicon
Metal
Width:Height ratio is ~1:2
Start
1:46 PM

SIMPLer - Netscape

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Bookmarks Netsite: http://www.ocf.berkeley.edu/~hhile/SIMPLer/SIMPLer.htm What's Related

IRIS, Instructi

Step Number 12

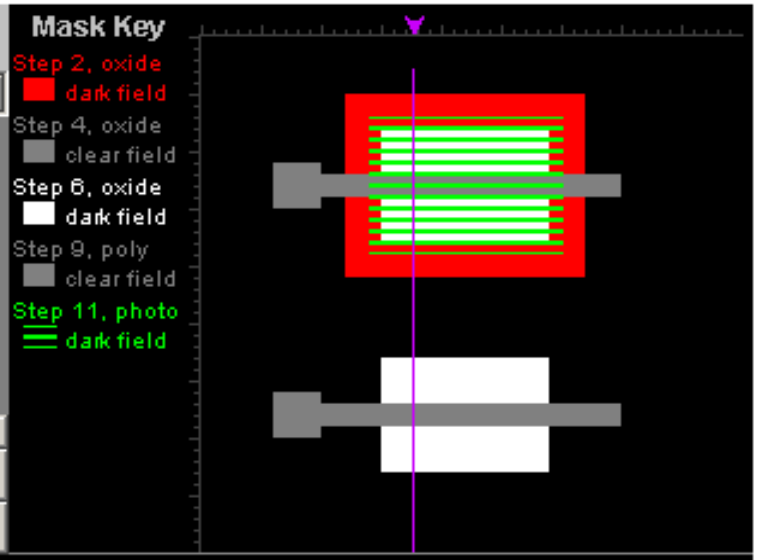
implant acceptors

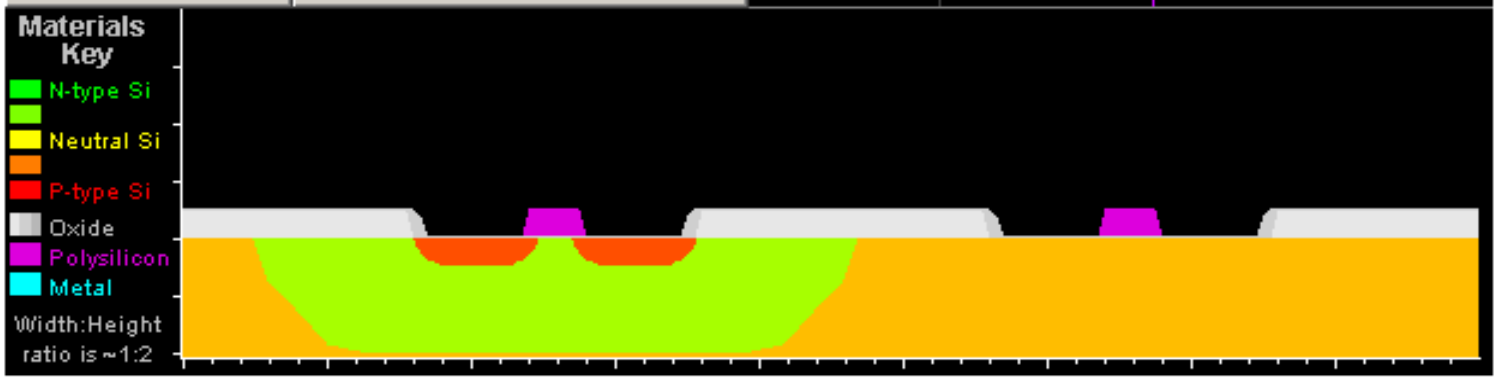
with a concentration of 10^12 ions per cm²

and anneal to a depth of 500 nanometers.

Delete Step | Add Step

Restart | Calculate Cross-Section





Start 1:39 PM

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IRIS, Instructi

Step Number 15

implant donors

with a concentration of 10^12 ions per cm²

and anneal to a depth of 500 nanometers.

Delete Step | Add Step

Restart | Calculate Cross-Section

Mask Key

Step 2, oxide — dark field

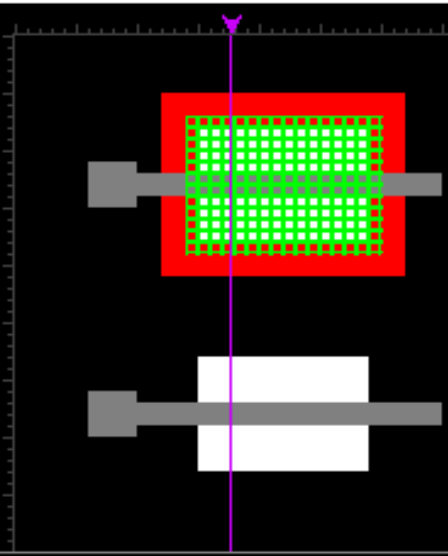
Step 4, oxide — clear field

Step 6, oxide — dark field

Step 9, poly — clear field

Step 11, photo — dark field

Step 14, photo — clear field



Materials Key

N-type Si

Neutral Si

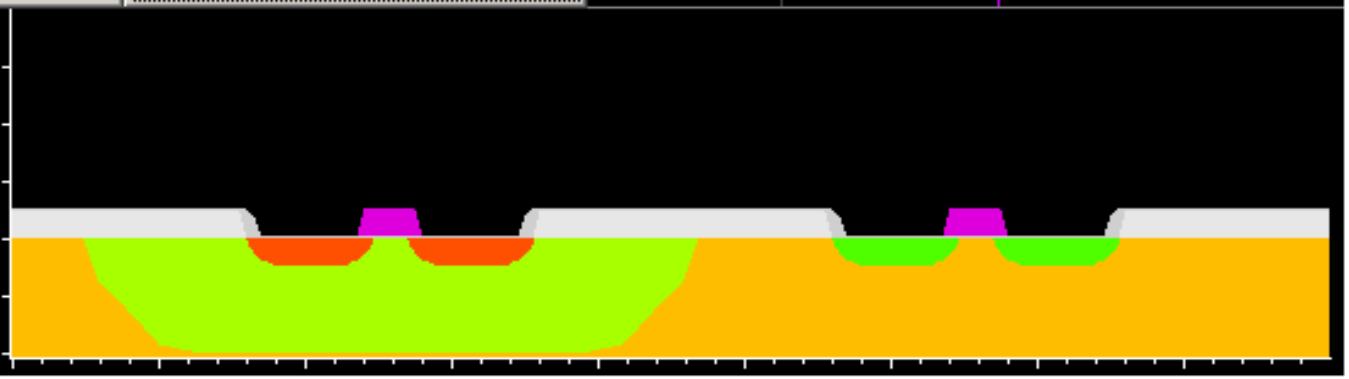
P-type Si

Oxide

Polysilicon

Metal

Width:Height ratio is ~1:2



Print this page

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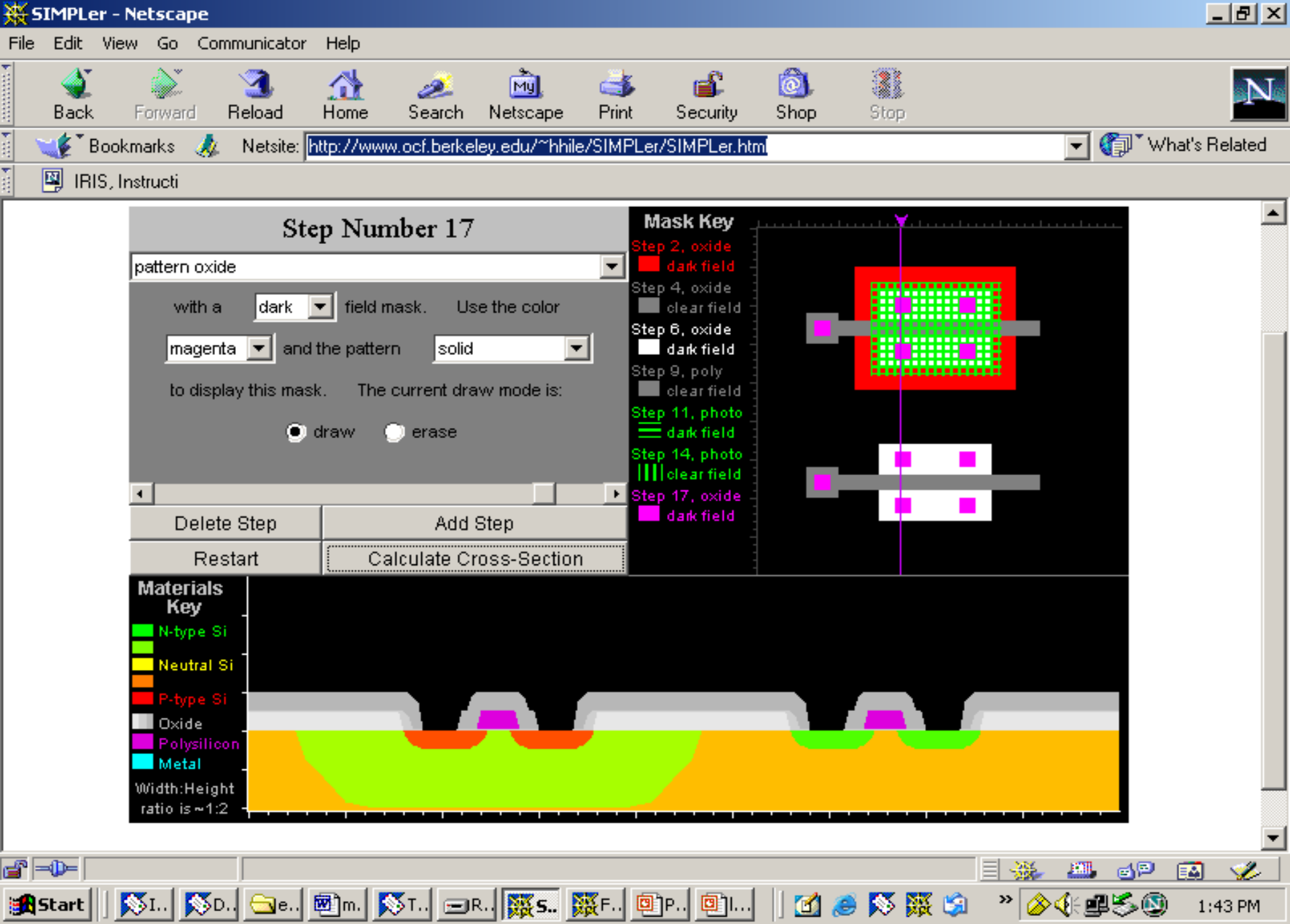
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Bookmarks Netsite: http://www.ocf.berkeley.edu/~hhile/SIMPLer/SIMPLer.htm What's Related
IRIS, Instructi
Step Number 17
pattern oxide
with a dark field mask. Use the color
magenta and the pattern solid
to display this mask. The current draw mode is:
draw erase
Delete Step
Add Step
Restart
Calculate Cross-Section
Mask Key
Step 2, oxide
dark field
Step 4, oxide
clear field
Step 6, oxide
dark field
Step 9, poly
clear field
Step 11, photo
dark field
Step 14, photo
clear field
Step 17, oxide
dark field
Materials Key
N-type Si
Neutral Si
P-type Si
Oxide
Polysilicon
Metal
Width:Height ratio is ~1:2
Start
1:43 PM

SIMPLer - Netscape

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Bookmarks Netsite: http://www.ocf.berkeley.edu/~hhile/SIMPLer/SIMPLer.htm What's Related

IRIS, Instructi

Step Number 19

pattern metal

with a clear field mask. Use the color

cyan and the pattern X's

to display this mask. The current draw mode is:

draw erase

Delete Step | Add Step

Restart | Calculate Cross-Section

Mask Key

Step 2, oxide
dark field

Step 4, oxide
clear field

Step 6, oxide
dark field

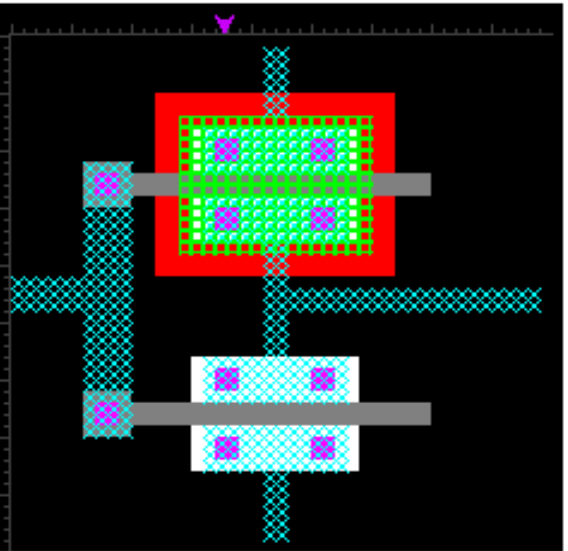
Step 9, poly
clear field

Step 11, photo
dark field

Step 14, photo
clear field

Step 17, oxide
dark field

Step 19, metal
clear field



Materials Key

N-type Si

Neutral Si

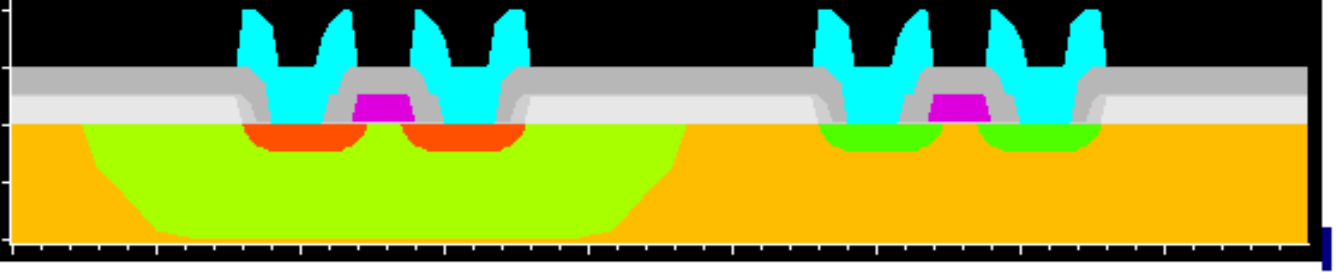
P-type Si

Oxide

Polysilicon

Metal

Width:Height ratio is ~1:2



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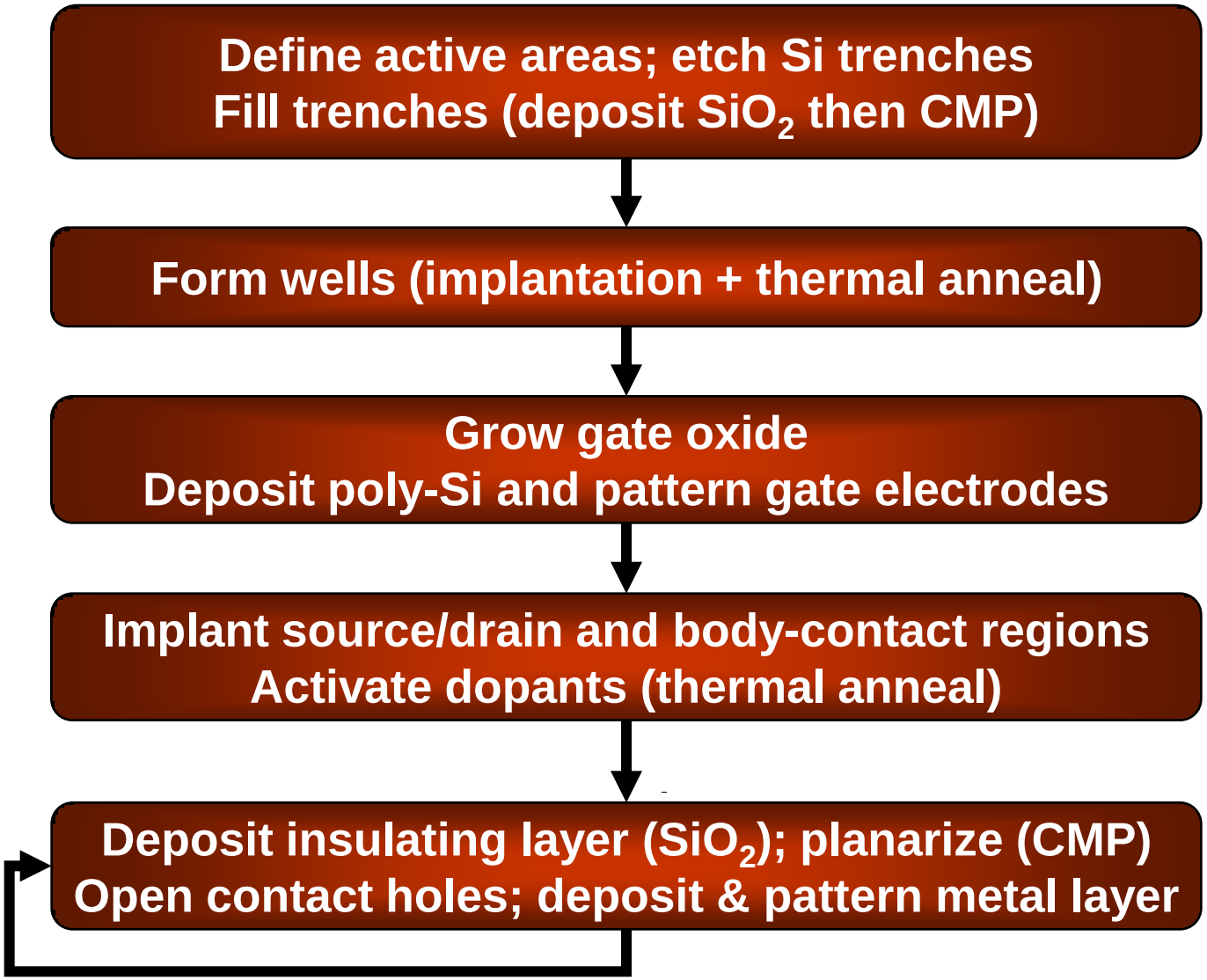
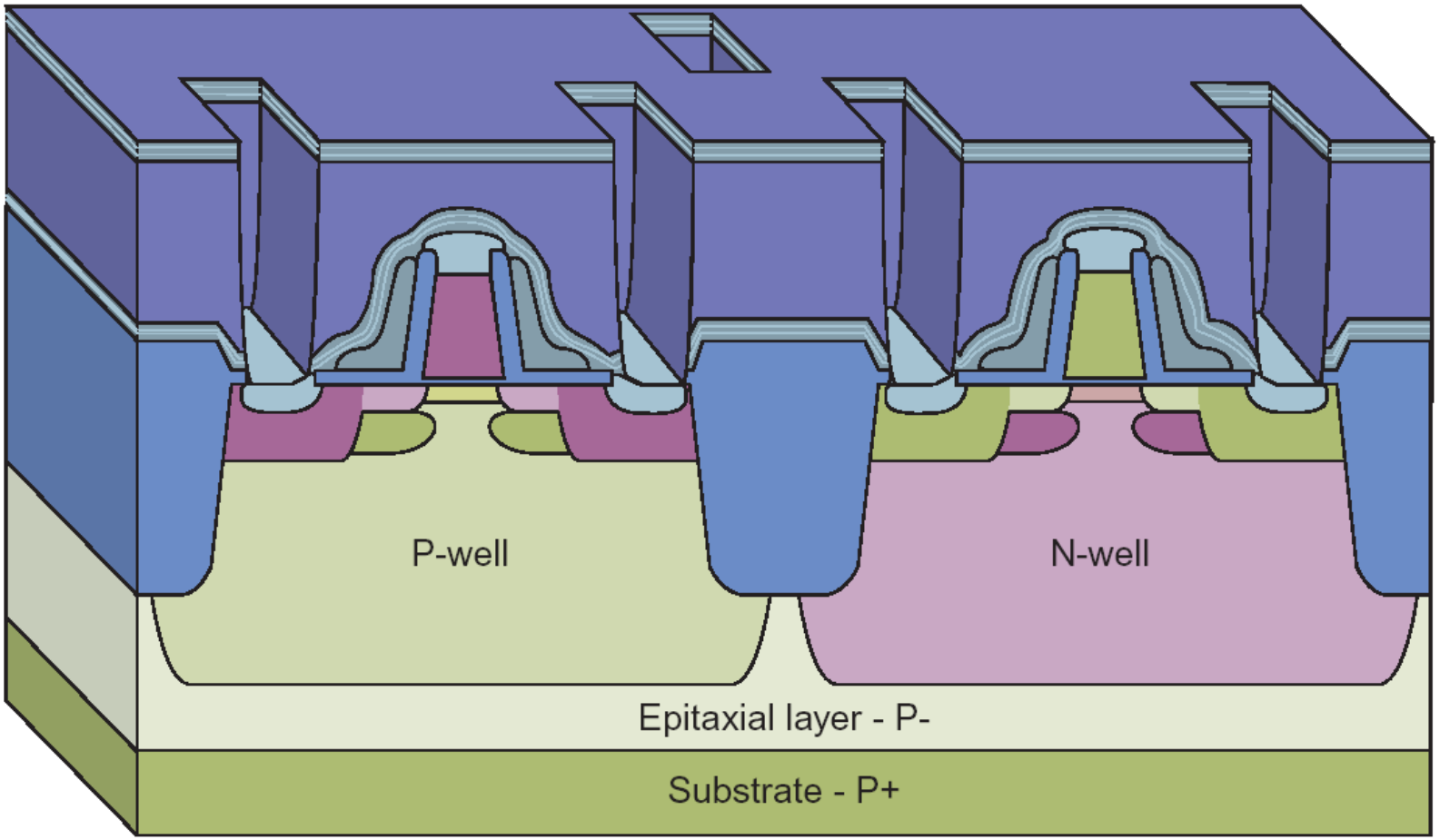
Twin Well + STI CMOS Process



3D view of a CMOS inverter after contact etch.

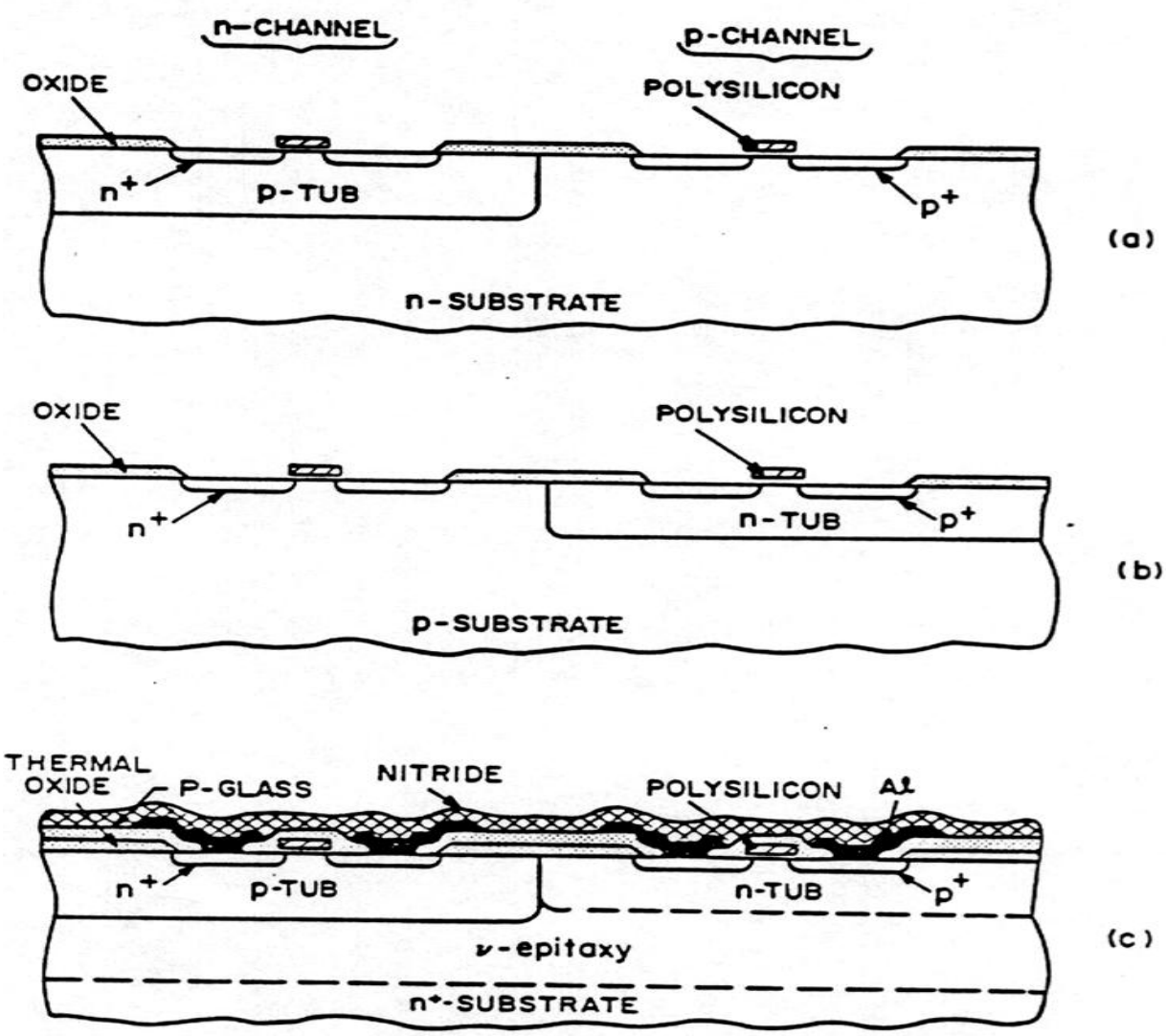


Well Engineering

P-tub

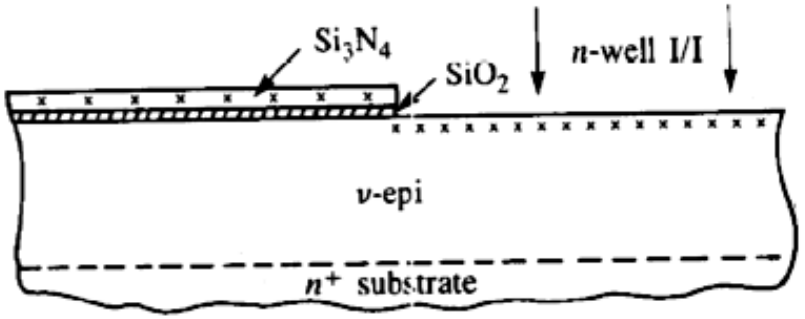
N-tub

Twin Tub

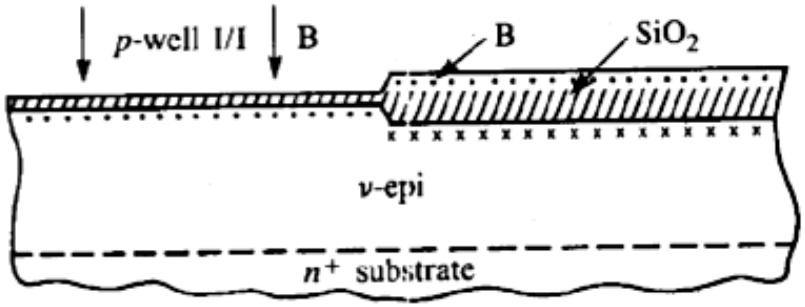


Various CMOS structures. (a) p tub. (b) n tub. (c) twin tub.

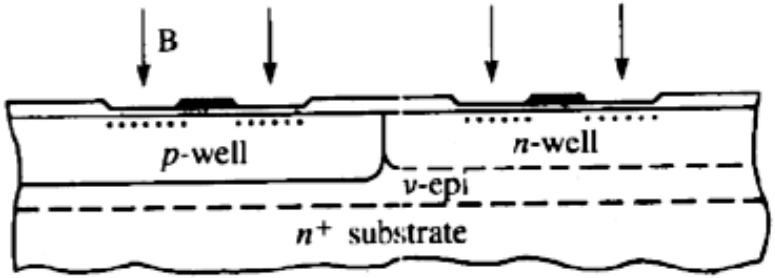
Twin Well CMOS Process Flow



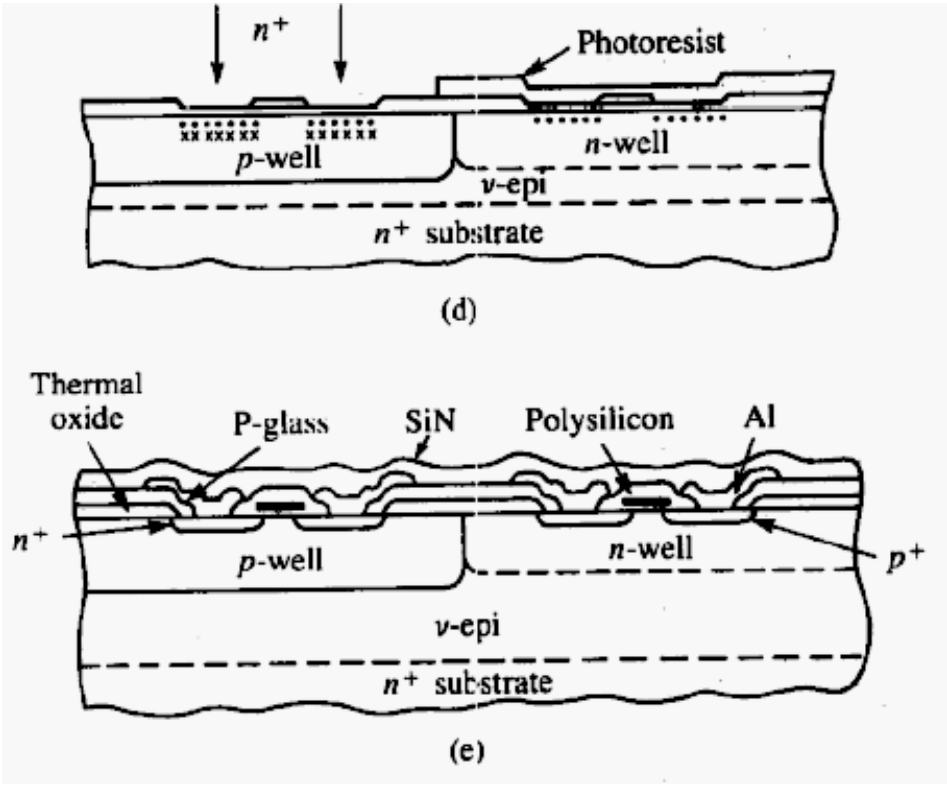
(a)



(b)



(c)

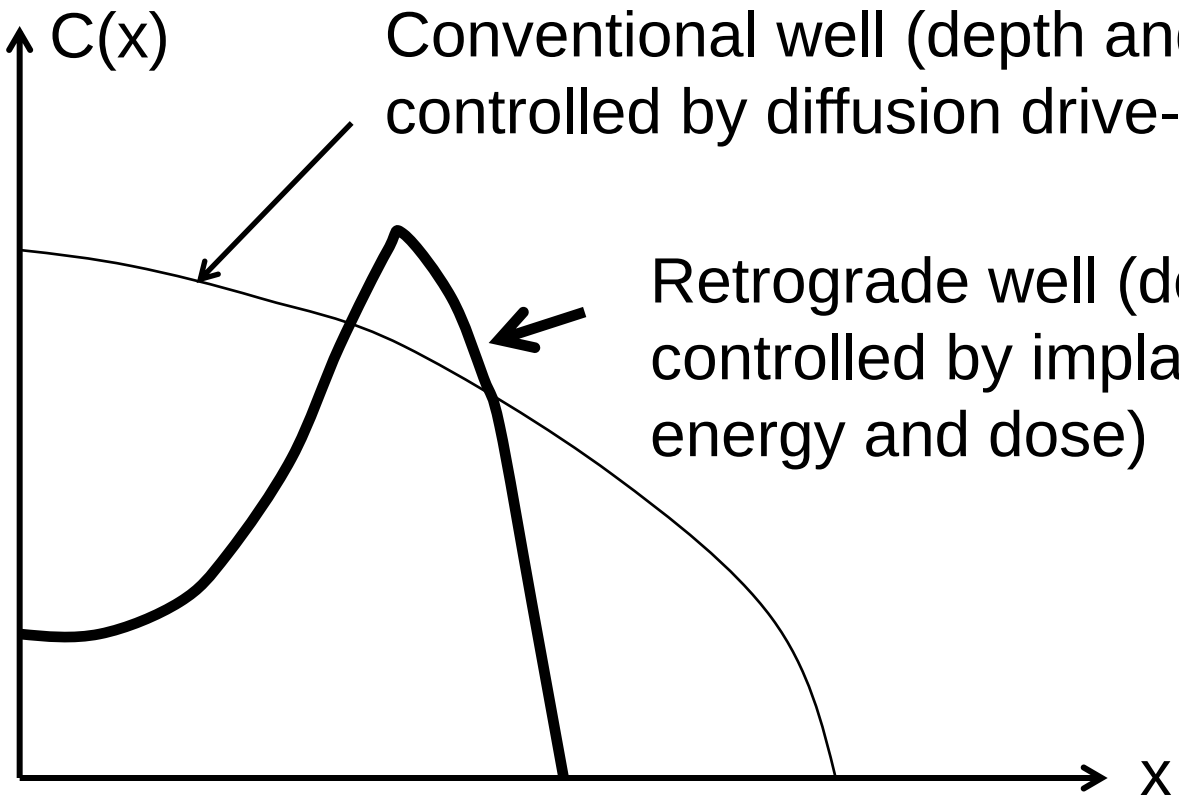


(d)

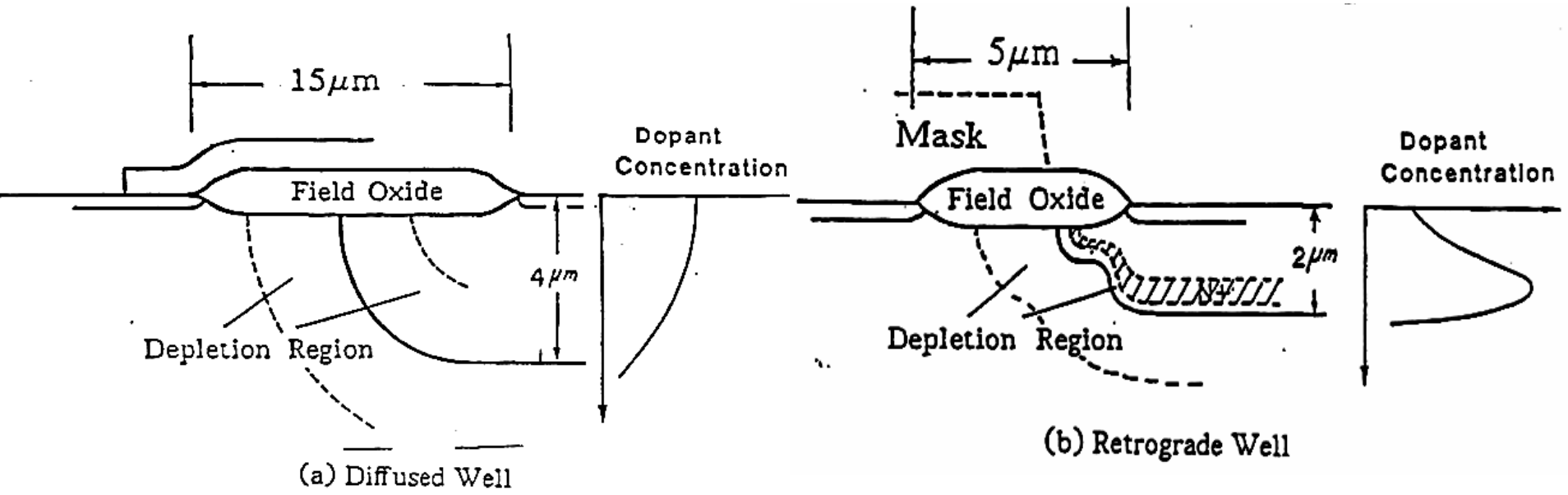
(e)

Retrograde Well

- formed by high energy (>200keV) implantation



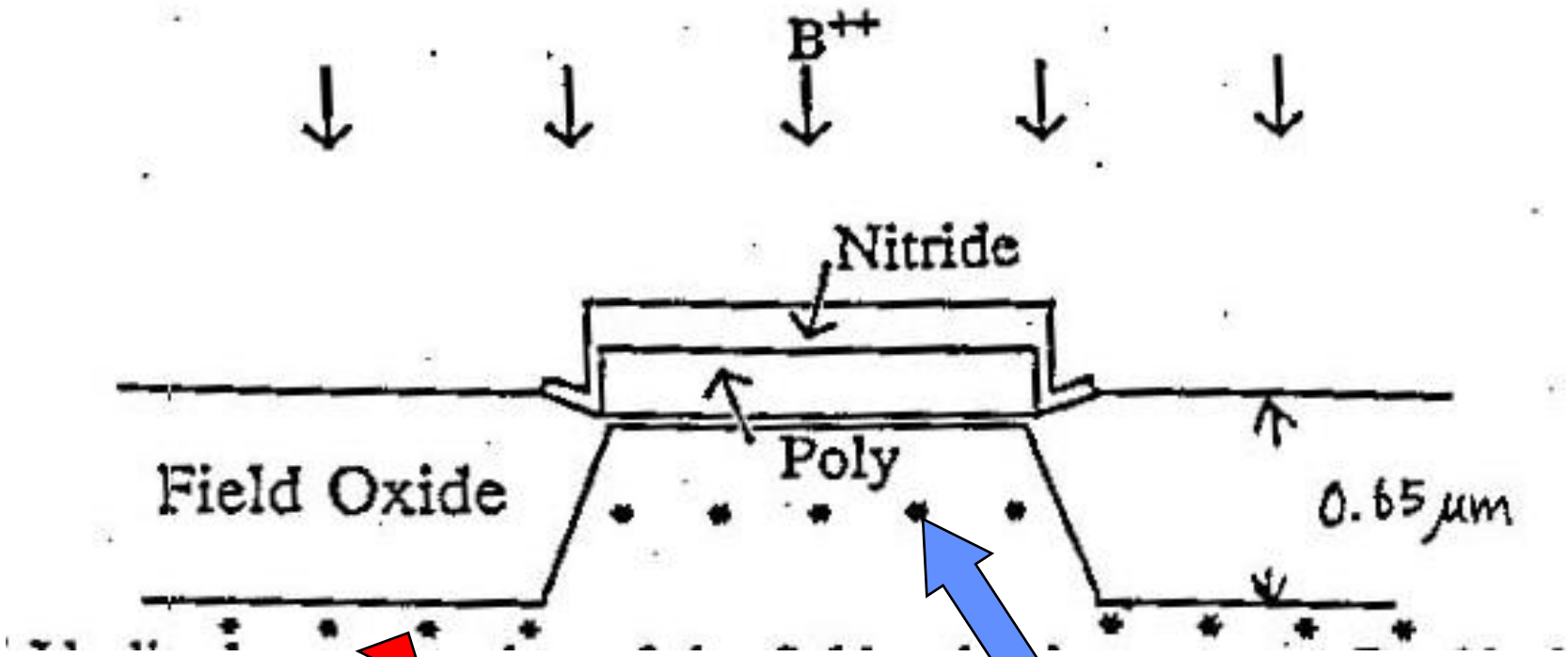
Conventional vs Retrograde Well



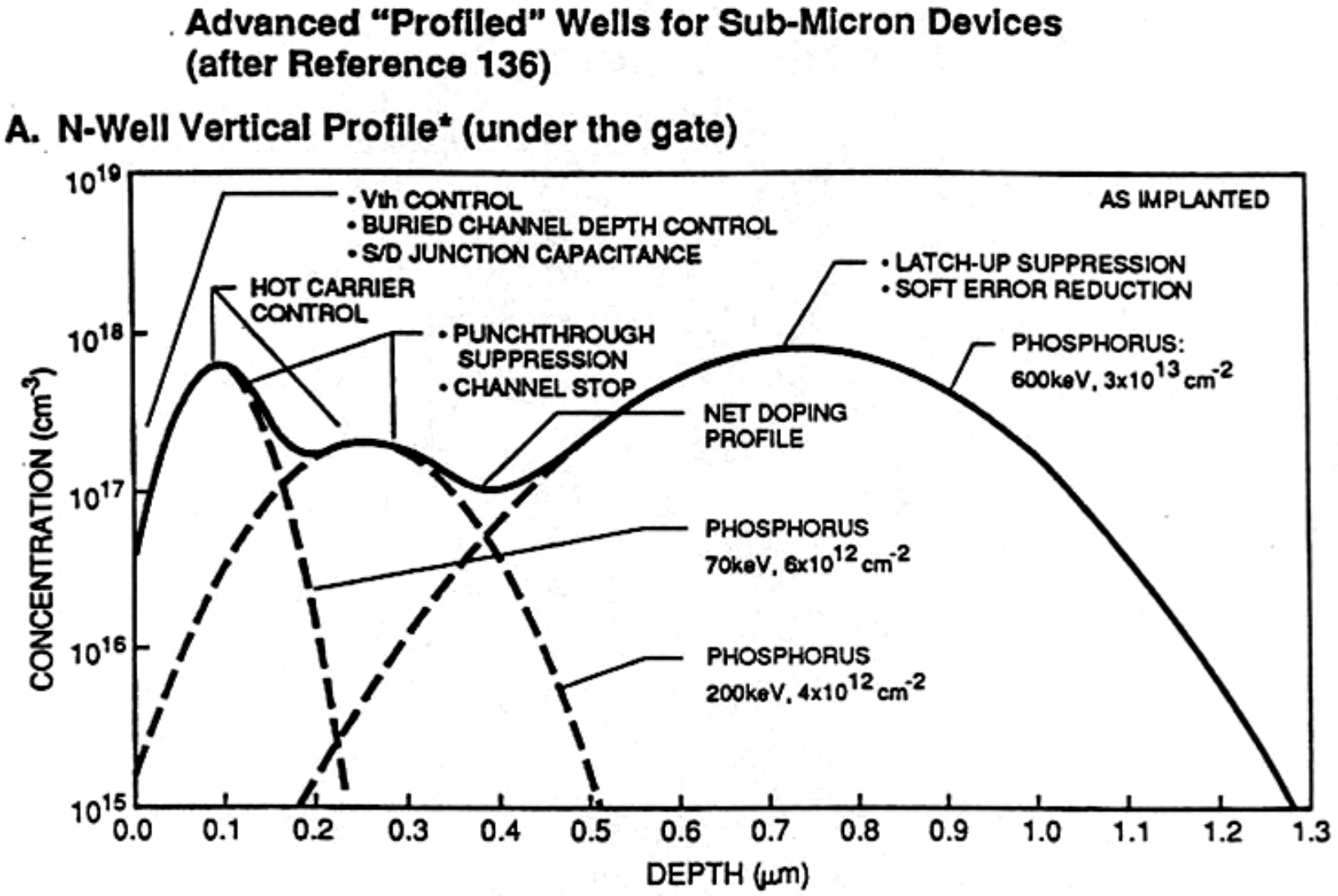
1) Very low thermal budget for well formation
(no need for diffusion drive-in)

2) Retrograde Well is formed AFTER field oxidation
$\Rightarrow$ small lateral diffusion and localized high conc under FOX

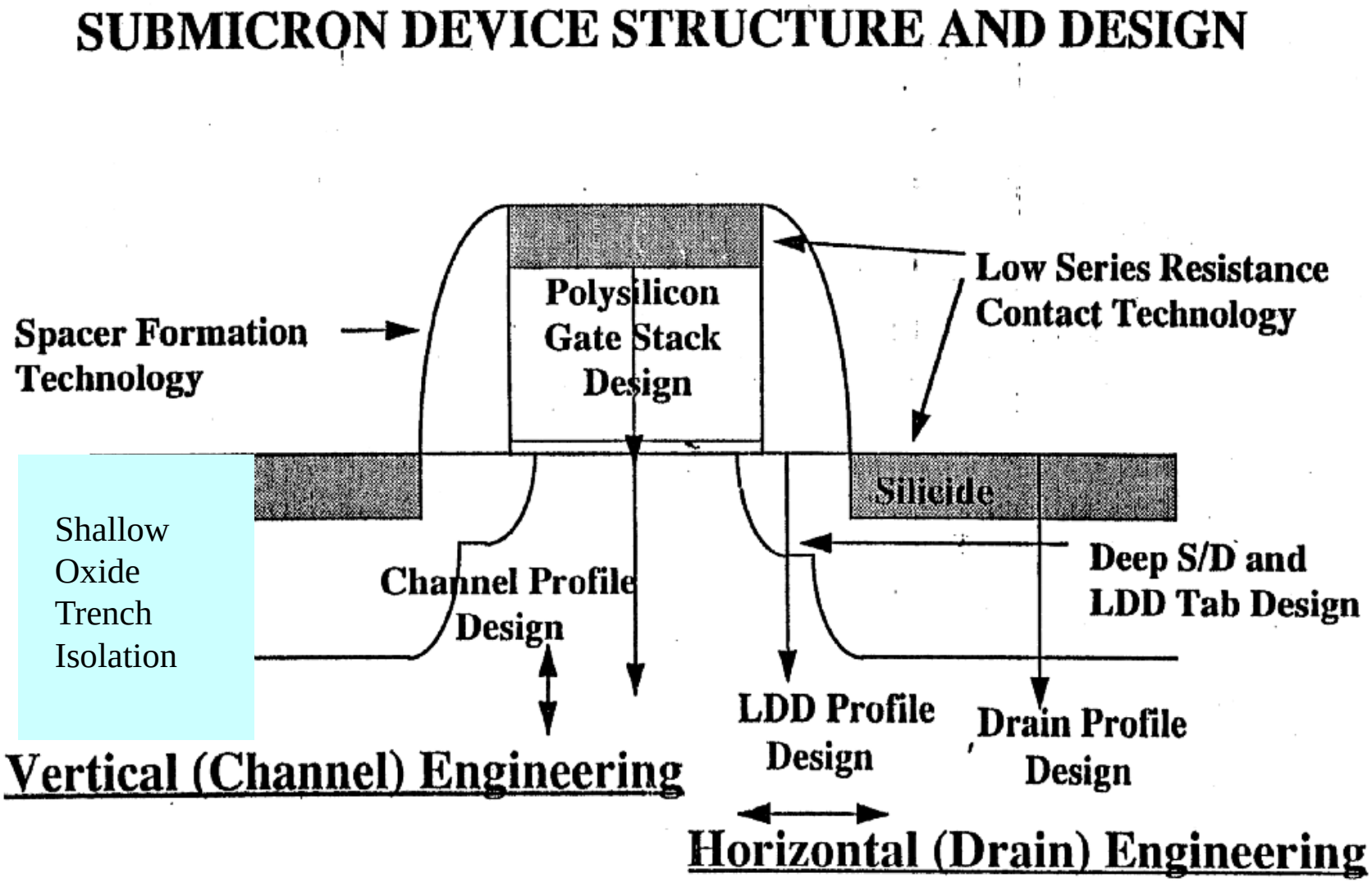
Example: Formation of Channel Stop and Retrograde Well in a single step



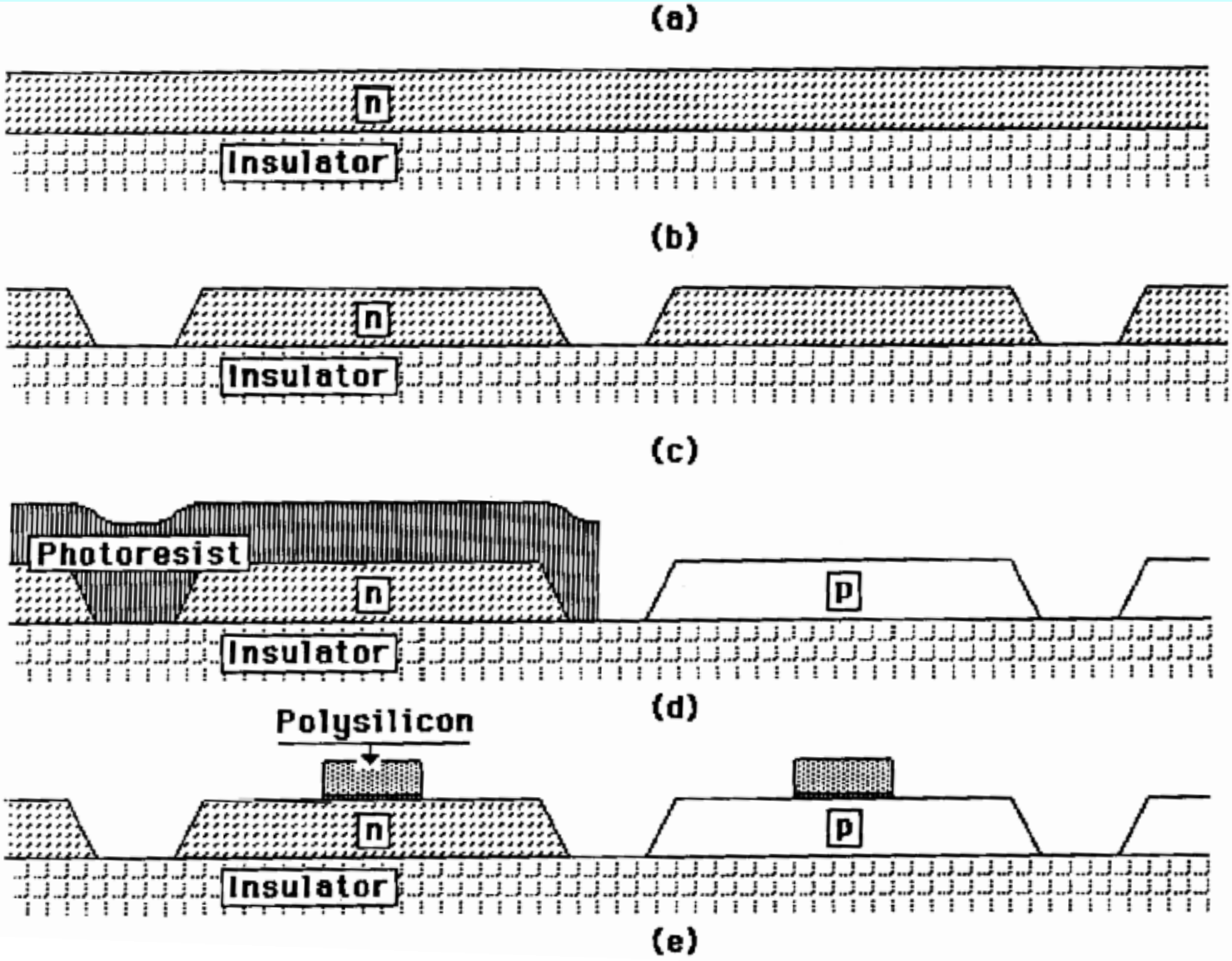
Multiple Implants for Well Engineering



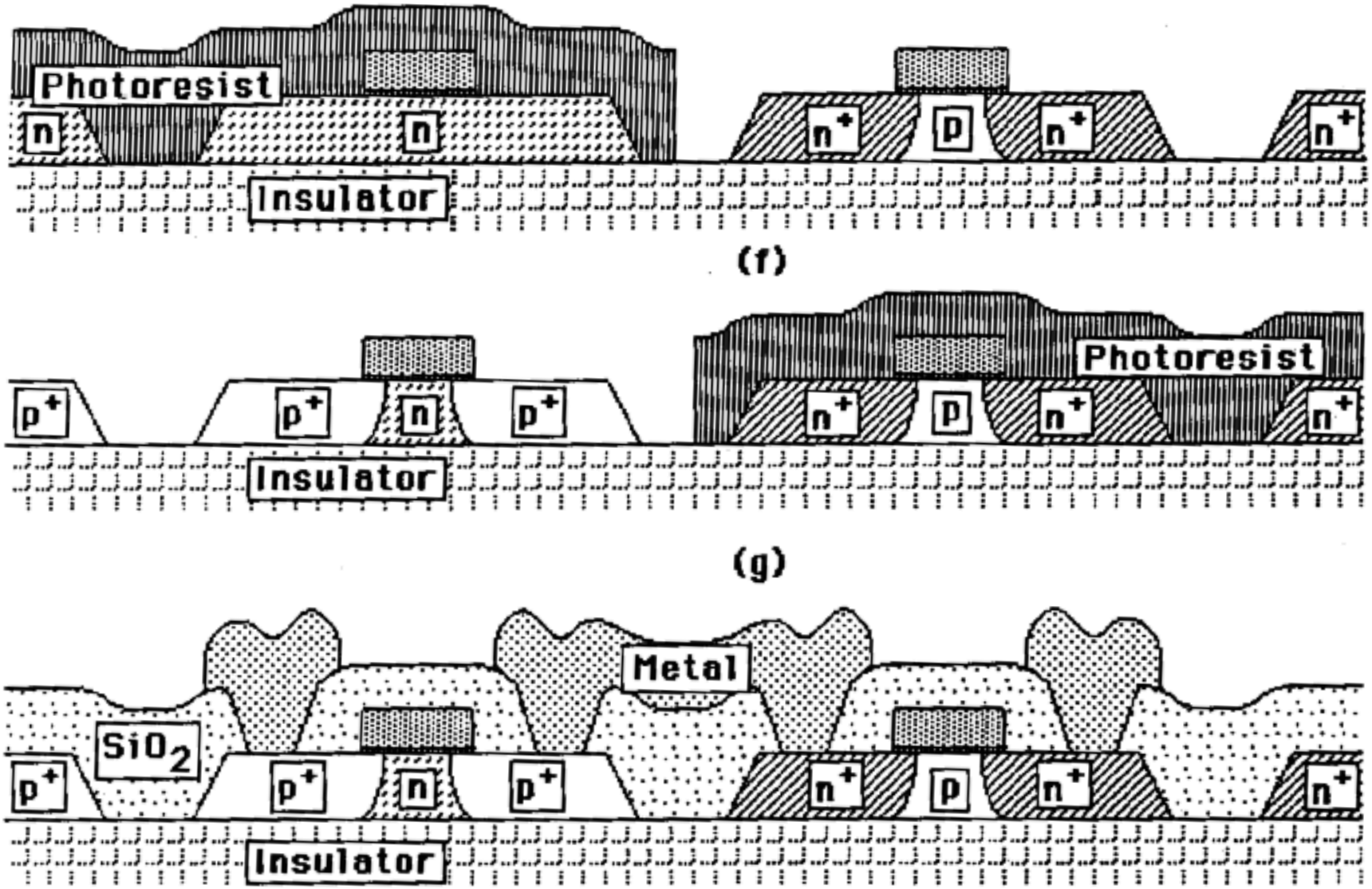
Channel Engineering



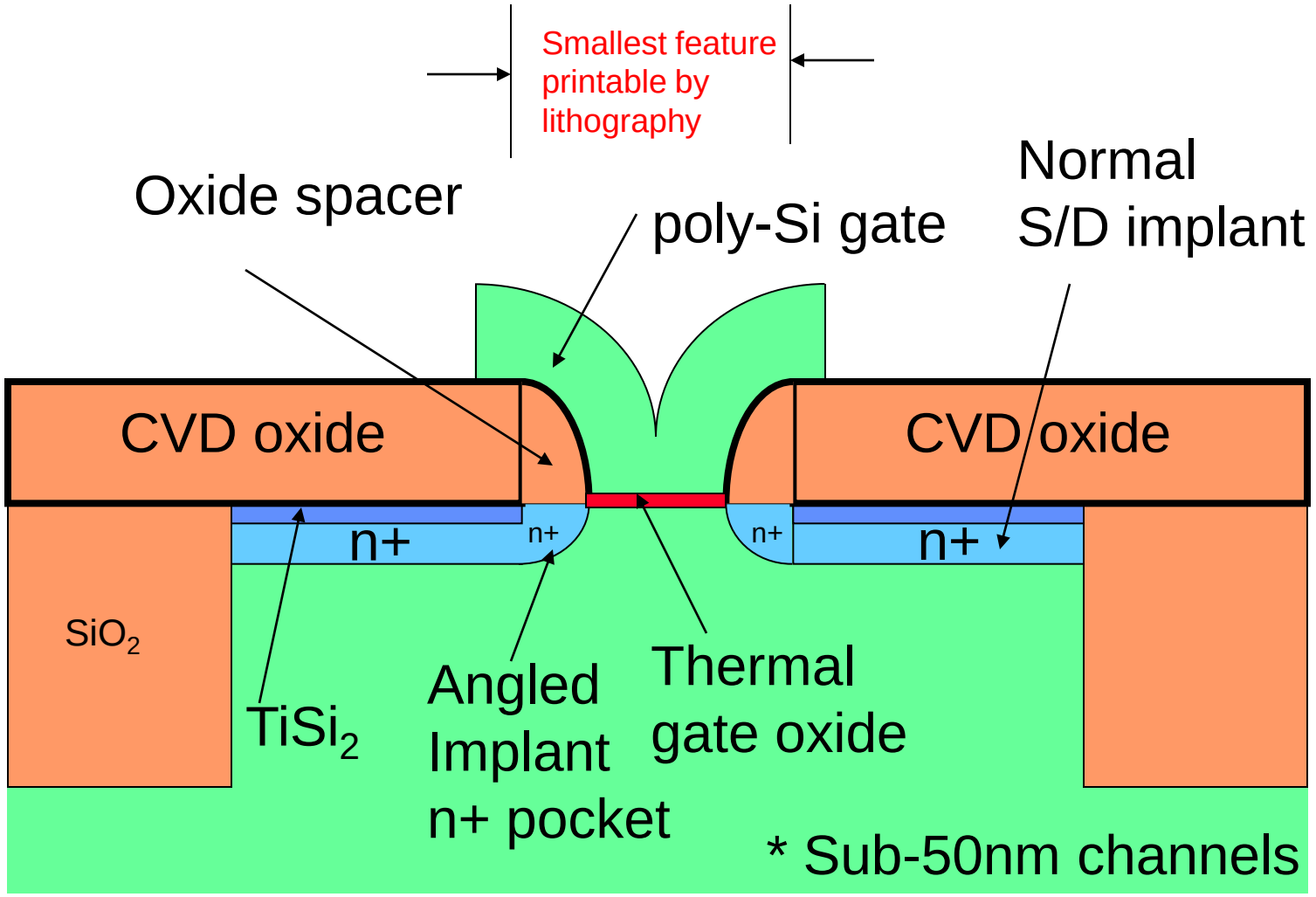
Generic Silicon-on-Insulator (SOI) CMOS Process Flow



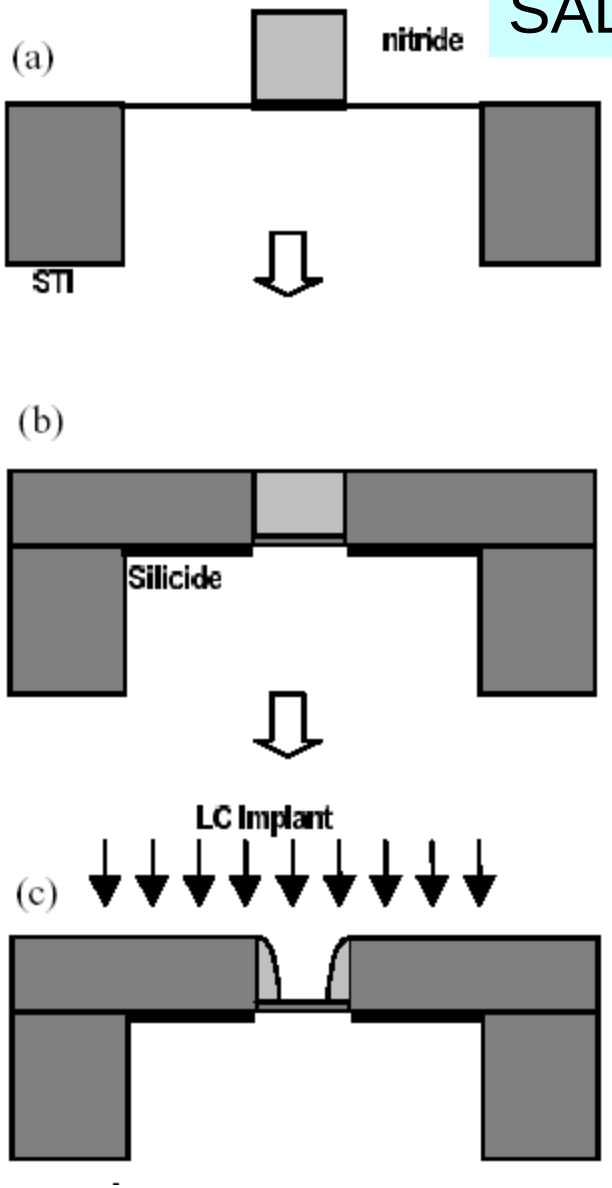
SOI Process Flow (continued)

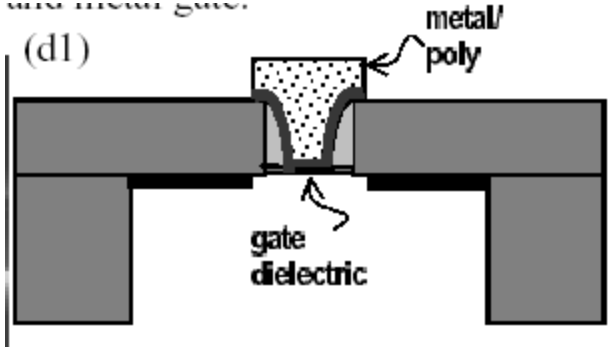


Self-Aligned Channel V-gate by Optical Lithography (SALVO) Process

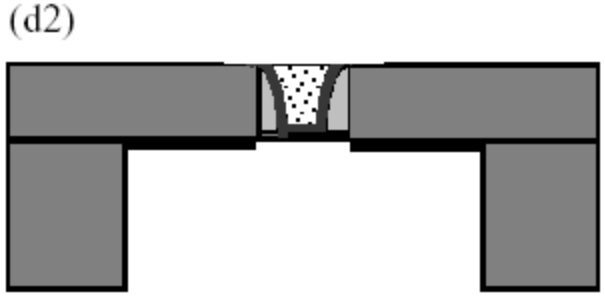


SALVO Process Flow





or



See Homework Problem

Chang et al, IEDM 2000

SUMMARY OF IC PROCESS INTEGRATION MODULE

- Self aligned techniques: channel stop, Source/Drain, LDD, SALICIDE
- How to read process flow descriptions and cross-sections
- Generic NMOS Process with LOCOS
- Generic CMOS Process with LOCOS and single well
- Modified Processes:
- Shallow Trench Isolation (STI), Twin Wells, Retrograde Well, SOI CMOS