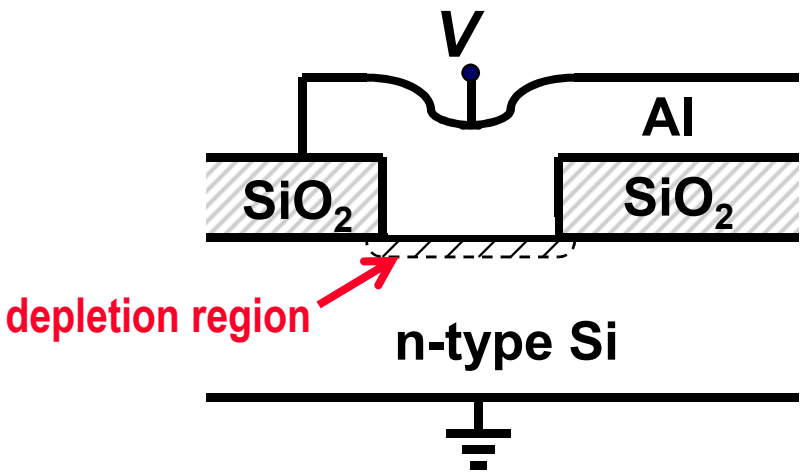
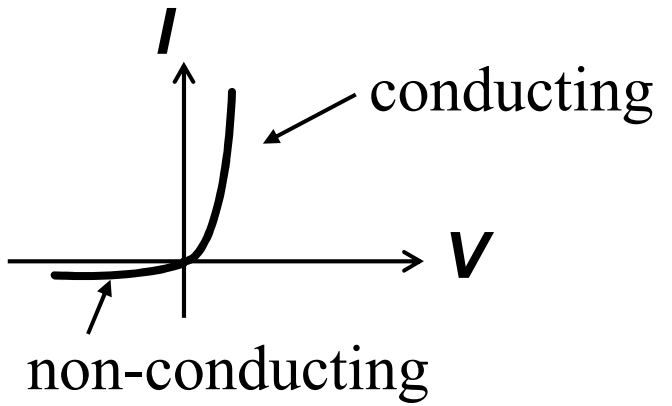
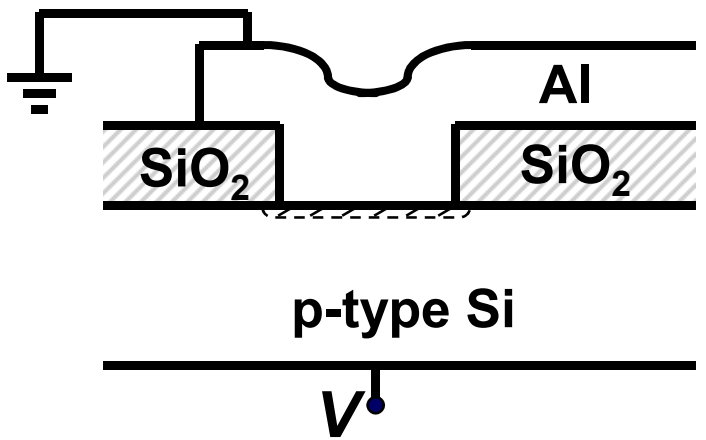
Electrical Contacts to Si

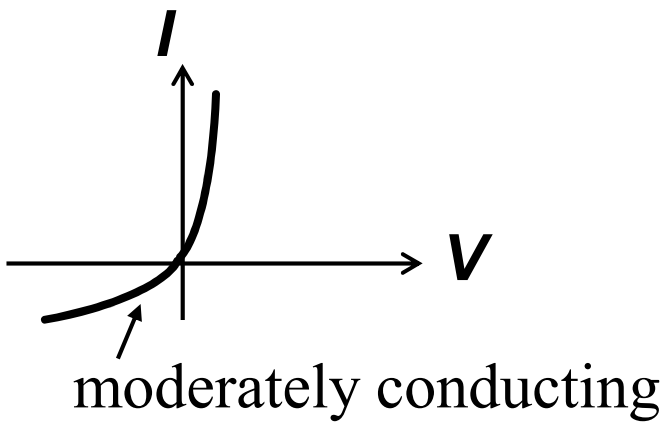
(1) Schottky (rectifying) contacts:





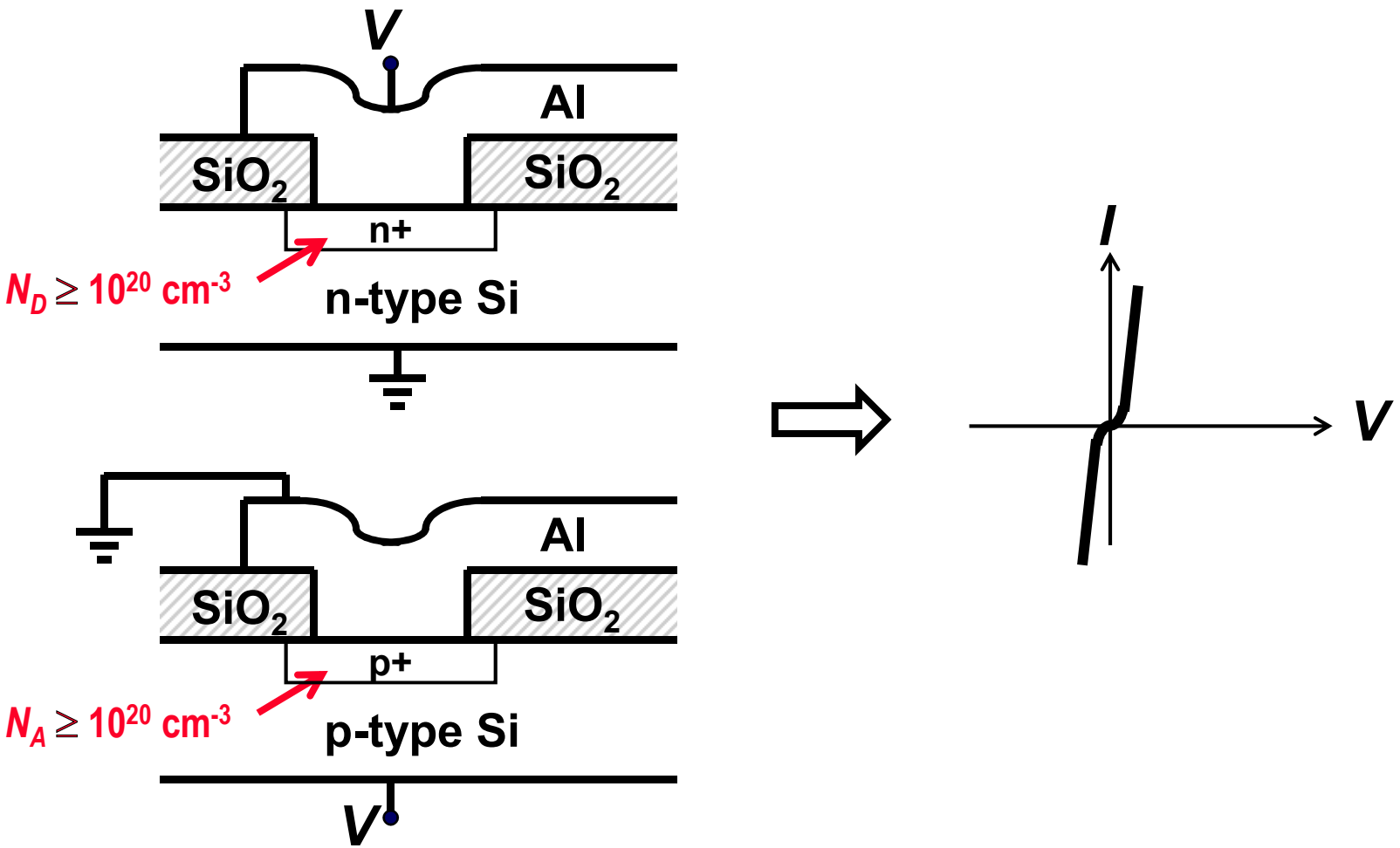
Majority carriers cannot move easily from the metal into the n-Si, due to a large potential barrier. For the same metal, this potential barrier is smaller for contacts to p-type Si.





The depth of the depletion region (x_d) decreases with increasing dopant concentration. For very high doping, x_d is small enough (<10nm) to allow quantum tunneling of carriers.

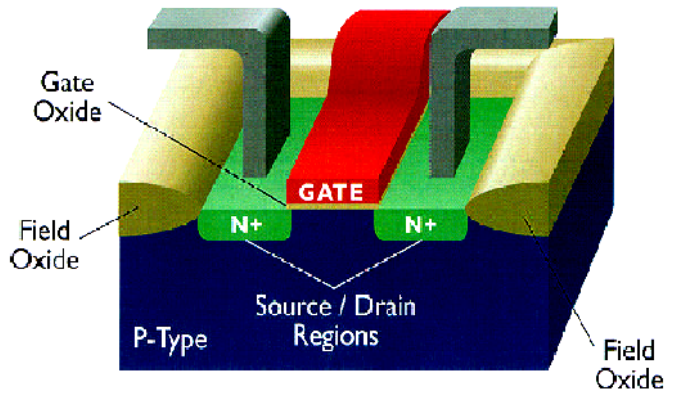
(2) Tunneling "ohmic" contacts:



Monolithic Integration: *Planar Technology*

starting substrate + *planar processing steps = monolithic integration of multiple devices

Si wafer



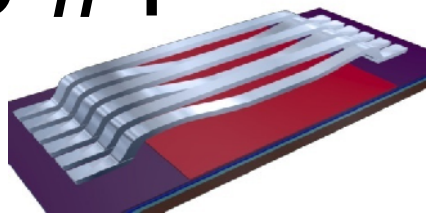
n-channel MOSFET

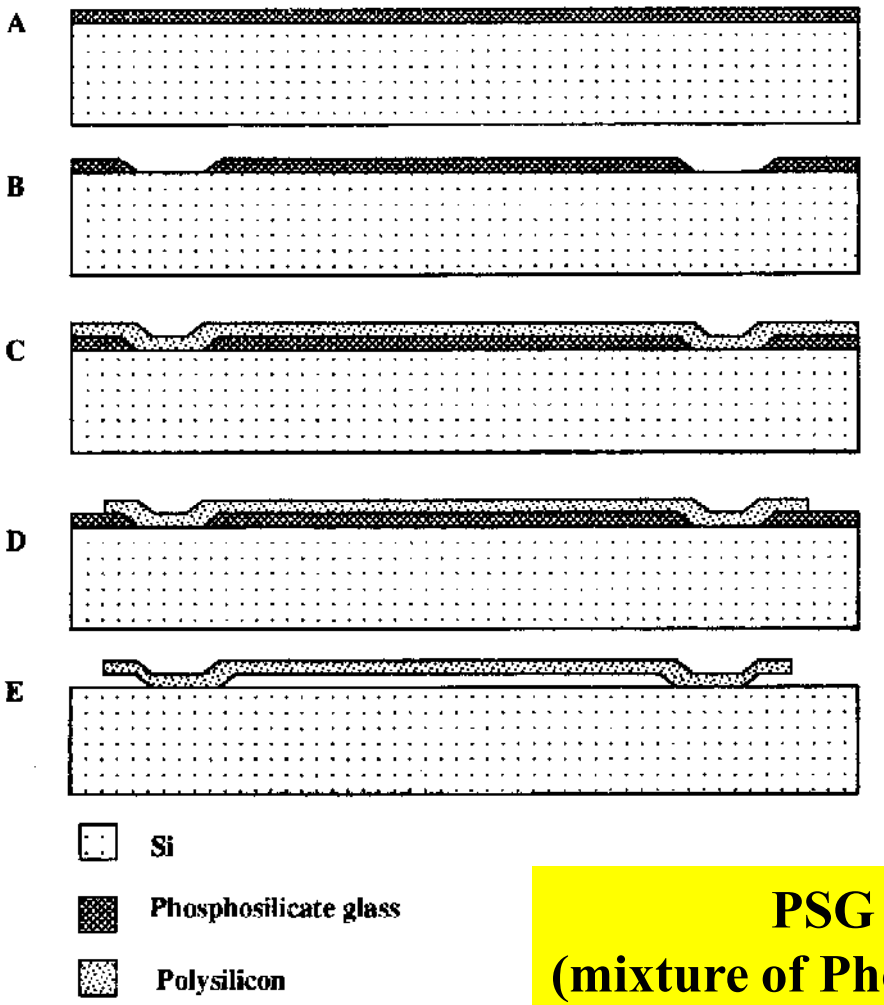
*sequence of **additive** and **subtractive** steps with **lateral patterning**

- **additive**: **e.g. oxidation, deposition, ion implantation**
- **subtractive**: **e.g. etching**
- **lateral patterning**: **e.g. lithography**

Process Flow Example #1

Suspended Beam Array





Doped oxide (PSG) deposition (CVD)
(blanket addition)

Anchor patterning (litho. & etch)
(patterned subtraction)

Poly-Si deposition
(blanket addition)

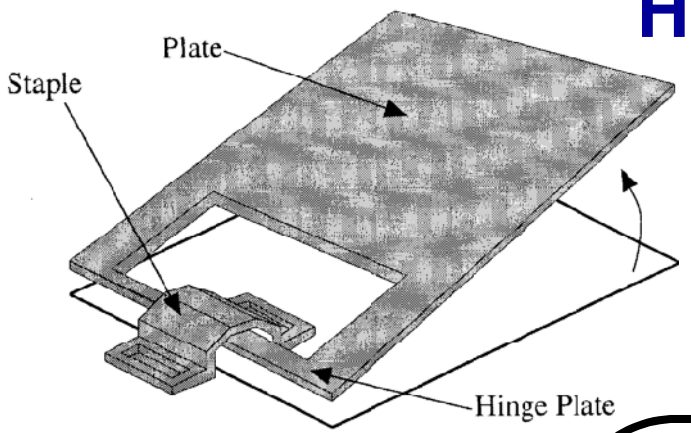
Poly-Si beam patterning (litho. & etch)
(patterned subtraction)

Selective etch of PSG
(blanket subtraction)

PSG = PhosphoSilicate Glass
(mixture of Phosphorus oxide and Silicon Oxide prepared by CVD)

Process Flow Example #2

Hinged Structure

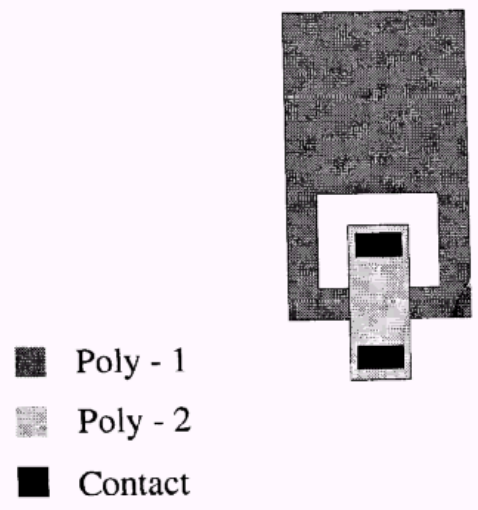


→ *out-of-plane movement*

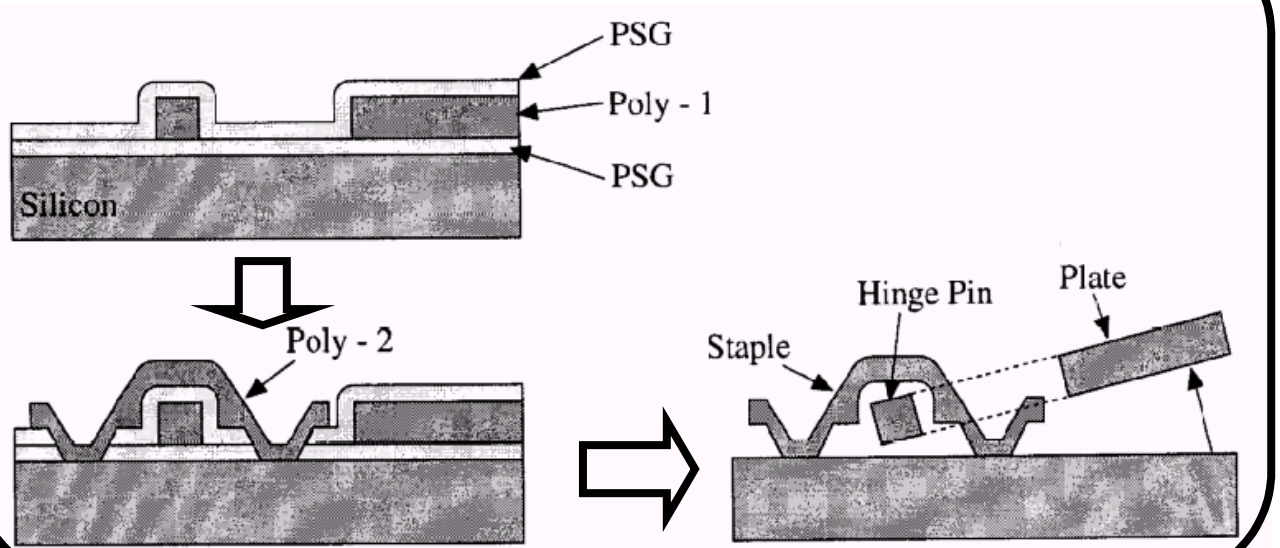
3 Lithography steps:

1) Hinge pattern
2) Staple anchor pattern
3) Staple pattern

Top view of masks

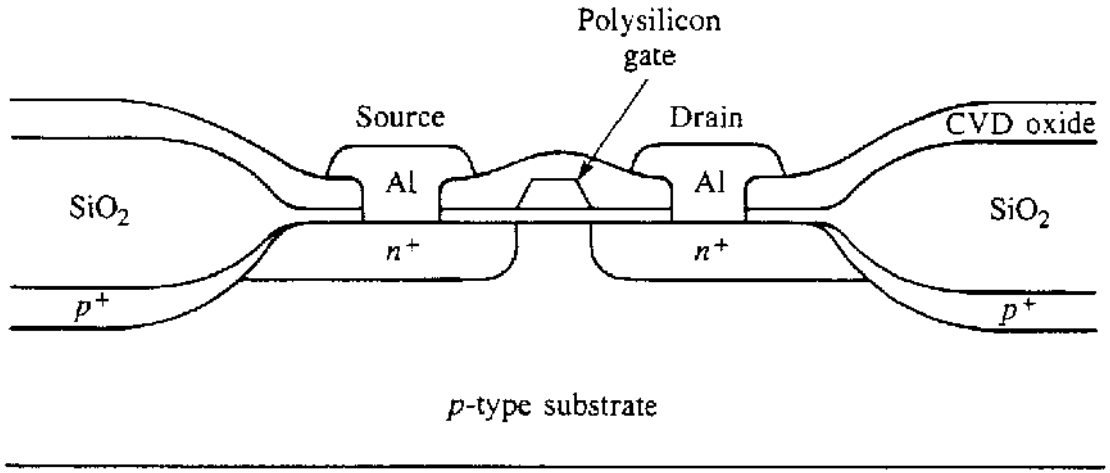


Cross-sectional views

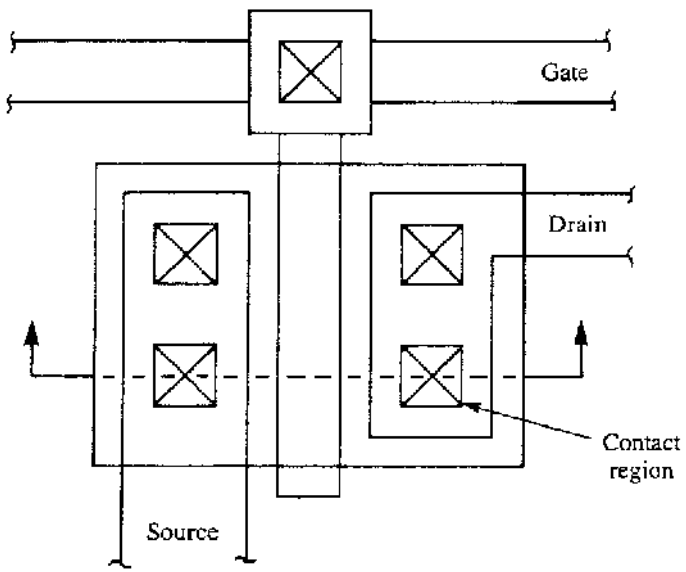


N-channel MOSFET

Schematic Cross-Sectional View



Layout (Top View)



4 lithography steps are required:

1. active area
2. gate electrode
3. contacts
4. metal interconnects

Process Flow Example #3

Simple nMOSFET Process Flow

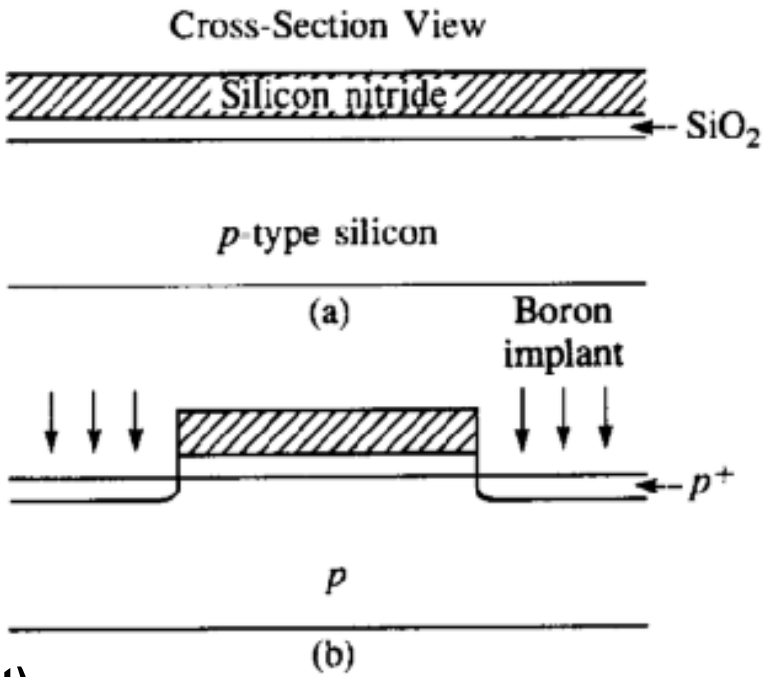
Read Jaeger (textbook) Chap 1 for narrative description

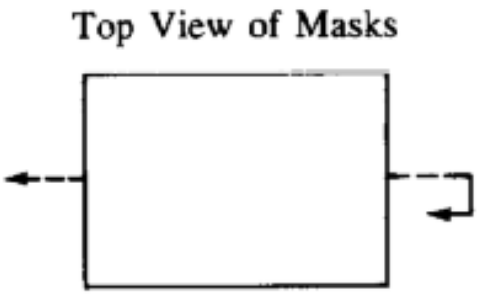
1) Thermal oxidation (~10 nm "pad oxide")

2) Silicon-nitride (Si_3N_4) deposition by CVD (~40nm)

3) Active-area definition (lithography & etch)

4) Boron ion implantation ("channel stop" implant)



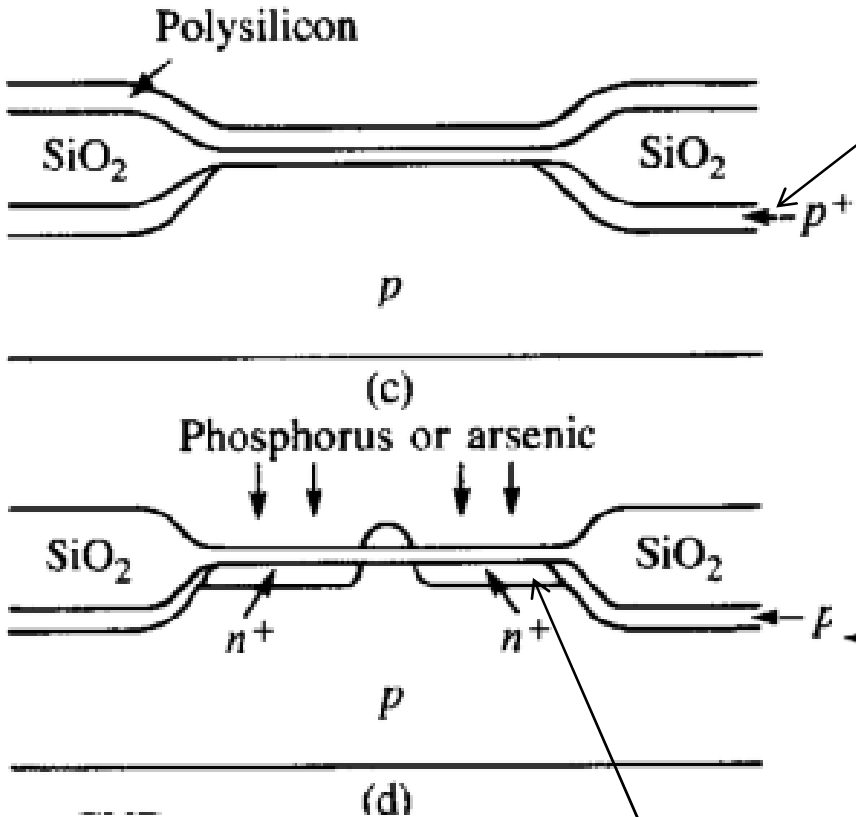


Process Flow Example #3 - cont

5) Thermal oxidation to grow oxide in "field regions"
6) Si_3N_4 & pad oxide removal
7) Thermal oxidation ("gate oxide")
8) Poly-Si deposition by CVD

9) Poly-Si gate-electrode patterning (litho. & etch)

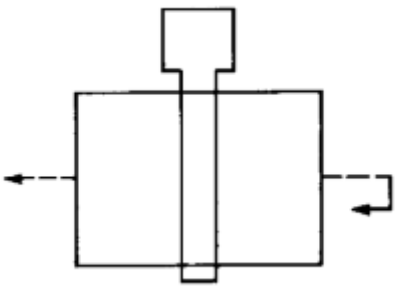
10) P or As ion implantation to form n+ source and drain regions



Doping Concentration ~$10^{17}/cm^3$

Doping Concentration ~$10^{20}/cm^3$

Top view of masks



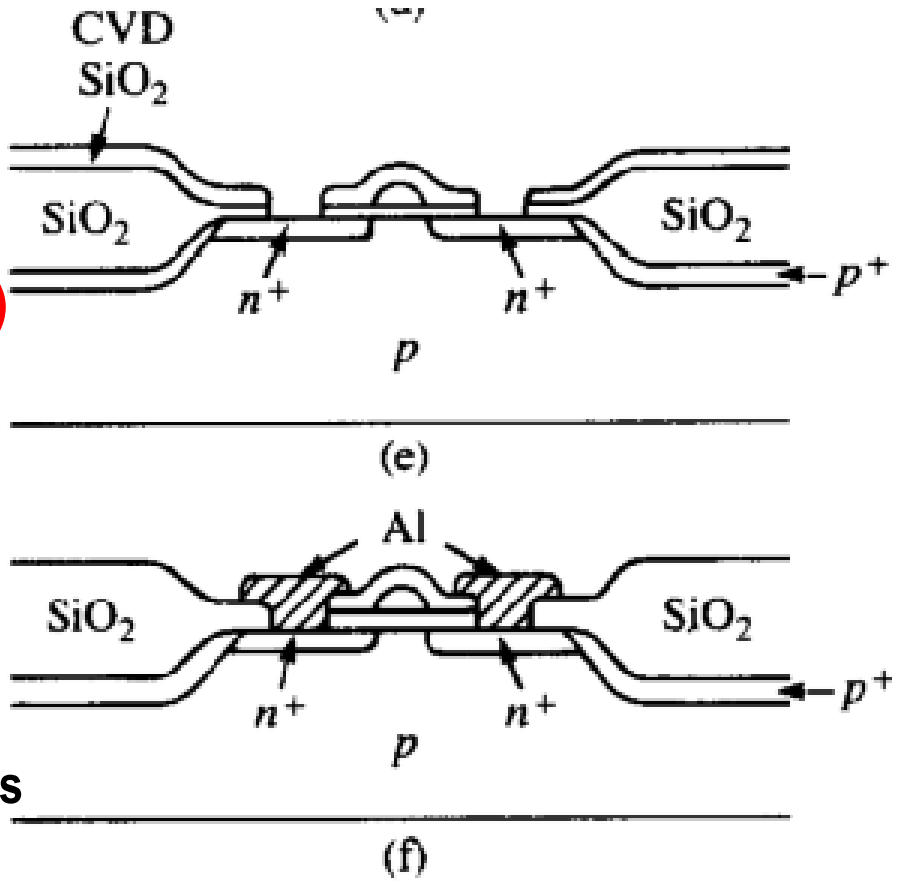
Process Flow Example #3 cont.

11) SiO_2 CVD

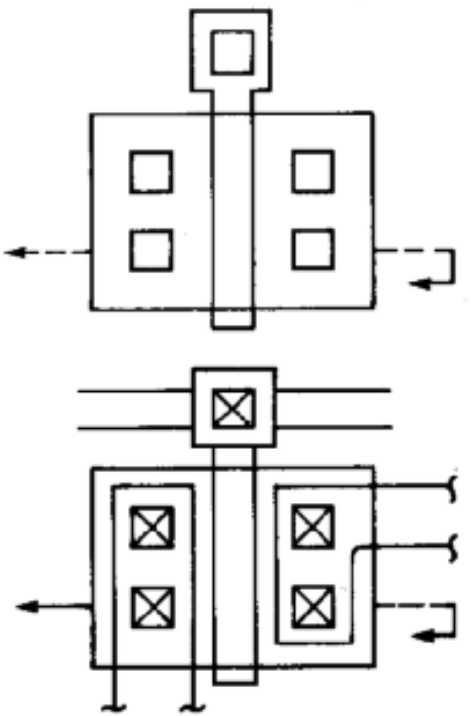
12) Contact holes
Definition (litho. & etch)

13) Al deposition
by sputtering

14) Al patterning
(litho. & etch)
to form interconnects



Top view of masks

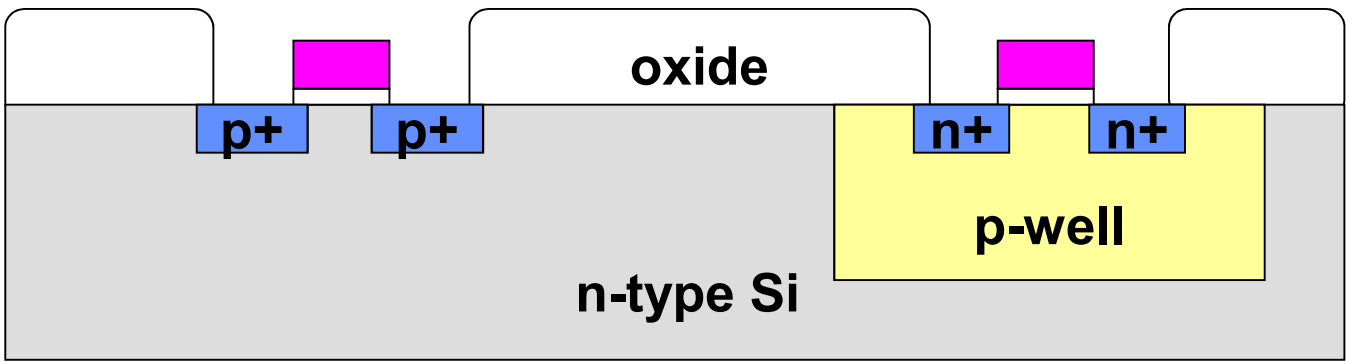


Example #4: CMOS Technology

Build both NMOS & PMOS transistors on a single silicon chip

- **N-MOSFETs need a p-type substrate**
- **P-MOSFETs need an n-type substrate**

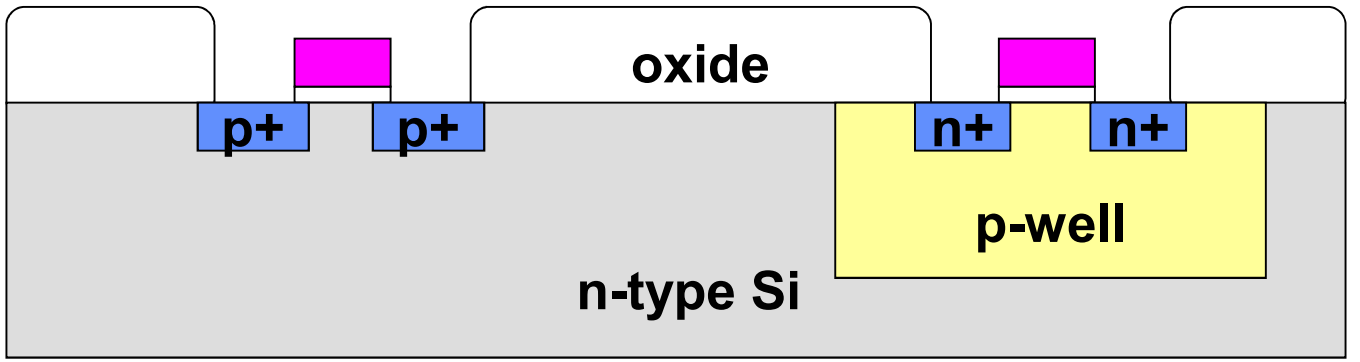
→ What extra process steps will be needed ?



A Simplified Conceptual CMOS Process to illustrate process flow

n-type wafer

*Create "p-well"



Grow thick oxide

***Remove thick oxide in transistor areas ("active region")**

Grow gate oxide

Deposit & *pattern poly-Si gate electrodes

*Dope n channel source and drains (need to protect PMOS areas)

*Dope p-channel source and drains (need to protect NMOS areas)

Deposit insulating layer (oxide)

*Open contact holes

→ At least 3 more masks, as compared to NMOS process

Deposit and *pattern metal interconnects

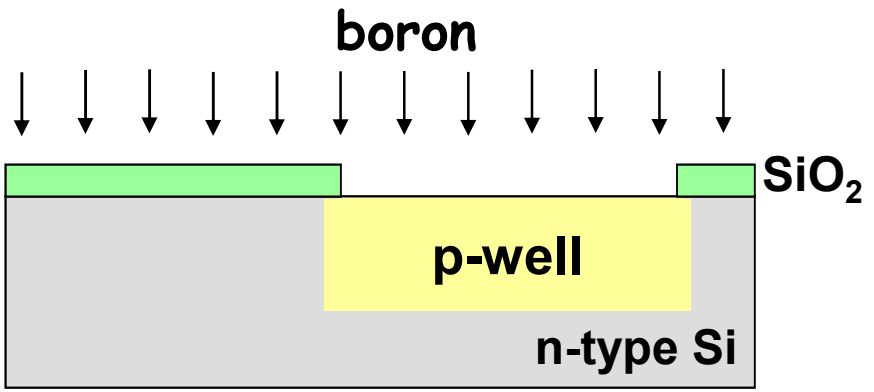
**A detailed CMOS Process will be presented later in course when we study Process Integration

Additional Process Steps Discussion

1. Well Formation

Top view of p-well mask

Cross-sectional view of wafer



- grow oxide layer; pattern oxide using p-well mask

- implant boron; anneal to form deep p-type region

2. Masking the two different Source/Drain Implants

"Select p-channel" → We must protect the n-channel devices during the boron implantation step, and

"Select n-channel" → We must protect the p-channel devices during the arsenic implantation step

Example: Select p-channel, use photoresist as boron implantation mask