Chip Layout:

Device Sizes:
Layout dimensions dimensions are in micrometers (1 µm = 1 micrometer). All contact holes are 5 µm x 5 µm. Metal pads are 100 µm x 100 µm. The devices are listed below by device number:

1a) Resolution Test Patterns (1 per mask):
Line widths as marked: 2, 3, 4, and 8 µm
Rails: 10 µm

1b) Alignment Marks and Verniers:
Vernier steps: 0.2 µm

2a) Diffused Resistor:
20 squares (L = 200 µm, W = 10 µm)

2b) Poly Resistor:
20 squares (L = 200 \text{\,\mu m}, W = 10 \text{\,\mu m})

2c) \textbf{Metal-to-Diffusion Contact Chain:}
14 contacts. Diffused segments: L = 150 \text{\,\mu m} \times W = 50 \text{\,\mu m}

2d) \textbf{Metal-to-Poly Contact Chain:}
14 contacts. Diffused segments: L = 150 \text{\,\mu m} \times W = 50 \text{\,\mu m}

3) \textbf{Field Oxide Capacitor:}
Top Metal Plate: 200 \text{\,\mu m} \times 200 \text{\,\mu m}

4) \textbf{Gate Oxide Capacitor:}
Active Area: 200 \text{\,\mu m} \times 200 \text{\,\mu m}
Top Plate (poly): 240 \text{\,\mu m} \times 240 \text{\,\mu m}
Metal Contact Pad (not including metal-poly overlap): 95 \text{\,\mu m} \times 240 \text{\,\mu m}

5) \textbf{Intermediate Oxide Capacitor:}
Top Metal Plate: 200 \text{\,\mu m} \times 200 \text{\,\mu m}

6a) \textbf{Junction Capacitor:}
Active Area: 300 \text{\,\mu m} \times 140 \text{\,\mu m}

6b) \textbf{Long Periphery Junction Capacitor:}
Center of Active Area: 300 \text{\,\mu m} \times 140 \text{\,\mu m}
Fins: 150 \text{\,\mu m} \times 20 \text{\,\mu m}

7) \textbf{Diode:}
Active Area: 50 \text{\,\mu m} \times 50 \text{\,\mu m}

8) \textbf{MOSFETs of various lengths:}
W/L = 15/4, 15/6, 15/8, 15/10 \text{\,\mu m}

9) \textbf{Long Channel MOSFETs:}
W/L = 10/20, 15/20, 20/20 \text{\,\mu m}

10) \textbf{Large MOSFET:}
W/L = 100/100 \text{\,\mu m}

11) \textbf{Field Oxide MOSFET:}
W/L = 100/100 \text{\,\mu m}

12) \textbf{Circular MOSFET:}
W/L = \sim 560/20 \text{\,\mu m}

13) \textbf{Lateral BJTs}
Base Widths = 5, 7, 9 \text{\,\mu m}
Emitter Dimensions (Active Area): 50 \text{\,\mu m} \times 50 \text{\,\mu m}

14) \textbf{Inverter:}
Load: W/L = 10/20 \text{\,\mu m}
Driver: W/L = 80/10 \text{\,\mu m}

15) \textbf{NOR Gate:}
Load: W/L = 10/20 \text{\,\mu m}
Driver: W/L = 80/10 \text{\,\mu m}

16) \textbf{Ring Oscillator (17 stages + buffer):}
Load: W/L = 10/20 \text{\,\mu m}
Driver: W/L = 80/10 \text{\,\mu m}

\textbf{For MEMS Layout, check the MEMS Chip Layout Page}

\textbf{Initials of the designers}
Resolution Test Pattern Layout:

1) Resolution Test Patterns (1 per mask):

Line widths as marked: 2, 3, 4, and 8 µm
Rails: 10 µm
Alignment Marks and Vernier Layout

1b) Alignment Marks and Verniers:

Vernier steps: 0.2 \( \mu \text{m} \)

\[ \text{step} = 0.2 \mu \text{m} \]
Resistor Layout:

2a) Diffused Resistor:

20 squares (L = 200 µm, W = 10 µm)

2b) Poly Resistor:

20 squares (L = 200 µm, W = 10 µm)
Contact Chain Layout:

2c) Metal-to-Diffusion Contact Chain:

14 contacts. Diffused segments: L = 150 µm x W = 50 µm

2d) Metal-to-Poly Contact Chain:

14 contacts. Diffused segments: L = 150 µm x W = 50 µm
**Field Oxide Capacitor Layout:**

3) Field Oxide Capacitor:

Top Metal Plate: 200 µm x 200 µm
Gate Oxide Capacitor Layout:

4) Gate Oxide Capacitor:

Active Area: 200 µm x 200 µm
Top Plate (poly): 240 µm x 240 µm
Metal Contact Pad (not including metal-poly overlap): 95 µm x 240 µm
Intermediate Oxide Capacitor Layout:

5) Intermediate Oxide Capacitor:

Top Metal Plate: 200 µm x 200 µm
Junction Capacitor Layout:

6a) Junction Capacitor:

Active Area: 300 µm x 140 µm
Long Periphery Junction Capacitor Layout:

6b) Long Periphery Junction Capacitor:

Center of Active Area: 300 µm x 140 µm
Fins: 150 µm x 20 µm
Diode Layout:

7) Diode

Active Area: 50 µm x 50 µm
MOSFETs of Various Lengths Layout:

8) MOSFETs of various lengths:

W/L = 15/4, 15/6, 15/8, 15/10 µm
8c 15/8μm

8d 15/10μm
Long-Channel MOSFETs of Various Widths Layout:

9) Long Channel MOSFETs:

W/L = 10/20, 15/20, 20/20 μm
Large-Area MOSFET Layout:

10) Large MOSFET:

W/L = 100/100 \mu m
Field Oxide MOSFET Layout:

11) Field Oxide MOSFET:

W/L = 100/100 μm
Circular MOSFET Layout:

12) Circular MOSFET:

W/L = ~560/20 \mu m
Lateral BJT Layout:

13) Lateral BJTs

Base Widths = 5, 7, 9 µm
Emitter Dimensions (Active Area): 50 µm x 50 µm
BJT
$X_B = 9 \mu m$
Inverter Layout:

14) Inverter:

Load: W/L = 10/20 μm
Driver: W/L = 80/10 μm
NOR Gate Layout:

15) NOR Gate:

Load: W/L = 10/20 μm
Driver: W/L = 80/10 μm
Ring Oscillator Layout:

16) Ring Oscillator (17 stages + buffer):

Load: W/L = 10/20 μm
Driver: W/L = 80/10 μm
Layout Designers

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