Spring 2006

UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering and Computer Sciences

EE143 Midterm Exam #2

Family Name _____ First name_____SID_____

Signature_____Solutions_____

Make sure the exam paper has 7 pages total (including cover page)

Instructions: DO ALL WORK ON EXAM PAGES
This is a 90-minute exam (8 sheets of HANDWRITTEN notes allowed)

Grading:

- **The reader can only assess what you put down on the exam paper, not what is inside your brain. Please be concise with your answers. For answers requiring explanation, adding sketches can be very effective.**
- **To obtain full credit, show correct units and algebraic sign. Numerical answers orders of magnitude off will receive no partial credit.**

Problem 1 (25 points)_____

Problem 2 (25 points)_____

Problem 3 (25 points) _____

Problem 4 (25 points) _____

TOTAL (100 points) _____

Problem 1 Lithography (25 points total)

(a) An optical stepper using G-line illumination (λ =436 nm) and NA=07 can produce a minimum printable feature l_m of 0.5 μm with a Depth of Focus of 1 μm.

The stepper is modified by changing the light source wavelength to 365nm (I-line) and by placing an aperture before the lens to reduce NA to 0.5.

	λ	NA
Old Stepper	436 nm	0.7
Modified stepper	365 nm	0.5

With the lithography technology factors being the same,

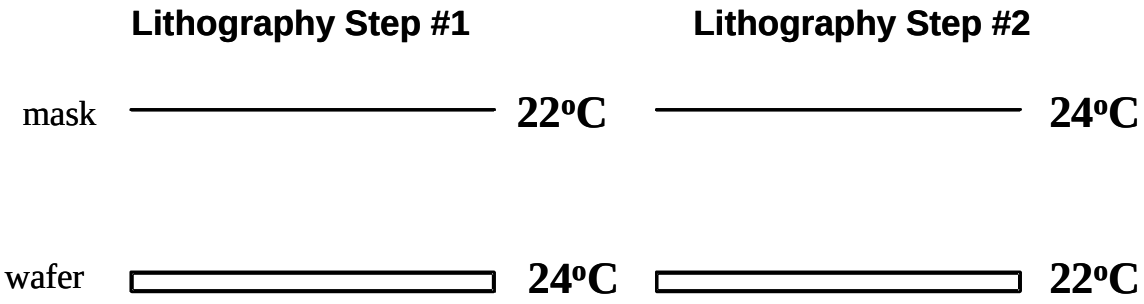
(i) (4 points) Calculate the new l_m

$$l_m \text{ (modified)} = l_m \text{ (old)} \times \frac{(\lambda/NA)(\text{modified})}{(\lambda/NA)(\text{old})} = \mathbf{0.586}\ \mu\mathbf{m}$$

(ii) (4 points) Calculate the new DOF

$$\text{DOF (modified)} = \text{DOF(old)} \times \frac{(\lambda/NA^2)(\text{modified})}{(\lambda/NA^2)(\text{old})} = \mathbf{1.64}\ \mu\mathbf{m}$$

(b) (8 points) With an 1X optical stepper, at lithography step #1, alignment marks are transferred to edge of the 100mm-diameter wafer with mask temperature at 22°C and wafer temperature at 24°C. At lithography steps #2, mask temperature is at 24°C and wafer temperature is at 22°C.



Calculate the thermal run-out (or run-in) error in microns for the alignment marks at lithography Step #2.

Given : Linear coefficients of expansion of mask material = 6×10^{-6} /°C

Linear coefficients of expansion of Si wafer = 2.3×10^{-6} /°C

$R = r\,(\Delta T_m \alpha_m - \Delta T_{Si} \alpha_{Si})$

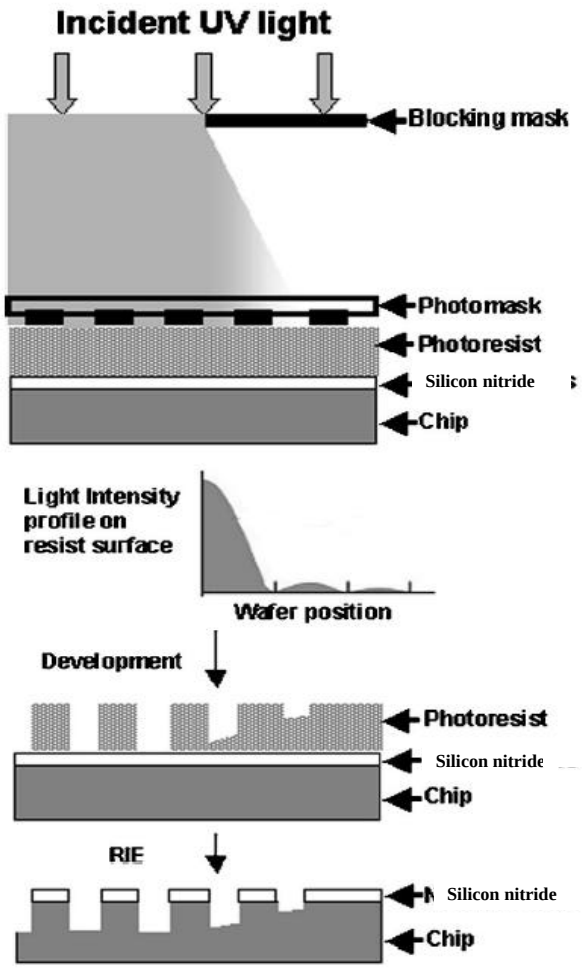
With $\Delta T_m = +2°C$ and $\Delta T_{Si} = -2°C$.

Mask image is bigger than wafer marks (thermal run-out)

$\therefore R = 50\text{mm} \times (1.2 \times 10^{-5} + 4.6 \times 10^{-6}) = 0.83\ \mu\text{m}$.

Problem 1 continued

(c) The following schematic illustrates how one can **GRADUALLY** reduce the height of an array of microfluidic channels in a substrate with one single lithography exposure. The channel patterns are defined by a photomask with contact printing. An additional blocking mask is used to modulate the lateral light intensity with edge diffraction.



(i) (5 points) For this special application, do you prefer a high or low photoresist contrast (γ)? Explain briefly.

Since we want a gradual transition of the remaining resist thickness when the light intensity varies, we prefer a LOW RESIST CONTRAST

(ii) (4 points) After photoresist development, describe steps you will use to transfer the resist pattern to the substrate. Specifically mention the selectivity and anisotropy of the etching processes.

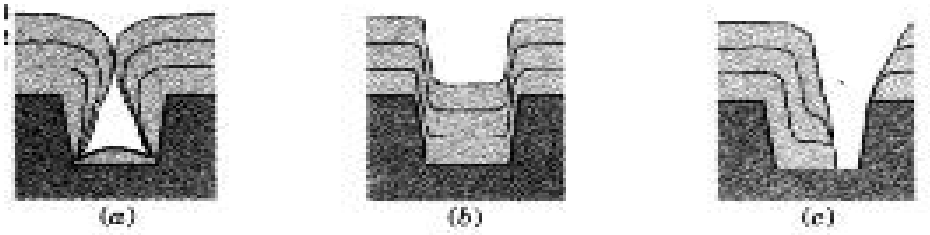
Process : Choose a highly anisotropic RIE process , and with selectivity between resist , nitride, and substrate ~ 1 (i.e. approximately same vertical etching rates)

Alternative Process

If one RIE recipe cannot be found, use two separate RIE processes with ~1:1 selectivity between resist and nitride, and nitride and substrate. Both highly anisotropic.

Problem 2 Thin Film Deposition (25 points total)

(A) **Evaporation** is used to deposit a thin film onto a substrate with trench structures. The following three sketches show time development of thin film (grey layers) topography. Describe the deposition conditions which can explain the features for cases (a) , (b) and (c). Illustrate with sketches if necessary.



Feature of Evaporation : small-area source and directional deposition flux.

Case (a) (3 points) Deposition condition

Rotating and tilting wafer during deposition

Case (b) (3 points) Deposition condition

Trench structures directly above evaporation source

Case (c) (3 points) Deposition condition:

Evaporation flux making an oblique angle with wafer (e.g. wafer tilt)

(B) **Consider the two control variables of CVD : temperature T, and gas flow velocity U.**

(i) (6 points) If high growth rate is the only consideration, choose conditions for T (high or low) and U (high or low) . Briefly explain you rationale.

Deposition Rate $= [1/ (1/ k_s + 1/ h_G)] (C_g / C_{solid})$ $k_s(T) \propto \exp [-E_A/kT]$ and $h_G (T) \propto T^{3/2}$ and $h_G (T) \propto U^{1/2}$

High T and High U will increase BOTH h_G and ks. Higher deposition rate

(ii) (5 points) If film thickness uniformity is the only consideration, choose conditions for T (high or low) and U (high or low) . Briefly explain you rationale.

Wafer can be very isothermal inside a furnace, flow velocity depends on position.
Making hG >>ks will make hG variation insensitive to overall growth rate (i.e., surface reaction limited)
Prefer Low T and High U
[Note: Chemical reaction takes place at film surface which is isothermal. Surface diffusion effects due to lateral concentration gradient is only secondary]

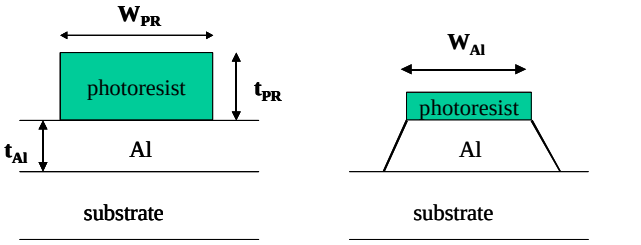
(i) (5 points) If conformal coverage over steps is the only consideration, choose conditions for T (high or low) and U (high or low) . Briefly explain you rationale.

For isothermal surface, surface reaction limited growth with give same growth rate over surface topography.
Prefer low T and high U

Problem 3 Etching (25 points total)

(a) Aluminum film of thickness t_{Al} is deposited on a substrate. Line patterns of photoresist is used as the etching mask with width W_{PR} and thickness t_{PR}. A reactive ion etching recipe is used to etch the Aluminum with the following characteristics (including variation if any):

Photoresist thickness $t_{PR} = 1.0 \pm 0.1$ μm
Aluminum thickness $t_{Al} = 1.1 \pm 0.3$ μm
Degree of anisotropy of Al etching = 1
Vertical etching rate of Al = 1 μm/min (no variation)
Selectivity of Al over photoresist: S varies from 2:1 to 4:1 (vertical etching rates)
Degree of anisotropy of photoreist etching =0
Etching does not attack substrate



Cross-section before etching Cross-section when Al is just cleared

(i) (3 points) What is the etching time (in minutes) that the thickest aluminum lines are just cleared ?

t = t_{al}(max)/Al etching rate = 1.4/1= 1.4 minutes

(ii) (4 points) What is the **minimum** photoreists thickness remaining when the thickest aluminum lines are just cleared?

Worst-case photoresist thickness removal
= t × photoresist etch rate (max)
= 1.4 × [1 μm/minute /S(min)] =1.4/2 = 0.7 μm
Worst-case remaining photoresist thickness = 0.9 –0.7 =**0.2 mm**

(iii) (5 points) If the top width of aluminum line (W_{Al}) has to exceed 1 μm , what is the required **minimum** initial photoresist width W_{PR}?

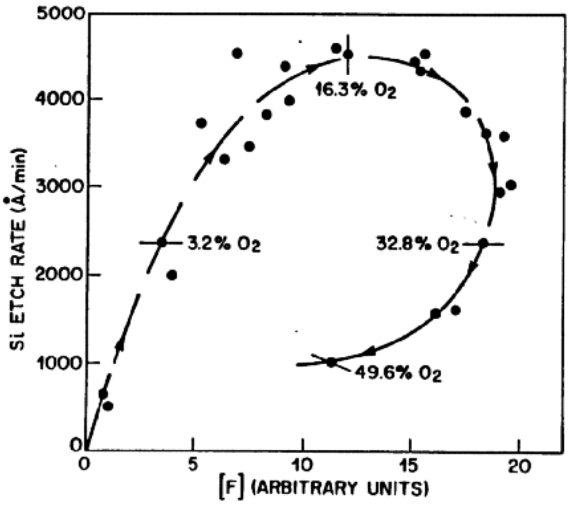
Lateral mask erosion = vertical mask erosion = 0.7 μm (because degree of anisotropy =0)
Minimum W_{PR} = 1 +2 ´ 0.7 = 2.4 mm

(b) (4 points) With all etching parameters in part(a) being the same, except degree of anisotropy of Al etching is now < 1, re-sketch qualitatively the cross-section when Al is cleared. Write down description of the major differences.

(1) W_{Al} will be smaller (underneath the photoresist pattern)
(2) Sidewall of Al will be a curve, not a straight line.

Problem 3 continued

(b) The Si etching rate in a $CF_4 + O_2$ plasma is plotted as a function of [F*] concentration for various oxygen content. F* is the excited F atoms.



(i) (3 points) With O_2 percentage below a certain value (i.e. 16.3%,) , explain why the Si etching rate increases with oxygen content in the plasma

Adding oxygen to CF4 plasma will generate more F* radicals. Si+F =SiFx reaction increase and hence is the Si etching rate.

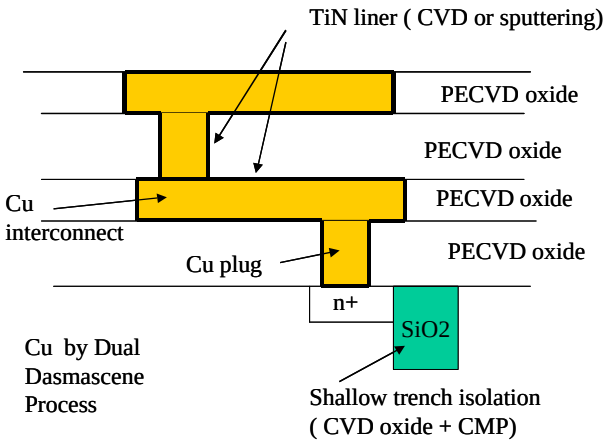
(ii) (3 points) With O_2 percentage increase 0 to 16%, do you expected the Si etching profile will become more isotropic or anisotropic. Explain your answer.

The Si+F=SiFx reaction is chemical in nature with no prefer directionality. Etching of Si more ISOTROPIC with more F*.
Another "possibility" : Oxygen will react sidewall hydrocarbon passivation layer to form volatile compounds. Lateral etching possible.

(ii) (3 points) With O_2 percentage above a certain value (i.e. 16.3%,) , explain why the Si etching rate decreases with oxygen content in the plasma

Si surface is oxidized by the oxygen to form SiO2 which has a slower etching rate than Si.

Problem 4 Metallization (25 points total)
The following schematic shows the cross-section of a Copper Dual Damascene multilevel metallization.



(i) (3 points) How many copper deposition steps are used ?

Two copper deposition steps

(ii) (3 points) List the Chemical-Mechanical Polishing (CMP) steps used and the purpose ?
CMP1- STI palnarization
CMP2- Dual Damascence Cu 1
CMP3- Dual Damascence Cu 2

(iii) (4 points) Describe the purpose(s) of using the TiN liner.

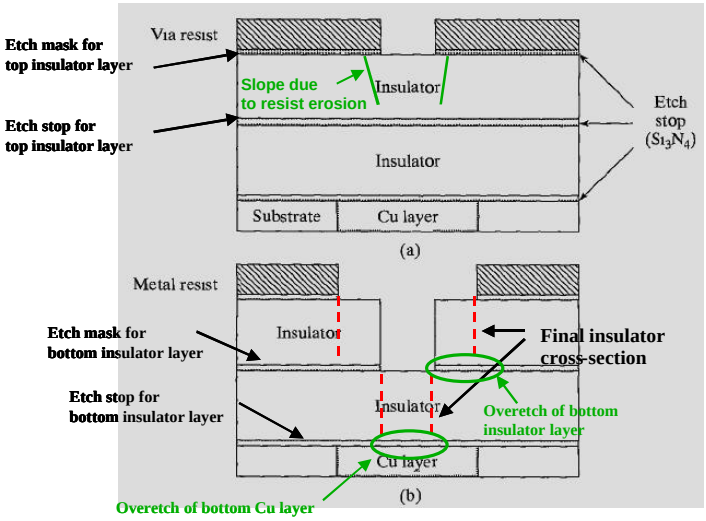
Diffusion barrier to prevent Cu outdiffusion and also a seed layer for Cu deposition (if plating is used)

(iv) (3 points) Why do we use shallow trench oxide isolation (instead of conventional local oxidation) ?
Planarizatin of the substrate and reduced oxide isolation spacing

(v) (3points) Why do we use plasma enhanced CVD oxide instead of thermal CVD oxide ?

Lower deposition temperature (~400C) instead 800C for thermal CVD

(vi) (6 points) Your textbook (Jaeger) describes a thin silicon nitride layer is used between the PECVD oxide layers as etch stops [not shown in above schematic]. Use sketches to illustrate the advantage of using these etch stops.



Etch stop essential if oxide layers have different thickness.

(vii) (3 points) Copper has a larger activation energy E_A for interconnect electromigration failure than aluminum. Is this good or bad ? Explain.
MTF proportional to exp ($+E_A/kT$). Long electromigration lifetime is desirable for interconnects.