Homework Assignment # 11 (Due Nov 22, Tue 9am !!!)

Required Reading

(1) EE143 Lecture Notes

(2) Visit the Device Visualization website http://jas.eng.buffalo.edu/

Start with http://jas.eng.buffalo.edu/education/mos/mosCap/biasBand10.html

(a) Run all four simulation of the MOS capacitors (set Q_{ox} =0 first and then see effect of Q_{ox} later.

(b) Run all three MOSFET simulations on http://jas.eng.buffalo.edu/education/mos/mosfet/mosfet.html

(3) Section of Streetman Chapter 8 on MOS (in Bspace Resources Directory)

Problem 1 Simple threshold voltage calculations

(a) Calculate the threshold voltage of an NMOS transistor when the **p-substrate** concentration is 2×10^{16} cm^{-3}, n+ poly-Si is used as the gate material, and a gate oxide thickness of 90nm. Assume there is no body bias and no oxide charges.

(b) Repeat part (a) for a PMOS transistor with **n-substrate** concentration = $2 \times 10^{16} cm^{-3}$. Gate material and oxide thickness are the same.

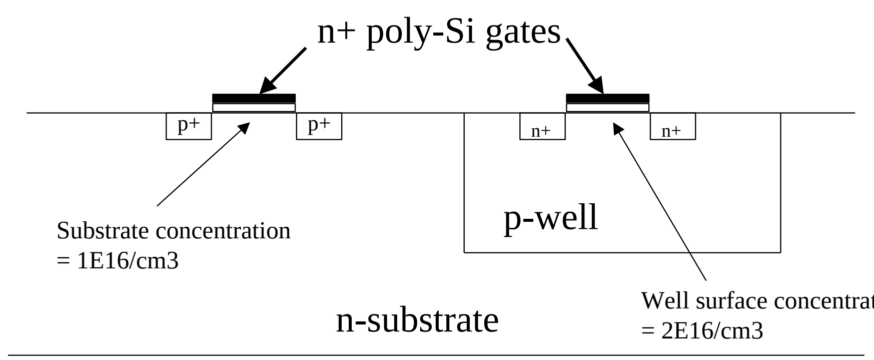
Problem 2 Threshold voltage calculation with Oxide Interface Charge and Threshold Implant

(a) Poly-Si gate (n^+) **NMOS** devices are fabricated with $5 \times 10^{15}/ cm^3$ boron-doped substrate. Assuming the Si/SiO2 interface charge Q_f to be $+3 \times 10^{10} q\ cm^{-2}$, find the required gate oxide thickness for V_T = +1.0 volt.

(b) Phosphorus is implanted through the gate oxide of the NMOS device described in part (a) such that **all** implanted phosphorus are inside the Si and are localized at Si-SiO_2 interface as a delta-function. Find the implantation dose required to make V_T = - 2 volts.

Problem 3 Threshold implant for CMOS

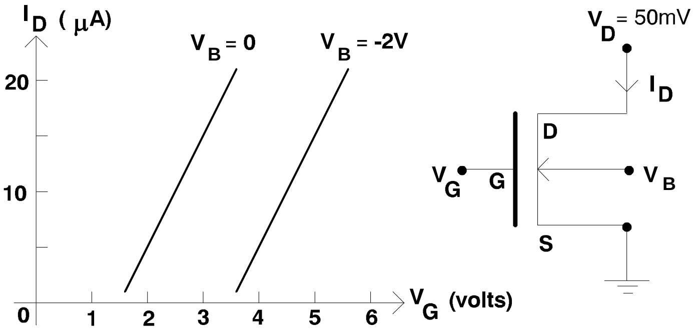
A p-well CMOS process uses n^+ poly as the gate material for both the n and p channel devices. The gate oxide thickness is 22nm with no oxide or interface charge. The n-substrate has a doping concentration of $10^{16}/ cm^3$ and the p-well has a doping concentration of $2 \times 10^{16}/ cm^3$ near the surface region.



A blanket threshold implant step is performed for both the n and p channel devices.(same specie, same dose). Our design goal is to make $V_{TN} = - V_{TP}$ after the implant. **Determine the implant dopant specie AND the required implant dose**.

Problem 4 Simple MOSFET I-V Analysis

The I_D versus V_G curves for a n-channel enhancement-mode MOSFET with a small fixed V_{DS} (=50 mV) are shown below. The transistor channel length is 10 μm and the channel width is 100 μm, with a gate oxide thickness of 1000 Å.

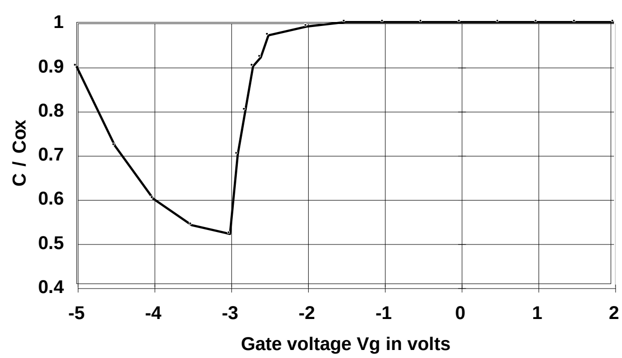


(a) Find the threshold voltages for (i) V_B=0 and (ii) V_B=-2V.
(b) Find the substrate doping concentration (assume the substrate is uniformly doped).
(c) Find the carrier mobility in the channel.
(d) Find I_{Dsat} of the transistor for V_B=0 and V_G =5V .

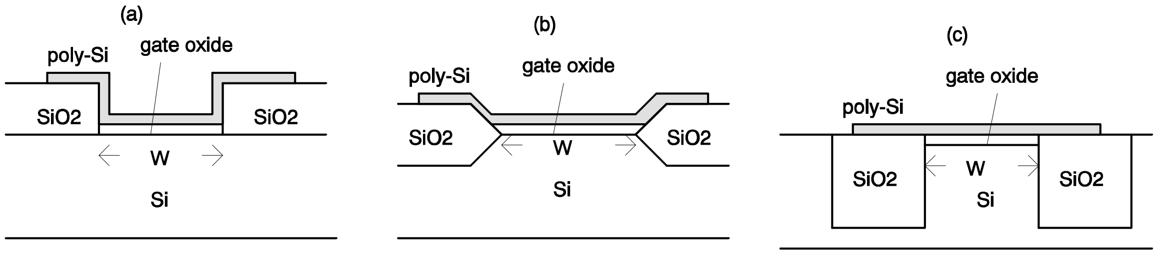
Problem 5 C-V Analysis

Experimental MOS data of C / C_{ox} versus V_G are given below . It is known that the oxide thickness is 260 nm, the SiO_2-Si interface charge Q_f= $+3.6\times 10^{11}$q /cm^2.

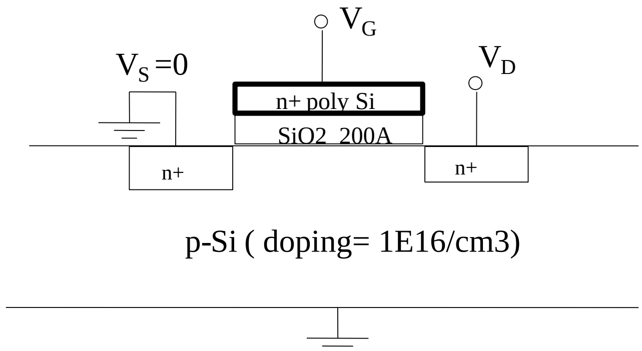
(a)Calculate the maximum depletion layer thickness, x_{dmax}
(b)Estimate the substrate doping concentration N_a (ANSWER REQUIRES ITERATION)
(c) Calculate the work function of the gate material.



Problem 6 MOS Narrow Width Effect
For identical **channel widths** W, discuss which one of the following three oxide isolation schemes will exhibit the most narrow width effect.: (a) oxide window, (b) LOCOS and (c) shallow trench oxide isolation. Illustrate your answer with sketches or a few sentences. [Note: the cross-sections are along the channel width direction, NOT the channel length direction]



Problem 7 Past exam question



The following cross-section shows a NMOS transistor with **n+ poly-Si gate**, gate oxide thickness = 20nm, and a p-substrate with doping concentration = 1E16/cm^3.

(a) Thermal SiO2 will have electrical breakdown when the electric field is > 8×10^6 V/cm. What is the **maximum** V_G that can be applied without causing gate oxide breakdown?

(b) If there is no oxide or oxide interface charge, calculate the threshold voltage V_T for V_D =0.

(c) Calculate the thickness of the depletion region (x_{dmax}) underneath the gate oxide when $V_G = V_T$, with V_D =0.

(d) Calculate the drain current for $V_G = V_D = 5$ volts. Use k =50 µA / V^2.

Note: I_{DS} (triode region) $= k\,[\,(V_G - V_T)\,V_{DS} - V_{DS}^2/2\,]$; I_{DS} (saturation region)$=k[(V_G-V_T)^2/2]$

(e) If a boron threshold implant is performed with a dose of 10^{12}/cm^2. What is the new threshold voltage of the transisitor.[You can assume the boron implant concentration profile is a delta function located exactly at the Si/SiO2 interface].

(f) What is the drain current for $V_G = V_D = 5$ volts for the MOSFET with the boron threshold implant described in part (e)?

(g) A small-signal C-V measurement across the gate and substrate terminals is performed with the MOSFET structure. V_D is grounded to zero voltage. Sketch qualitatively the C versus V_G curve from –10V to +10V.

(h) Calculate the maximum C value (in F/cm^2) and the minimum C value (in F/cm^2).