N.CHEUNG **EE143, Fall 2010**

Homework Assignment # 8 (Due Oct 29, Friday 9am)

Reading Assignment

Introduction: Chapter 7 of Jaeger on Interconnect and contacts
Section 3.8.2 of Jaege -.Brief description of CMP
Reprint: Chapter 15 Campbell on metallization [You can skip sections 15.1 and 15.5]

Problem 1 RC Time constant

Aluminum-copper-silicon alloy has a resistivity of 3.2 μohm-cm.
(a) What is the sheet resistance of a 1-μm-thick film.
(b) What would be the resistance of a line 500 μm long and 10 μm wide?
(c) What is the capacitance of this line to another parallel identical line separated by 1 μm of SiO2 ? Relative permittivity of SiO2 is 3.9.
(d) What is the RC time constant associated with this 500 μm-long line?
(e) If the oxide is replace by a gap filled with air (relatively permittivity =1), what is the new RC time constant ?

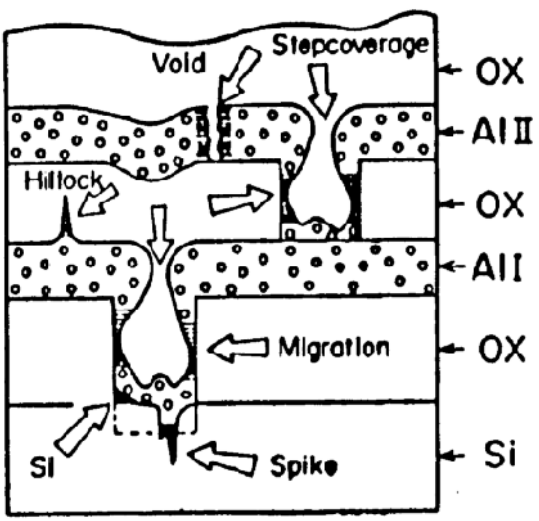
Problem 2 Electromigration failure

a) Electromigration failure time depend exponentially on 1/temperature.
What is the ratio of the MTFs of identical aluminum interconnects operating at the same current density at 300 K and 400 K? Use an activation energy $E_A = 0.5$ eV for aluminum electromigration failure.

b) For interconnect reliability, design rules are used to ensure the current density of interconnects is below a safety value. What is the maximum current that may be allowed to flow in an aluminum conductor 1 μm thick and 1 μm wide if the current density must not exceed 5×10^5 A/cm^2

Problem 3 Issues with Al metallization

The following cartoon shows some major problems of using Al as the metal for multilevel metallization. Describe your understanding of the origins AND methodologies used to minimize/eliminate such problems.

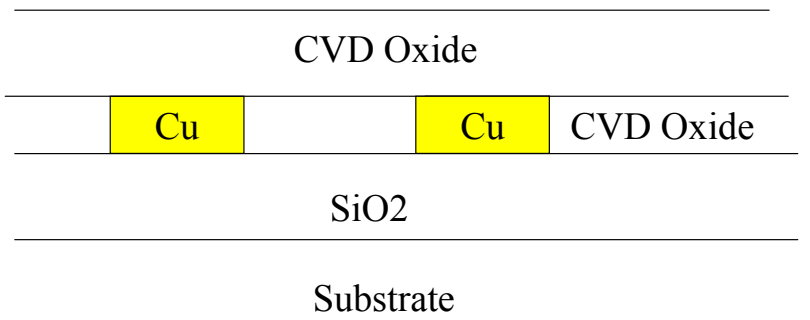


(a) Hillock and Void formation in interconnects
(b) Al spiking into silicon substrate
(c) Step coverage problem

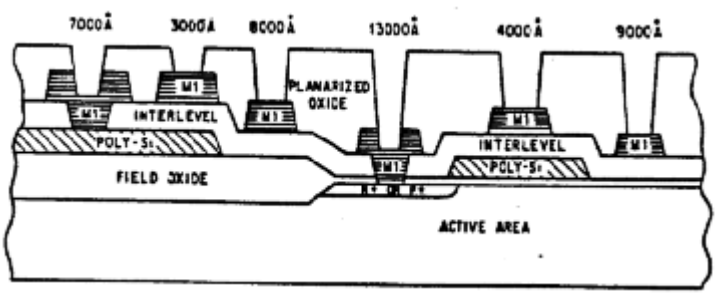
Problem 4 Copper interconnect process

Copper is proposed as an interconnect material in newer generation of ICs because of its low electrical resistivity. There is no reliable process recipe to etch copper by RIE. Propose and a process flow to fabricate copper interconnects in a planarized multilevel metallization scheme.

Which method will you use to deposit copper?
How will you pattern copper interconnects? .
Starting with a SiO_2 layer on Si substrate, show your steps with process description and cross-sections.



Problem 5 Planarization
The following cross-section (Fig.A) shows a poorly planned planarization process with planarization starting only at the Planarized Oxide step.



(a) What difficulties you will encounter when etching contact holes through the Planarized Oxide to reach the Metal-1 (M1) surface ?
(b) Instead of using LOCOS to form the Field Oxide, propose another isolation oxide structure to achieve better planarization. Sketch Fig.A again with your proposed isolation.
(c) Continue with your structure in part(b), let us improve the planarization by performing a planarization step after the interlevel dielectric layer is deposited. Sketch Fig.A again.
(d) After part(c) , you find you can still improve the planarization by putting a tungsten plug between M1 and the substrate N+ or P+ contact. Sketch Fig.A again with this improvement.