

## Homework Assignment # 1 Solutions

## Problem 1 Processing Terminologies

(a)

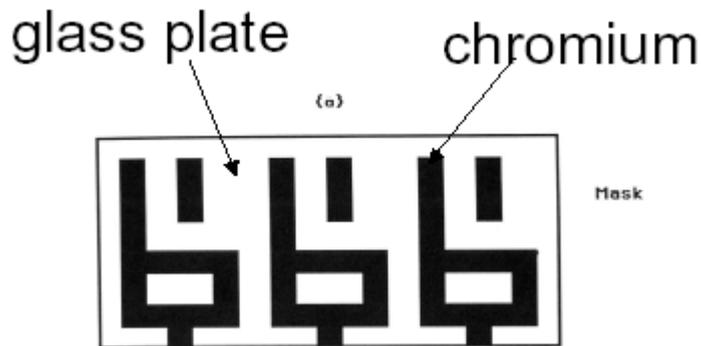
**“Growing” an oxide layer:** Thermal oxidation is used to form  $\text{SiO}_2$  by reacting the Si substrate atoms with oxygen or steam. Si substrate atoms will be consumed using this process.

**“Depositing” an oxide:** The  $\text{SiO}_2$  material is deposited from external sources (e.g. by chemical vapor deposition or sputtering deposition methods). No Si substrate atoms will be consumed to form the  $\text{SiO}_2$ .

(b)

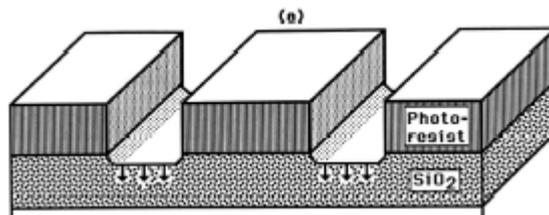
(i) What is a photomask?

The glass plate with chromium patterns used in optical lithography. Chrome regions will block out the light and will not expose the photoresist.



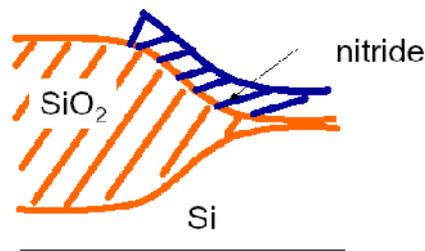
(ii) What is an etching mask? Quote one example.

Patterns of materials on the wafer which protects the regions underneath from being etched. Example: photoresist patterns on an oxide layer.



(iii) What is an oxidation mask? Quote one example.

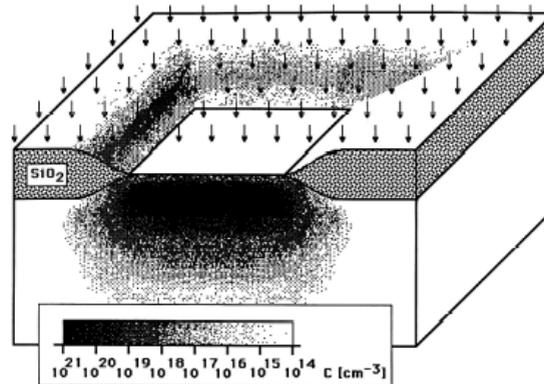
Patterns of materials on the wafer which protects the regions underneath from being oxidized during a thermal oxidation step. Example:  $\text{Si}_3\text{N}_4$  patterns on top of Si wafer



(iv) What is an implantation mask? Quote one example.

Patterns of materials on the wafer with sufficient physical thickness to block the penetration of ions during the implantation step.

Example: Thick photoresist or thick oxide patterns on top of wafer.



## Problem 2

1) A total of 4 lithography steps are used in this Al-gate process

Mask 1 . Pattern thick oxide to define the source/drain area

Mask 2 Pattern gate area

Mask 3 Pattern contact holes for Al contact to source/drain

Mask 4 Pattern Al interconnects

2) The photoresist cannot withstand processing temperature higher than ~180°C .Photoresist patterns will be distorted by reflow at moderate temperature and the resist material will be carbonized at high temperature. Because the source/drain diffusion step is at ~ 900 °C, photoresist has to be stripped prior to the diffusion step.

## Problem 3

(i) Pad Oxide grown by **Thermal Oxidation**.

(ii) Silicon nitride deposited by **Chemical Vapor Deposition**

(iii) **Gate oxide growth** by thermal oxidation

[Optional: Ok also to mention pad oxide removal by wet etching. This is done before gate oxide growth. The gate oxide can then be grown with very precise thickness control and minimal interface charge between oxide and silicon substrate.]

(iv) We cannot use thermal oxidation step to replace CVD oxide. The oxide layer is to electrically isolate the Al metallization from the poly-Si gate and substrate and require a sufficient thickness. If too much Si is consumed by using thermal oxidation in the poly-Si gate and source/drain regions , the gate dimensions and the n<sup>+</sup> source/drain thickness will be significantly reduced.

(v) No. Al will melt during the annealing step (~900°C) after source/drain dopant implantation.

## Problem 4

(i) **Three lithography steps** are used in this process flow.

Mask 1: Pattern Poly-1 hinge plate

Mask 2: Pattern the staple anchor openings through bottom PSG

Mask 3: Pattern the Poly-2 staple

(ii) **Four CVD steps** are used:

CVD1- bottom PSG deposition

CVD2- poly-1 deposition

CVD3- top PSG deposition

CVD4- poly-2 deposition

(iii) **Four thin-film etching steps** are used:

Etch 1: Etch Poly-1( hinge plate)

Etch 2: Etch staple anchor openings through bottom PSG

Etch 3: Etch Poly-2 (staple)

Etch 4: Etch all PSG sacrificial layers to release hinge

(iv) NO. Part of the hinge structure is **underneath** the staple structure. If staple is formed first, there is no way to pattern the hinge outline (litho and etch) AND no way to deposit the part of poly-1 which is underneath the staple structure.

(v) AGREE. There is no high-temperature processing steps used after Al deposition, Al melting is a non-issue.

[Optional answer: DISAGREE. One has to find a proper wet/plasma etching recipe with the right selectivity to etch PSG without attacking Al.]

(vi) Major differences (schematic shown below: red is structure using poly-1 oxidation) :

- (1) poly-1 plate thinner ( poly-Si is consumed during thermal oxidation)
- (2) cross-section of poly-1 under staple area is smaller (affects poly-1 & poly-2 gap spacing under staple)
- (3) staple cross-section has more vertical sidewalls because there is no PSG (layer 1).

